

A 110nm CMOS process with fully depleted high resistivity substrate for NIR, X-ray and charged particle imaging

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ABSTRACT

In this contribution, we present a customized 110nm CMOS process tailored for the fabrication of pixel sensors on fully depleted High-Resistivity substrates. The process was specifically developed for the detection of charged particles, but its characteristics make it suitable for high energy photons and NIR light imaging. Preliminary results from the electrical and functional characterization of test devices in the dark and with near infrared light sources are presented.

INTRODUCTION

The development of pixel detectors with large fully depleted active volumes can benefit many scientific and industrial applications. Charged particle trackers are used in high-energy physics, medical imaging and astrophysics. The efficient detection of X-rays in the energy range from 1-keV to 15keV also requires detectors with a thickness of a few 100s of μm (Figure 1). The same requirement is present for the detection of NIR light at wavelengths between 900nm and 1100 nm, where depletion depths of a few microns available in mainstream CMOS image sensors cannot provide a high quantum efficiency (Figure 2). Since such a large depleted silicon thickness can hardly be managed biasing the image sensor from the front side [1], several CMOS-compatible approaches using a backside bias have been proposed since the early 1990s [2-5].

PROCESS DEVELOPMENT

The process presented here was developed starting from a commercial 0.11 μm CMOS flow with several technology add-ons, including high-resistivity n-type substrates, additional front-side implantations and backside processing. All the fabrication steps have been carried out by LFoundry.

The first fabrication runs included a pixel array (Figure 3(a)) and a set of test structures for the qualification of the process flow (Figures 3(b) and 4). A deep pwell was added to allow placing a full CMOS electronics inside the pixels. The backside junction was obtained by ion implantation followed by laser annealing for dopant activation and was covered by an anti-reflective coating. To cope the large bias voltage required for the full substrate depletion, a termination structure consisting of multiple guard rings was implemented.

An n-type epitaxial layer with a doping concentration larger than the substrate was included to allow sensor operation at low voltage, avoiding the flow of a punch-through current between deep pwells and backside p+ region. The process and layout were optimized with the aid of TCAD simulations (Figure 5).

TEST DEVICES

A small pixelated sensor, consisting on an array of 24 x 24 pixels with 50 μm x 50 μm size was implemented in the first test run (Figure 6). The pixels include a readout channel based on charge-

integrating amplifier and a CDS stage. The architecture of the pixel array was designed for charged particle detection, with a gain of $21\mu\text{V}/e^-$ and a frame rate of 25 kfps.

The first silicon runs, with active thicknesses of 100, 300 and $400\mu\text{m}$, were processed. Backside diodes for the qualification of the termination structures with different number of guard rings were included (Figure 7). Among the test structures there are also pixel arrays having the same geometry as the main array but without integrated electronics and with the collection diodes connected in parallel (Figure 4). These structures were designed to obtain a larger flexibility for the electrical characterization of the pixels. Current-Voltage measurements could be used to estimate depletion voltage, punch-through voltage between deep wells and bottom p^+ implantation and average leakage current, while the dynamic response could be measured by connecting the charge-collection diodes to a wideband amplifier.

CHARACTERIZATION RESULTS

The characterization of backside test diodes on $300\mu\text{m}$ thick silicon substrates shows the effectiveness of the guard ring termination structures. With 10 guard rings, a backside voltage in excess of 400V could be applied (Figure 8).

Measurements on the pixel structures show that, at a typical operation voltage, the sensors can be fully depleted below 150V and undergo punch through above 220V. The dark current is in the pA range for small arrays of 8×8 pixels with $50\mu\text{m}$ pitch connected in parallel (Figure 9).

Dynamic measurements using a picosecond pulsed IR laser showed that, thanks to the full depletion, complete charge collection from the whole active volume can be obtained within a few 10s of ns (Figure 10). Full depletion also accounts for a low crosstalk between neighboring pixels (Figure 11).

CONCLUSION

The basic functionality of the proposed process was verified. The termination structures at the backside can stand the voltage necessary to fully deplete a thickness of a few 100s μm , and fast charge collection has been demonstrated experimentally on test structures. Design activities are currently going on to implement large area sensors for charged particle imaging applications.

ACKNOWLEDGEMENT

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REFERENCES

- [1] K. D. Stefanov et al., "Fully Depleted, Monolithic Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias", Proc. IISW 2017, paper P13.
- [2] W. Snoeys et al., "PIN detector arrays and integrated readout circuitry on high-resistivity float-zone silicon," IEEE Tran. Electron Devices, Vol. 41, No. 6, pp. 903-912, 1994.
- [3] Y. Arai et al., "Developments of SOI Monolithic Pixel Detectors," Nuclear Instr. Meth. Phys. Res. A, Vol. 623, No. 1, pp. 186-188, 2010.
- [4] S. Lauxtermann, V. Vangapally, "A Fully Depleted Backside Illuminated CMOS Imager with VGA Resolution and 15 micron Pixel Pitch," Proc. IISW 2013, paper 7.18.
- [5] A. Süß et al., "A Fully Depleted $52\mu\text{m}$ GS CIS Pixel with 6 ns Charge Transfer, $7 e^-_{\text{rms}}$ Read Noise, $80\mu\text{V}/e^-$ CG and $>80\%$ VIS-QE," Proc. IISW 2017, paper R59.

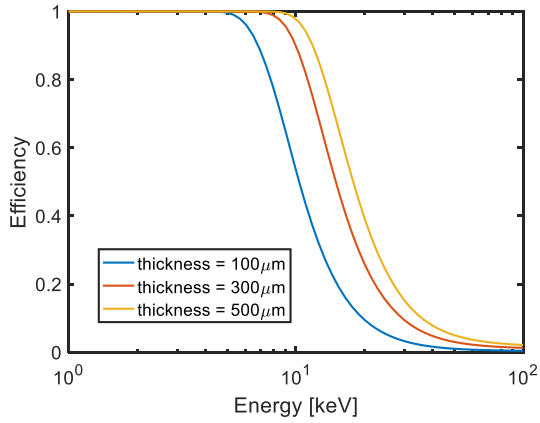


Figure 1. Calculated X-ray detection efficiency for a Si detector as a function of photon energy and detector thickness

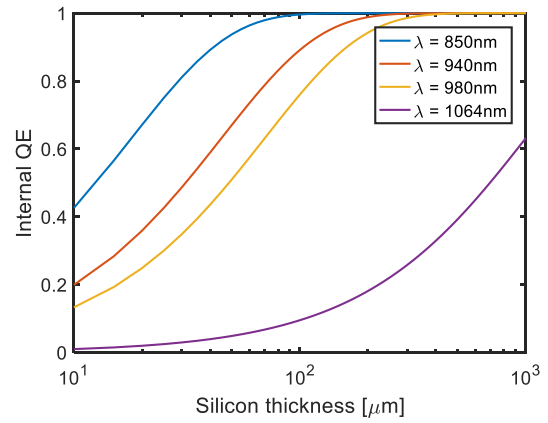


Figure 2. Calculated Internal Quantum Efficiency at different NIR wavelengths as a function of detector thickness.

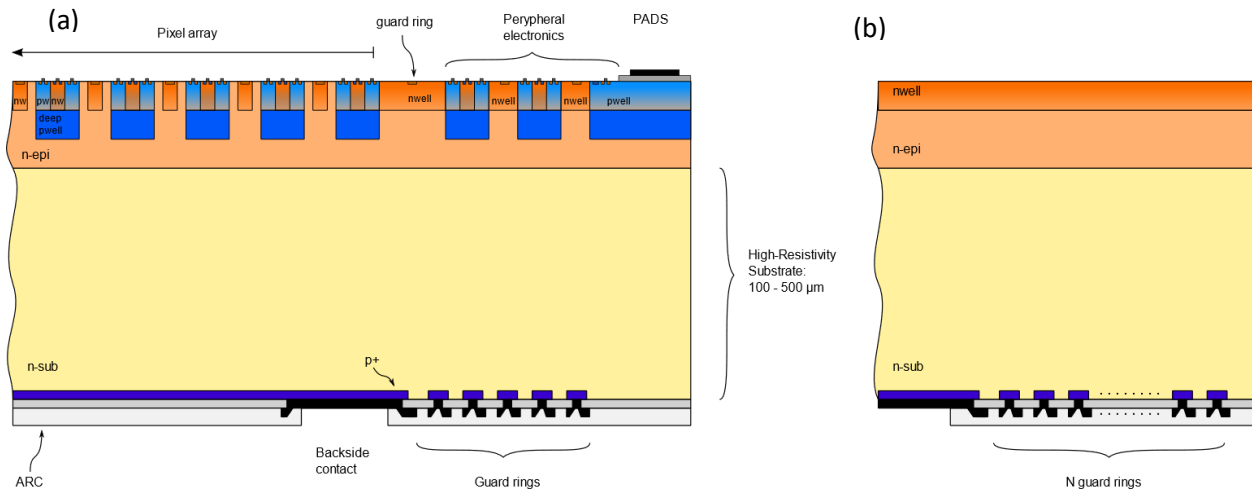


Figure 3. Schematic cross section of pixel array (a) and backside diode test structure (b)

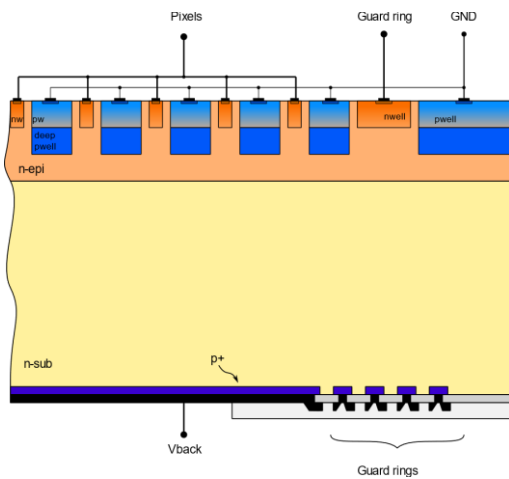


Figure 4. Pixel test structure schematic cross section

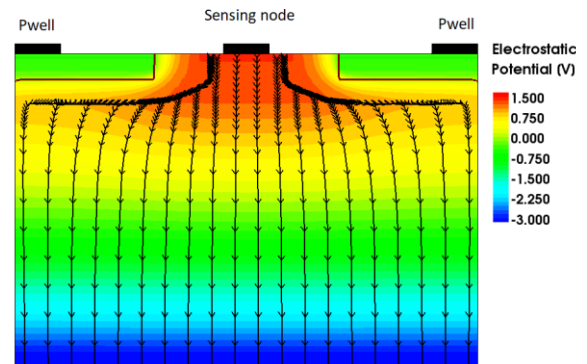


Figure 5. Simulated electrostatic potential and electric field lines in a pixel with 50- μ m pitch. The plotted domain is limited to the surface region.

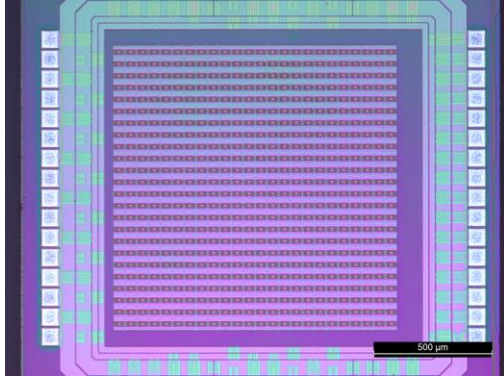


Figure 6. Pixel array micrograph

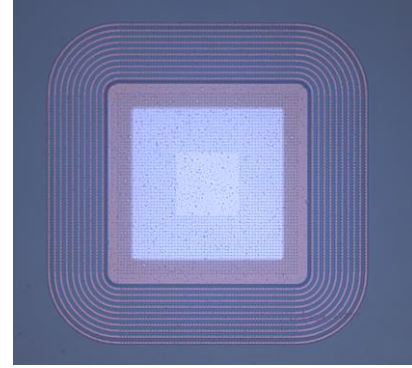


Figure 7. Micrograph of backside diode test structure with 10 guard rings

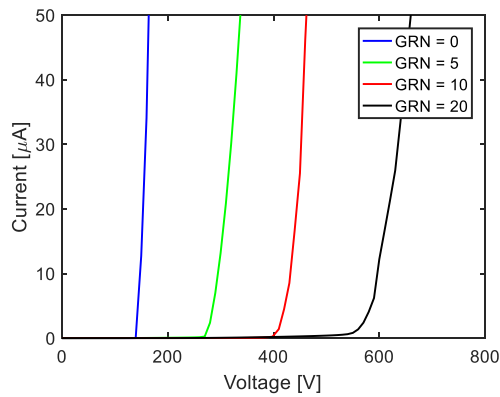


Figure 8. IV curves of backside diode test structures with different number of guard rings (GRN)

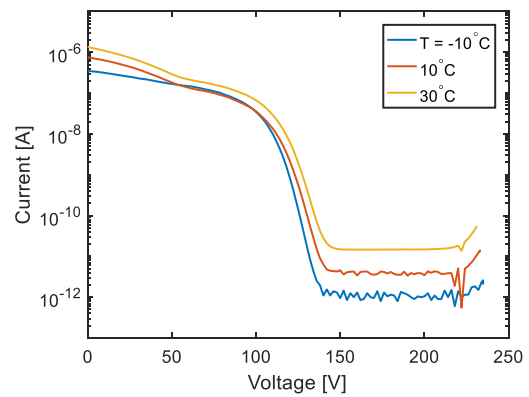


Figure 9. Dark current as a function of bias voltage measured on pixel test structure at 3 different temperatures

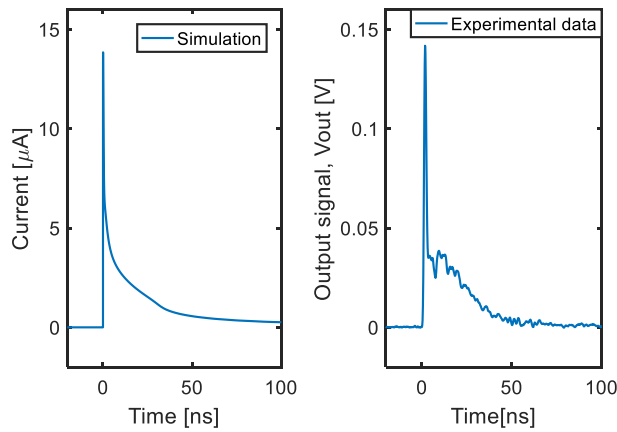


Figure 10. Optical transient response: simulated and measured on pixel test structures with fast pulsed IR laser (FWHM < 100ps, $\lambda = 1064\text{nm}$). In the measurement the test structure was connected to an external 1-GHz amplifier.

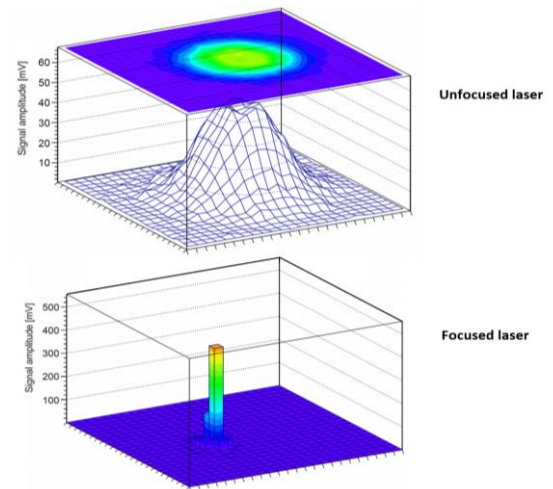


Figure 11. Laser profile measurement on pixel array. Laser wavelength is $\lambda = 1060\text{nm}$, width of the laser spot is $8\text{-}\mu\text{m}$.