Electrostatic surface passivation for p-type BSI Image Sensors

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Abstract

We propose in this paper a surface passivation approach for BSI p-type image sensors. It consists in integrating an oxide-nitride-oxide (ONO) stack on the silicon's back-side surface. Thicknesses of stacked dielectric layers are determined with antireflect consideration. Minimum charge density needed for effective field-effect passivation is evaluated via TCAD simulations. The ONO stack in three different deposition process configurations is measured using Corona Oxidation for Characterization of Semiconductors (COCOS) technique. It is also integrated with arrays of 2µm-pitch pixels on test chips. The measured parameters of COCOS characterization and dark currents of test chips are compared between different configurations. The mean dark current is to 8h+/s in case of effective electrostatic surface passivation. The main population of pixels is at 5h+/s, with smallest tail for the best configuration.

1. Introduction

Thanks to better achievable performances related to light collection, BSI has nowadays been widely adopted in developing high-resolution image sensors. P-type sensors have also been proposed for advantages such as radiation hardness [1]. In such developments, surface passivation is a key issue in order to minimize pixel's dark current. The p-type sensors in our studies have p-type pixel readout chain on silicon frontside surface and CDTI (capacitive deep trench isolation) integrated as pixel sidewalls with active passivation [2]. The p-type photodiode has a hole-collection zone takes almost all the pixel's volume, extending to the silicon backside surface. In such a case, there is remaining backside surface whose passivation should be effective so as to avoid dark current degradation.

We propose here an electrostatic (or field-effect) surface passivation approach with a deposited positively-charged, oxide-nitride-oxide (ONO) stack. It is worth mentioning that oxide-nitride film has been used for passivation mainly in solar cell applications [3]. On the other hand, similar ONO stack has also been suggested for memories for its long charge-retention time [4]. Our propose ONO stack for p-type BSI image sensors is illustrated in Figure 1.

2. Positively-charged ONO stack

The proposed ONO stack has been designed with antireflect optimization for a nearly 100% light transmission ratio at 550nm wavelength (see Figure 2). The thicknesses of the different layers are chosen as follows: 20nm for the first oxide, 60nm for the nitride and 160-170nm for the last oxide.

Sentaurus's electrical simulations have been carried out to evaluate field-induced passivation effect of the charge placed at the oxide-nitride interface. Figure 3 compares 4 various charge quantities: $1e^{11}cm^{-2}$, $5e^{11}cm^{-2}$, $1e^{12}cm^{-2}$ and $2e^{12}cm^{-2}$. From electrostatic potential and electron density at the backside silicon-oxide interface, we can see that passivation is ensured for a charge density more than $5e^{11}cm^{-2}$. This will induce an electron concentration over $1e^{17}cm^{-3}$ with a surface potential pinned to the value imposed by the n-source.

The ONO stack can be fabricated by plasma enhanced chemical vapor deposition (PECVD). Three different processes have been employed to deposite the first oxide layer on the silicon surface to compare their passivation effect. The first two processes are made with TEOS, He and O_2 precursors. Theses two TEOS deposition processes have equivalent TEOS deposition rates with one using a single high frequency plasma power, and the other a double frequency plasma power (high and low frequency power). The third oxide deposition process is made out of SiH_4, N_2 and N_2O. As silane oxide precursor is used, a single high frequency power has been adopted. These three first-layer deposition processes have resulted in three ONO stack configurations, respectively called TEOS_Single, TEOS_Dual and USG.

The second layer of the stack is hydrogenated silicon nitride SiN_x:H. Despite complex mechanisms of hydrogen desorption and passivation, it has been observed that post-deposition annealing of SiN_x:H is necessary in chemical passivation for

reducing dark current [5]. On the other hand, the nitride film is positively charged due to its K centers [3]. The positive charges retained in this layer will play the role of field-effect passivation (Figure 4).

Finally, the last deposited layer is a TEOS oxide film.

3. Characterization Results

3.1. COCOS characterization

COCOS technique has been employed to characterize the deposited dielectric layers on silicon wafers [6]. It allows estimation of density of interface states D_{it}, total charges Q_{tot} in the dielectric layers (including fixed, mobile and trapped charges), flat-band voltage Vfb and contact potential difference Vcpd. It is worth mentioning that, V_{fb} is more sensitive to charges located at silicon-oxide interface (equals to $\varphi_{ms} - \frac{Qtot}{C_{diel}}$ in ideal case of all charges at interface) while V_{cpd} is more sensitive to charges located at the surface ($\varphi_{ms} + V_{sb} + \frac{Qtot}{C_{diel}}$ in ideal case of all charges at surface).

Measurements have been performed on the different oxides splits after deposition and after forming-gas annealing, including splits with oxide and nitride layers'post deposition annealing. Also, for comparison with the three ONO stack configurations, a nitride film directly deposited on silicon and with forming-gas anneal treatment has been measured, and is called "Nitride only".

Figure 5 compares mesured interface state density (D_{it}) representing minimum value of interface states' spectrum in the silicon gap. The D_{it} is above $1e^{12}cm^{-2}.eV^{-1}$ for all the oxides after each deposition. It is decreased by annealing for all splits, but still remains high. In contrast, the decrease is much more significant to be below $1e^{11}cm^{-2}.eV^{-1}$ for oxide-nitride stack. This confirms the effective passivation role of the nitride film by releasing hydrogren it contains when annealing.

Figure 6 shows that Q_{tot} has the same tendency as D_{it} by annealing effect. It decreases from above $1e^{12}cm^{-2}$ after deposition down to $5e^{11}cm^{-2}$ after annealling with nitride. The correlation between D_{it} and Q_{tot} can be explained by the fact that part of Q_{tot} represents interface-trapped charges Q_{it}. The post-annealing charge density Q_{tot} remains high enough for all oxide splits for reaching inversion of carrier population at interface (according to TCAD-simulated results; see Figure 3).

On the other hand, both Vfb and Vcpd (Fig. 6 and 7) remain practically unchanged after annealing for all oxides, meaning that no sensitive redistribution of charges in nitride. However, a closer look at the measured parameters reveals differences between different configurations.

For Nitride-only deposition, D_{it} is 5 times larger than other configurations having oxide deposited on silicon surface. This confirms poor interface quality between silicon and nitride. This Nitride-only deposition also gives higher Q_{tot} than other configurations, with V_{fb} down to -5V in extreme (see Figure 8). As low V_{fb} indicates large Q_{it}, this results from large D_{it} These measurements confirm the need of an oxide film between silicon and nitride for a better interface quality.

Considering TEOS_Dual configuration (Figure 8), Q_{tot} is more dispersive over a wafer; V_{cpd} is off the chart with more than 1V deviation; V_{fb} also has a large dispersion. These results reveal that this configuration of ONO stack is unstable in terms of electrical property. In comparison with TEOS_Single configuration having more reproducible Q_{tot} and V_{fb}, we suggest that the first-layer oxide in TEOS_Dual does not play a good barrier role between silicon and nitride, which may lead to uncontrolled charge distribution in the stack.

3.2. Pixel's dark current

Dark current measurements have been performed at 60°C on test chips integrating matrices of 86x1200 2µm-pitch pixels. Figure 9 plots mean dark current for the three configurations. Splits with TEOS_Single and USG show low and comparable currents around 8h+/s with fair reproducibility. These results are in concordance with COCOS measurements showing low D_{it} and sufficient and stable Q_{tot} for these two configurations. In contrast, TEOS_Dual configurations gives a mean value of about 50h+/s with large dispersion.

Figure 10 shows statistic distribution of pixels' dark currents of a test chip. All the three configurations have their main population at 5h+/s but TEOS_Dual shows a much larger tail distribution. This large tail contribution indicates unsufficient passivation of the back-side interface. In contrast, USG gives best results with smallest tail.

4. Conclusions

Our proposed ONO stack fabricated in different configurations has been evaluated by COCOS and dark current measurements. For configurations ensuring effective field-effect passivation of the back-side silicon surface, the mean dark current is down to 8h+/s. The main population of pixels' dark currents is at 5h+/s, with smallest tail for the best case.

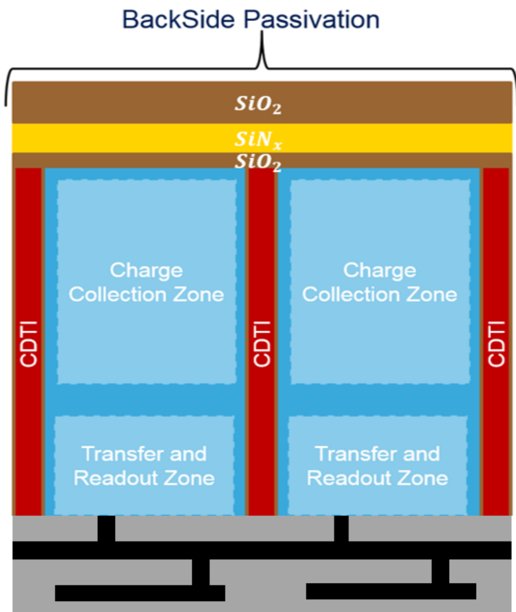

Figure 1: Schematic structure of the BSI pixel with ONO backside passivation

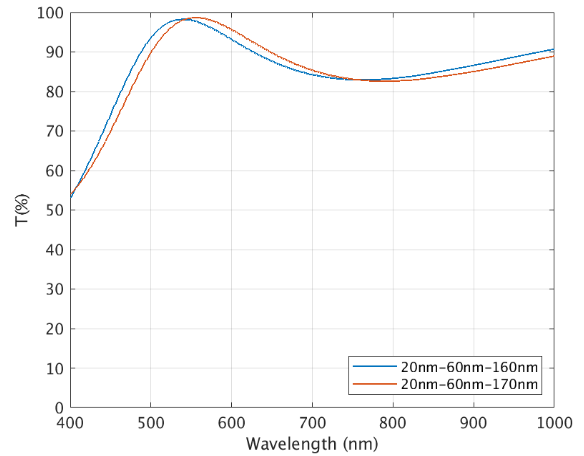

Figure 2: Transmission graph of the ONO stack

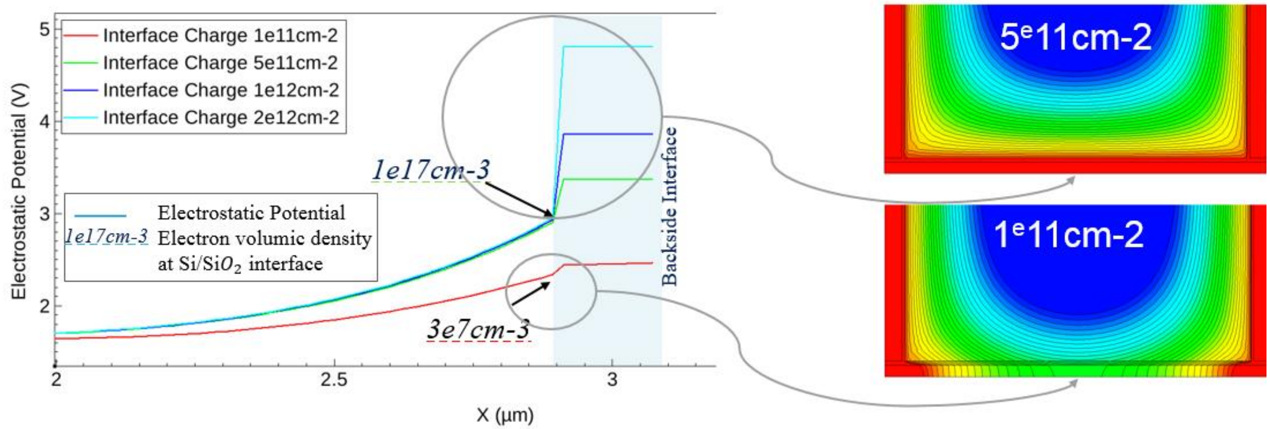

Figure 3: Electrostatic Simulation of backside interface with Electrostatic Potential (left) and the corresponding potential 2D profiles (right)

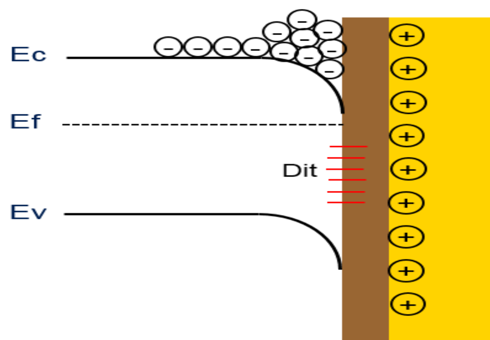

Figure 4: Field-effect passivation mechanism for oxide and positively charged nitride stack

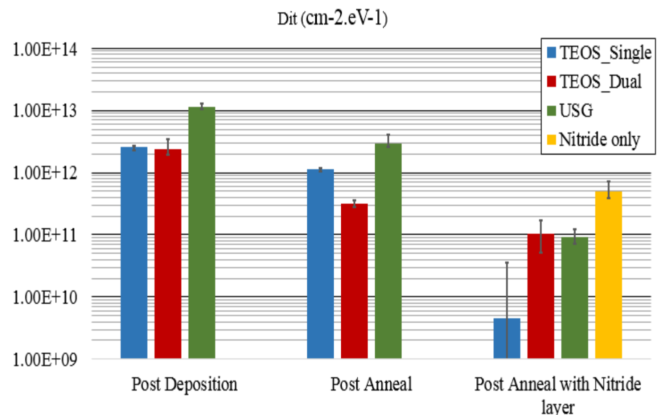

Figure 5: Interface Defects measurement (D_{it}) for the different oxide and nitride splits at different process steps

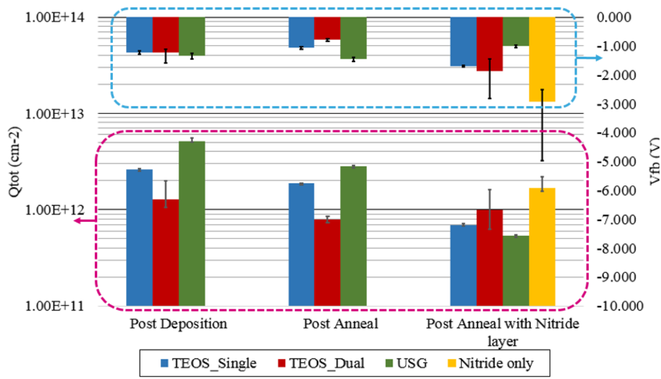

Figure 6: Measurement of Q_{tot} and V_{fb} in dielectrics for oxide and nitride splits

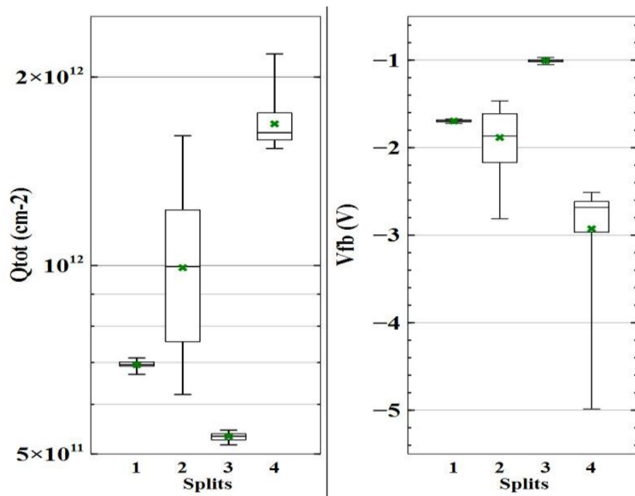

Figure 8 : Zoom over Q_{tot} and V_{fb} for studied splits (TEOS_Single, TEOS_Dual, USG and Nitride only, in this order) post anneal with nitride film

References

[1] B.Mamdy, PhD Thesis, ‘‘Nouvelle architecture de pixel CMOS éclairé par la face arrière, intégrant une photodiode à collection de trous et une chaine de lecture PMOS pour capteurs d'image en environnement ionisant’’, 2016

[2] N.Ahmed, et al.,‘‘MOS Capacitor Deep Trench Isolation for CMOS image sensors’’, IEEE 2014

[3] V.Sharma, PhD Thesis, ‘‘Study of Charges Present in Silicon Nitride Thin Films and Their Effect on Silicon Solar Cell Efficiencies’’, 2013

[4] F.Libscht, M.White, ‘‘Charge transport and storage of low programming voltage SONOS/MONOS memory devices’’, in *Solid-State Electronics*, 1990

[5] D.Benoit, PhD Thesis, “Etude des propriétés du nitrure de silicium PECVD et de sa stabilité thermique. Influence sur les dispositifs de la microélectronique’’, 2006

[6] M.Wilson, et al., ‘‘COCOS (Corona Oxidation for Charaterization of Semiconductors) non contact metrology for gate dielectrics’’, in *American Institute of Physics*, 2006

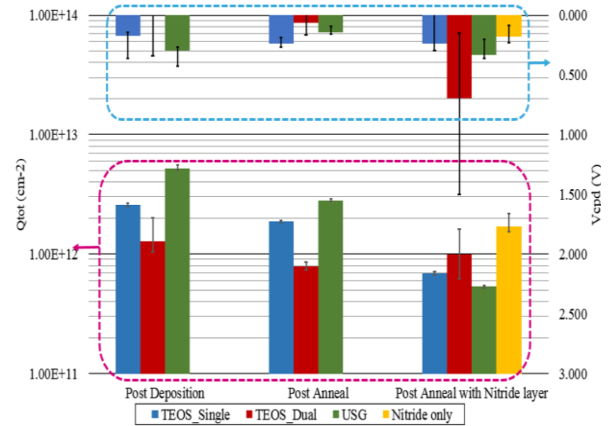

Figure 7: Measurement of Q_{tot} and V_{cpd} in dielectrics for the oxide and nitride splits

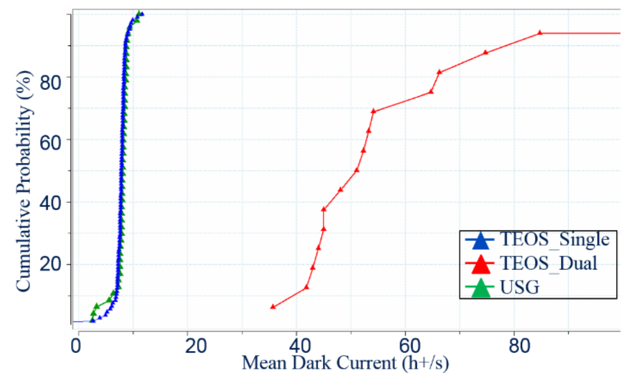

Figure 9: Cumulative graph of mean dark current at 60°C for matrix pixel with ONO stack with splits on first oxide

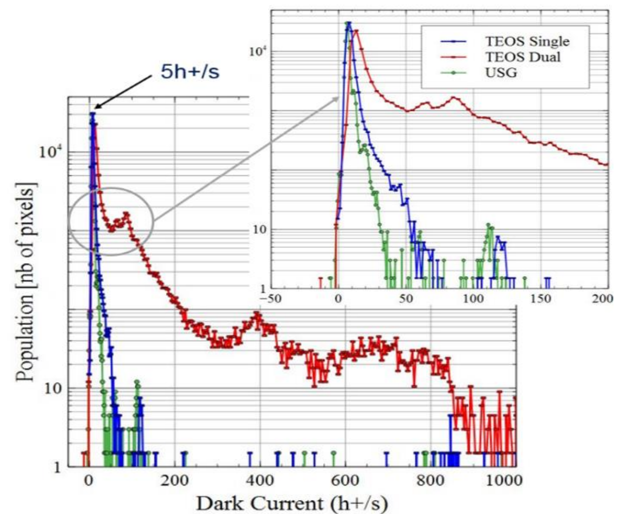

Figure 10: Histogram of the dark current at 60°C and its zoom of the matrix pixels depending on the first oxide