Floating Diffusion Dark Current and Dark Signal Non-Uniformity Reduction for High Dynamic Range Overflow Collection Pixels in High Temperature Applications

M. Guidash[1], M. Oh[1], D. Collins[1], R. Mauritzson[2], D. Tekleab[1], W. Xu[1], S. Nicholes[2]
ON Semiconductor, [1] Santa Clara, CA, [2] Meridian, ID
michael.guidash@onsemi.com

Abstract

Photodiode overflow charge collection (OC) has been utilized to provide high dynamic range (HDR) image sensors for automotive and other applications. The *total SNR* (SNR including dark fixed pattern noise), of these sensors is degraded by floating diffusion (FD) dark current (DC) and dark signal non-uniformity (DSNU). We present work on FD DC and DSNU reduction, to provide required SNR versus signal level for OC pixels at temperatures up to 120°C.

Introduction

Much work has been done and presented on the photodiode (PD) DC and DSNU, directed to low light SNR [1, 4]. For overflow collection OC HDR image sensors, FD DC temporal noise is a key consideration for the low to high light transition region SNR [5]. FD DSNU fixed pattern noise (FPN) is a dominant noise source for OC HDR pixels at high temperatures. We compare FD and PD DC and DSNU for 3 different wafer fabs. We then show results of using TCAD to drive process and layout changes to produce a ~28X reduction in FD DC and DSNU. All data shown is at 80°C and an integration time of 33 msec. DC and DSNU data is normalized to the Fab1 process condition with the maximum junction electric field (Efld).

Initial Data and Analysis

It is well known that PD DSNU is dependent on process contamination and Efld in the PD [1, 4]. FD DC and DSNU is more complicated. With OC HDR pixels, FD DC and DSNU is comprised of multiple regions, some with and without STI, and some with and without a contact. TCAD was used to determine the junction and gate Efld for the PD and FD regions for devices and various initial process conditions from 3 fabs, [2, 3]. The FD DSNU and DC vs. junction Efld is shown in Figure 1. PD DSNU and DC is shown in Figs. 2 and 3 respectively. There is an exponential relationship between DSNU and junction Efld for PD and FD. PD DC is not correlated with junction Efld, but FD DC has an exponential dependence on junction Efld. There is a linear relationship between FD DC and DSNU (Figure 4). For temperatures $\geq$ 80°C the FD DSNU was much larger than the FD DC shot noise, and was the limiting factor for *total SNR* in the transition region. A simple empirical model was determined for FD DC and DSNU as a function of gate and junction Efld based on this data and TCAD Efld results.

New Process Modification Experiments

TCAD was used to determine a first set of process splits (New1) to reduce the FD junction and gate Eflds in 2 fabs. The process variables included LDD and n+ implants, STI depth, STI doping and anneals. These were fabricated and measured. Predicted results for FD DC and DSNU matched the measured data, (Figure 6). This experiment included a contact layout modification. Results indicate there was large FD DC and DSNU component related to contact placement, (Figure 5).

TCAD was next used to determine a second set of process splits (New2) to further lower FD junction and gate Eflds. These results, along with some results from the first set of process splits, and predicted results of the second process splits are shown in Figure 6. The predicted FD DSNU for Fab1 devices measured to date closely match the predicted results. Some of the Fab 1 process splits are still in queue for testing. A 28x reduction from the initial

Fab1 process condition has been demonstrated. FD DC histograms of selected Fab1 process conditions are shown in Figure 7. There is a clear reduction the mode and tail of the histograms as the FD junction Efld is reduced.

The observed results of Fab2 devices are much higher than the predicted values. The process splits included variations for STI sidewall doping. It is suspected that the STI interface state density in Fab2 is much higher than that for Fab1 and with insufficient STI sidewall doping the DSNU floor is dominated by the STI to silicon interface. A readout timing experiment was also used to determine FD DSNU of 2 different FD regions; (1) a minimum geometry active region with a contact and (2) a larger active region, (~2.5x area, ~3x STI periphery, same gate periphery), without a contact. Region 1 had ~4x the DSNU of region 2. This indicates that a second dominant component related to the contact is limiting the DSNU floor.

Conclusions and Further Work

Both FD DSNU and DC were found to have an exponential relationship with FD junction Eflds. By process modifications directed at reducing FD junction and gate Eflds a 28x reduction in FD DSNU at 80°C and 33 msec. integration time was achieved. With this level of FD DC and DSNU a *total SNR* > 25dB in the transition region can be achieved at 100°C, (Figure 8). As the FD junction and gate Eflds are reduced, FD DSNU reduction can be limited by other components (e.g. STI, contact), based on the specific fabrication process details.

References:

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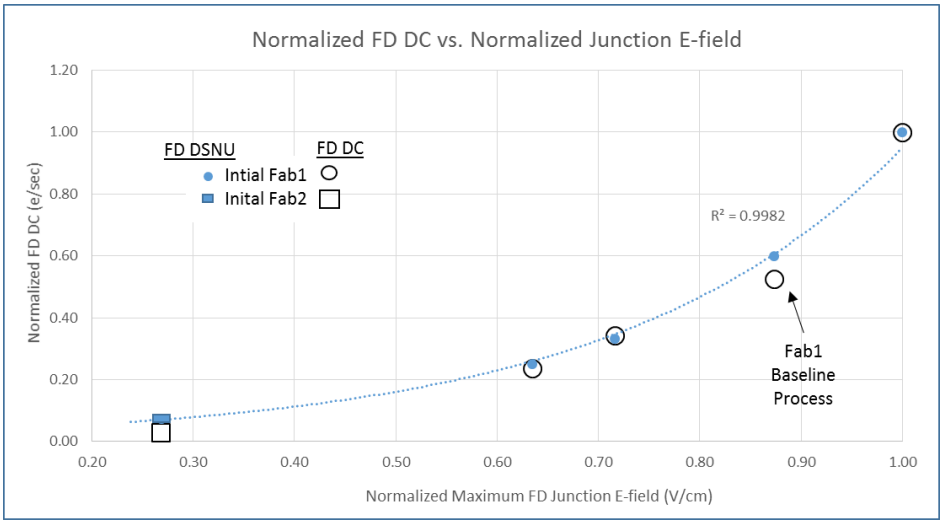

Figure 1: FD DSNU of Initial Processes vs. FD Junction E-Field; Fab1 & 2

FD

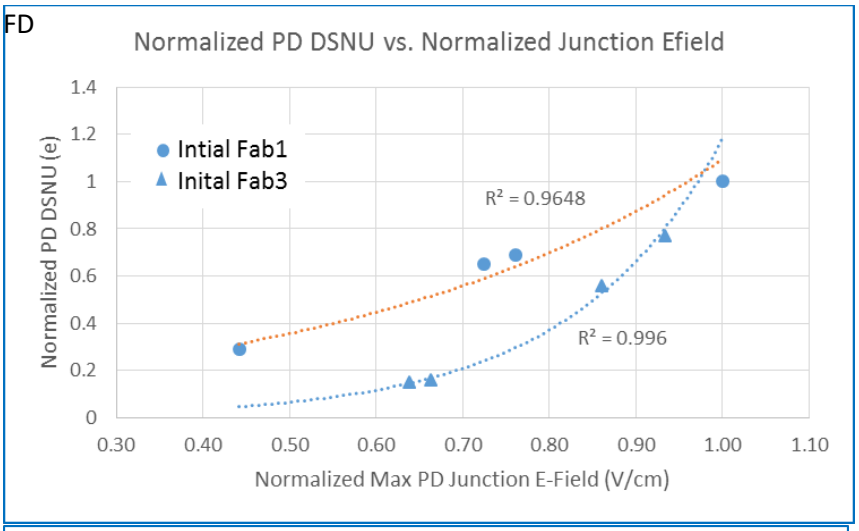

Figure 2:
PD DSNU vs. PD E-Field
Fab 1 & 3

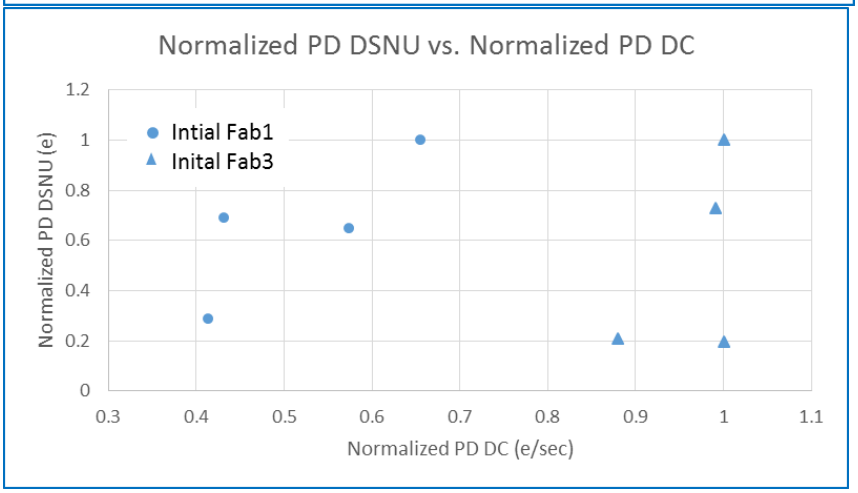

Figure 3:
PD DC vs. PD DC
Fab1 & 3

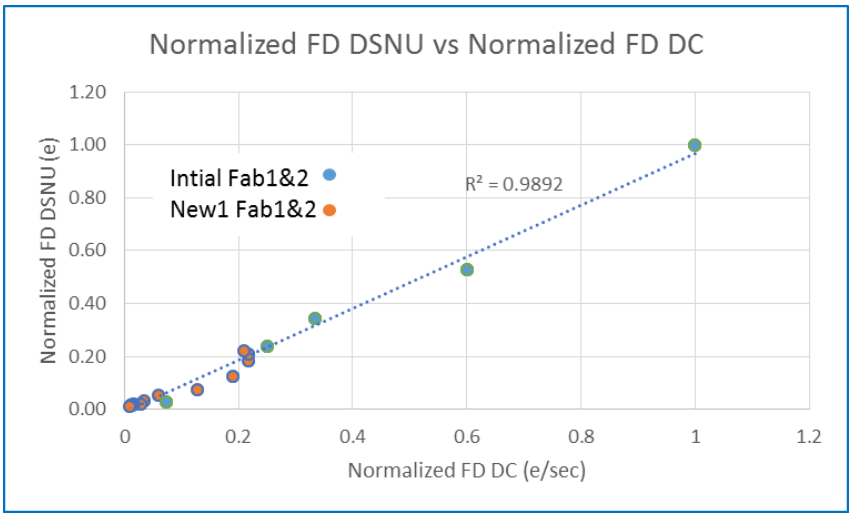

Figure 4:
FD DC vs. FD DSNU
(Fab1 & 2)
Both initial processes and new processes

$$total\ SNR = 20log_{10}\frac{Signal}{\sqrt{TN^2 + FPN^2}}$$

Figure 8:
total SNR includes FD DSNU

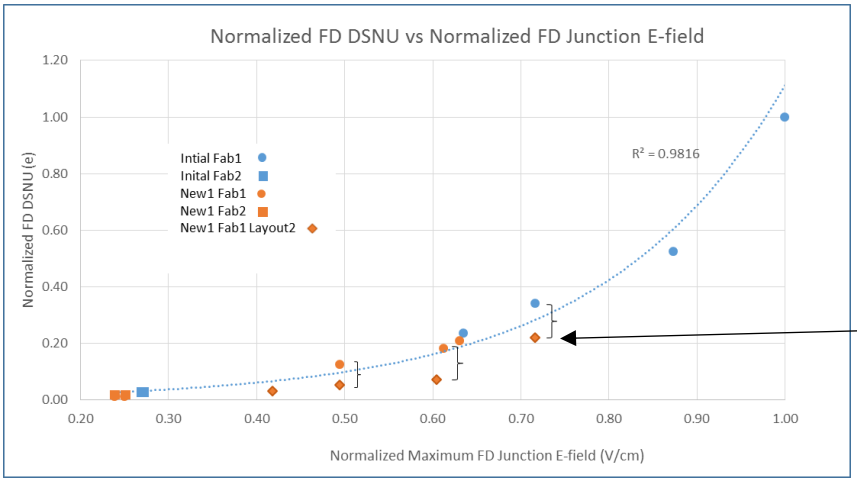

Figure 5:
FD DSNU vs. FD Junction E-Field for new process conditions and new layout

Reduction in DSNU at same junction E-Field due to contact layout

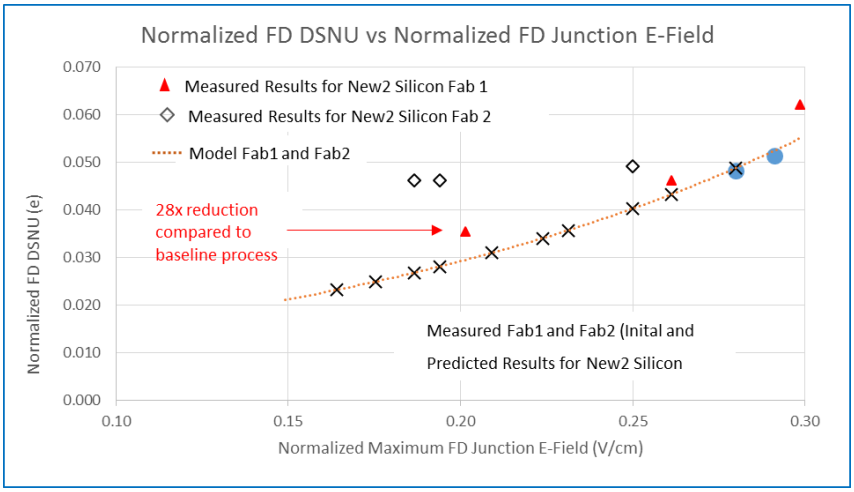

Figure 6:
New Process Conditions FD DC & FD DSNU (measured vs modeled)

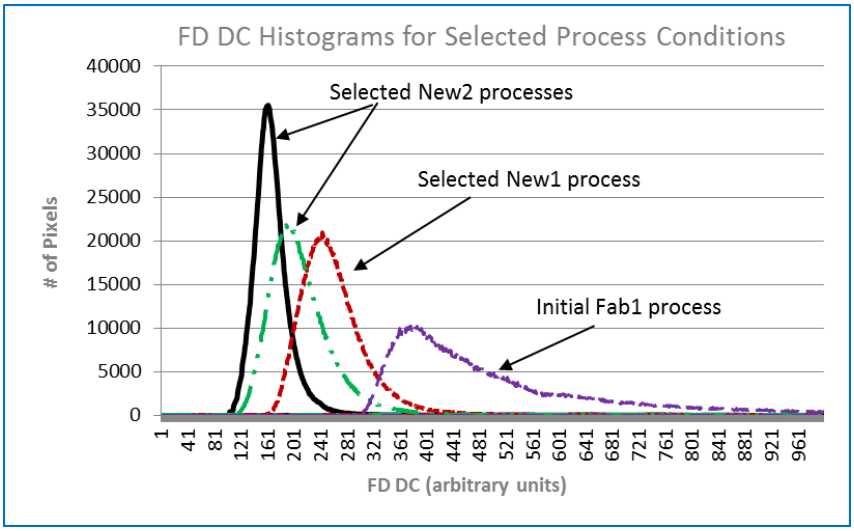

Figure 7:
FD DC Histograms