CMOS Single-photon Avalanche Diodes using Gated Reset Circuit with On-chip Pulse Width Modulation

Chun-Chang Hsu*, Chia-Ming Tsai, and Sheng-Di Lin

Institute of Electronics, National Chiao Tung University, 1001 University Road, Hsinchu 300, Taiwan
**Corresponding Author: qwefghuiopjj@gmail.com, telephone: +886-3-5712121#54240*

Abstract

We demonstrate a gated reset circuit with integrated pulse width modulation for CMOS single-photon avalanche diodes. The simple design extends the dynamic range and achieve a maximum count rate of 153 MHz. Afterpulsing effect and ranging test using gated reset method is performed and exhibit its advantage over conventional active or passive reset scheme.

1. Introduce

CMOS single-photon avalanche diodes (SPADs) play a key role in various applications, such as light detection and ranging (LiDAR) for autonomous driving [1], fluorescence lifetime imaging microscopy [2], time-gated Raman spectroscopy [3], due to its high sensitivity and excellent timing precision. SPAD's Geiger-mode operation enables single-photon sensitivity but acquires quenching and reset circuit so unwanted detection deadtime is introduced. This becomes a serious issue when strong background light, for example, sunshine in vehicle LiDAR application, makes SAPDs too busy to detect laser photons.

2. Gated Reset Circuit

Passive quenching and reset circuit using a single MOS transistor is the simplest way but the deadtime is long (>10-20 ns) due to large resistance during recharging SPAD. To make it shorter without going into complex active-reset circuit, very recently, Antolovic et. al. [4] demonstrated that a clock-driven scheme could largely extend the dynamic range although the maximum count rate for single SPAD is only about 10 MHz. **Fig. 1** explains the basic working principle of clock-driven reset using the same passive reset circuit. Different from the operation of conventional passive-quenching-passive-reset using constant gate voltage, clock-driven or gated reset scheme does quenching at low gate voltages and recharging at high ones, as shown in the simulated timing diagram in **Fig. 2**. To enhance the stability and to control the period and duration of the clock-driven gate voltage, in this work, a pulse width modulation circuit is integrated on the same chip, as shown in **Fig. 3**, which can be shared with other SPADs in array applications.

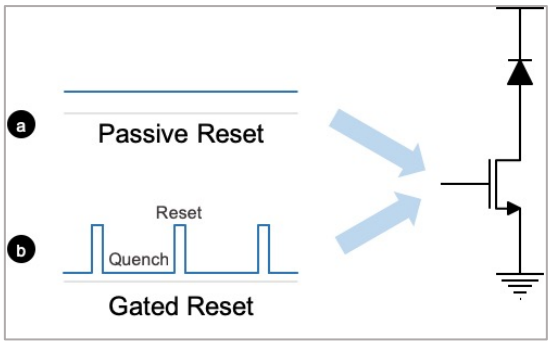

Fig. 1 Passive rest and gated reset schematic.

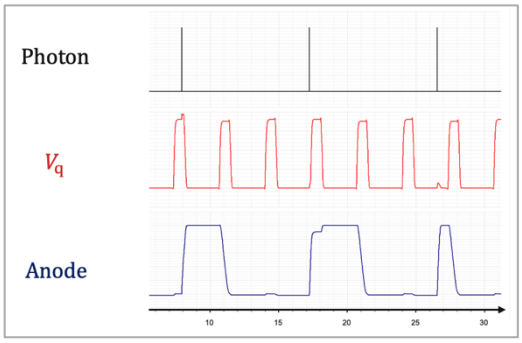

Fig. 2 Timing waveform using gated reset method.

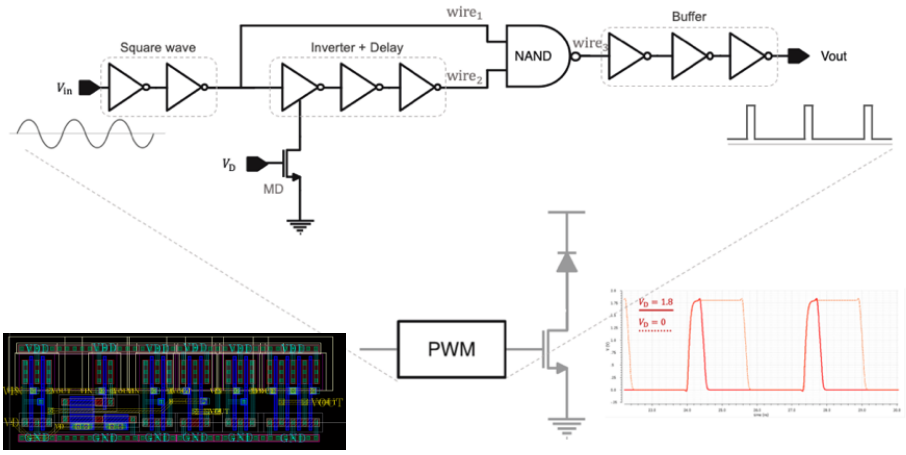

Fig. 3 Gated reset scheme with an integrated pulse width modulation design and layout.

3. SPAD Device

Based on the same device reported previously [5], we use a 20-μm-diameter SPAD in this work. The device structure is shown in **Fig. 4**. The P-N junction is formed by DPW and NBL layers with HVPW layer as a guard ring. We have designed and fabricated the chips using TSMC high-voltage 0.18-μm CMOS technology without any customization. The breakdown voltage of our SPAD is 48.5V. We operate the SPAD at the excess bias is 2.5V. The corresponding dark count rate (DCR) is 276Hz. The measured spectra of photon detection probability (PDP) at various excess bias voltages are shown in **Fig. 5**. The maximum PDP is 21.4% at 550 nm at the excess bias of 2.5 V.

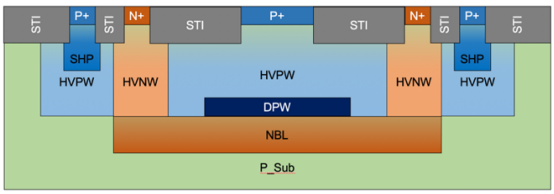

Fig. 4 Schematic device structure of our SPAD

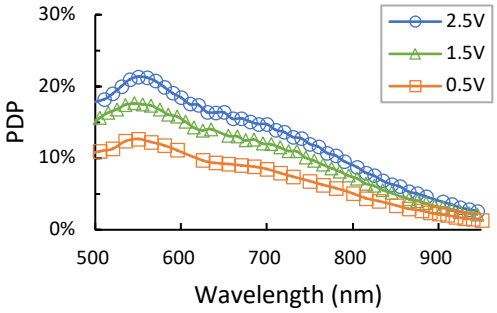

Fig. 5 Photon detection probability (PDP) of our SPAD at different excess bias

4. Dynamic Range

Fig. 6 exhibits the dynamic range experiment setup. Using integrator sphere with a 625-nm light-emitting diodes as light source, a calibrated photodiode (PD) and the SPAD chip were mounted on the two holes on the sphere. The effective input counts, denoted as n, can be calculated by the measured photocurrent of calibrated PD and the photon detection probability (PDP) of SPAD. That is, $n =$ photon flux on SPAD sensing area times PDP. The detector count, denoted as m, is the actual output counts from SPAD. **Fig. 7** exhibits the measurement results of dynamic range of the SPAD under gated reset and passive reset operations. In passive reset scheme, where the conventional constant gate voltage was used, the highest count rate of 39.8 MHz was obtained at quenching bias of 0.91 V. In contrast, in gated reset operation (350-MHz clock frequency, 0.6-ns pulse width, gate voltages of 0 V and 1.8 V), the linear region is largely extended and the dynamic range has been significantly increased to a maximum count rate of 153 MHz, about 4-fold enhancement.

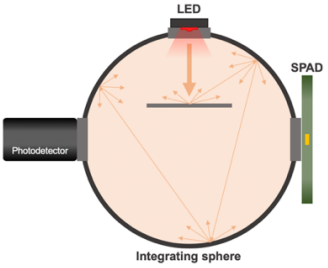

Fig. 6 Dynamic ranges experiment setup

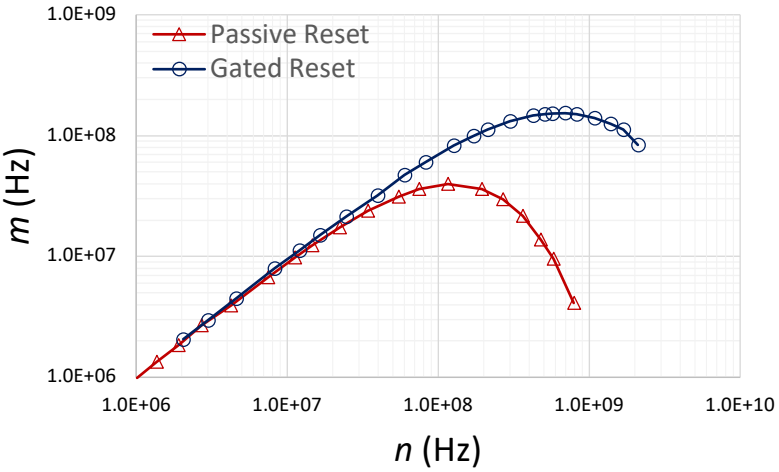

Fig. 7 Measured dynamic ranges of passive reset and gated reset methods.

5. Afterpulsing Probability

For SPADs, afterpulsing probability (APP) increases with shorten deadtime and increased breakdown current. [6] For gated reset scheme, if a breakdown event occurs during reset period, the breakdown current cannot be quenched immediately so the resultant APP gets worse. The measured APP as a function of the pulse width is plotted in **Fig. 8**. The clock frequency is fixed at 350 MHz. By reducing the pulse width to 0.6 ns, 3-fold reduction of APP is obtained. **Fig. 9** exhibits the measured APP as a function of the clock frequency with fixed pulse width of 0.6ns. Clearly, the APP increases with the increasing clock frequency because occurrence probability of the shorter deadtime is higher.

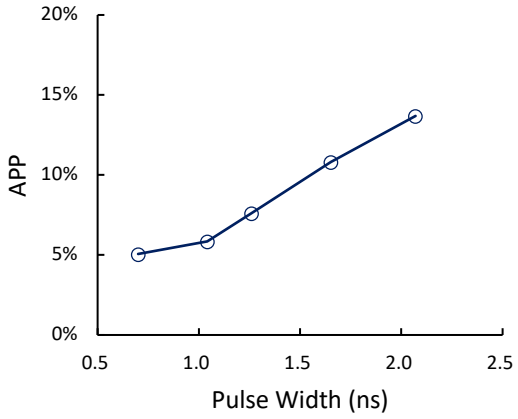

Fig. 8 Measured APP as a function of pulse width.

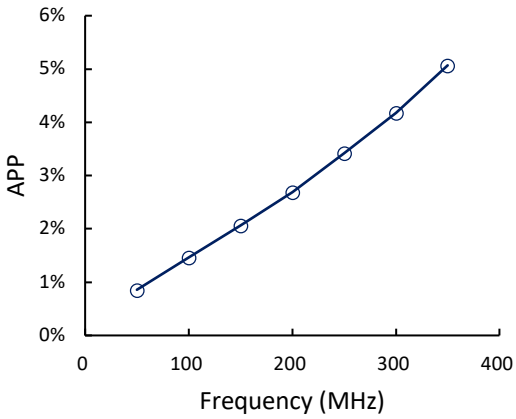

Fig. 9 Measured APP as a function of the clock frequency.

6. Ranging Experiment

An intriguing feature using gated reset scheme is its varying deadtimes. This is potentially helpful in LiDAR application. We have performed a ranging experiment using active-reset [7] and gated reset schemes with the respective APP of 4.8% and 5.0%. The laser condition for ranging is, repetition rate of 2.5 MHz, wavelength of 780

nm, pulse width of 70 ps, and enough laser power to trigger SPAD for each pulse. The arrival time is recorded by the time-correlated single-photon counting (TCSPC) card with time bin resolution of 250 ps. The integration time is 5s. The obtained histograms are illustrated in Fig. 10. Due to the fixed deadtime in the active reset method, the periodic subsequent peaks arising from APP observed clearly. These counts could cause incorrect judgment of multiple echoes. In contrast, by using gated reset scheme, the APP peaks are rounded and the peak value is significantly reduced.

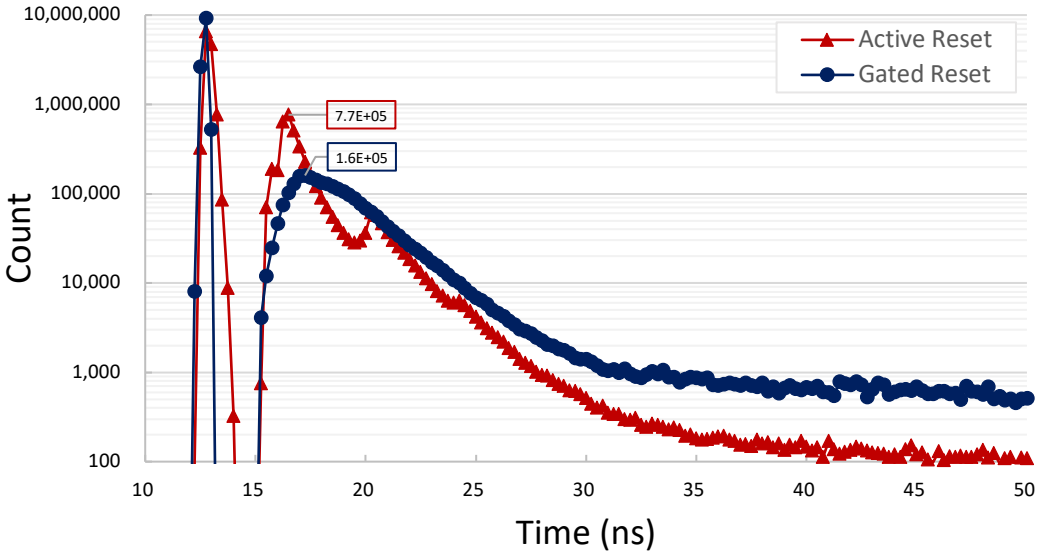

Fig. 10 Ranging histogram of gated reset and active reset.

7. Conclusion

In this work, the gated reset scheme using simple passive reset and pulse width modulation circuit is proposed and demonstrated. The dynamic range has been largely extended. APP is reduced with shortened pulse width. Due to its varying deadtimes, the APP peaks in ranging histogram are rounded and weakened so can avoid mistaken detection in LiDAR application.

Acknowledgement: We thank the financial support from MOST in Taiwan. We are grateful to the National Center for High-performance Computing for computer time and facilities and ITRI for their help on chip fabrication.

References

[1] Takai, H. Matsubara, M. Soga, M. Ohta, M. Ogawa, and T. Yamashita, "Single-photon avalanche diode with enhanced NIR-sensitivity for automotive LIDAR systems," Sensors, vol. 16, no. 4, p. 459, Mar. 2016.

[2] L. Pancheri, N. Massari, and D. Stoppa, "SPAD image sensor with analog counting pixel for time-resolved fluorescence detection," IEEE Trans. Electron Devices, vol. 60, no. 10, pp. 3442–3449, Oct. 2013.

[3] J. Kostamovaara et al., "Fluorescence suppression in Raman spectroscopy using a time-gated CMOS SPAD," Opt. Exp., vol. 21, no. 5, pp. 31632–31645, Dec. 2013.

[4] I. M. Antolovic, C. Bruschini, and E. Charbon, "Dynamic range extension for photon counting arrays," Opt. Express, vol. 26, no. 17, pp. 22234–22248, 2018.

[5] L. D. Huang et al., "Single-photon avalanche diodes in 0.18-μm highvoltage CMOS technology," Opt. Exp., vol. 25, no. 12, pp. 13333–13339, 2017.

[6] M. W. Fishburn, "Fundamentals of CMOS single-photon avalanche diodes," Ph.D. dissertation, Dept. Elect. Eng., Math., Comput. Sci., TU Delft, Delft, The Netherlands, 2012

[7] W. S. Huang *et. al.* Solid-State Dev. Mater., Japan (2017).