A Low Noise Single-Slope ADC with Signal-Dependent Multiple Sampling Technique

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Abstract

A low noise single-slope analog-to-digital converter (SS-ADC) is presented employing a signal-dependent multiple sampling scheme for low-light imaging and high-accuracy ranging. The SS-ADC adopts multiple ramps to convert the signal of a pixel several times to average out random noise of readout circuits, improving a signal-to-noise ratio without any penalty on a readout time. The prototype SS-ADC fabricated in standard 0.11 μm CIS process with an indirect time-of-flight pixel array improves a depth accuracy up to about 40% at a long distance.

I. Introduction

Temporal random noise (RN) suppression in CMOS image sensors (CIS) is crucial for improving the image quality in a low light condition where photon shot noise is not dominant. A correlated multiple sampling (CMS) technique has been introduced to average the RN out of the signal but takes a long time to read pixel data out as the number of samples is increased [1]. This demerit is critically shown with a single-slope analog-to-digital converter (SS-ADC), degrading a frame rate. To address this issue, multiple sampling techniques with the SS-ADC having modified ramp slopes have been reported for mitigating RN while keeping the frame rate [2–4]. One method, a pseudo-multiple sampling, changes the resolution of the ADC by a factor of the number of samples, making a steeper slope than that of a normal ramp signal. Since no additional hardware is required, it is an effective solution to high-resolution CIS with a small column pitch, but the quantization noise level limits RN suppression. The other techniques utilize small-range multiple ramp signals relying on the light intensity. The multiple sampling in a single frame is not necessary for imaging in a high light condition because it cannot reduce photon shot noise. Therefore, they focus on mitigating RN from readout circuits such as a source follower and an ADC, and column-parallel SS-ADCs generate or select adaptive ramp signals, achieving 0.66e- rms noise.

This paper also presents the SS-ADC with a signal-dependent multiple sampling for low-noise imaging applications. One of four ramp signals with the same slope and different durations is chosen depending on a signal level, converting it to a digital value in several times. Simple digital logic for ramp selection is implemented to the proposed ADC, and it also provides the ramp information together with the converted digital value. The proposed ADC is incorporated with a time-of-flight (TOF) pixel, improving the depth accuracy by reducing RN.

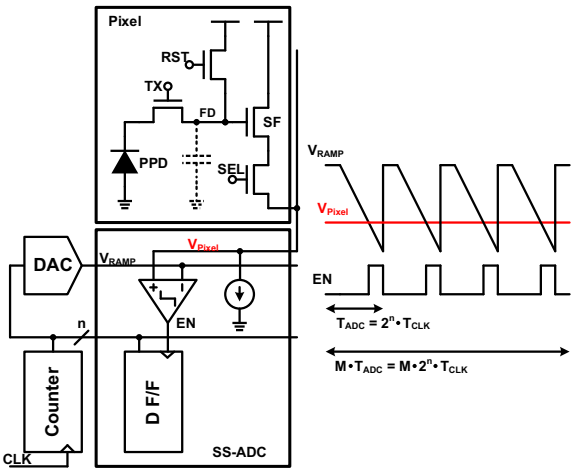

Fig. 1. Block and timing diagrams of conventional SS-ADC with multiple sampling

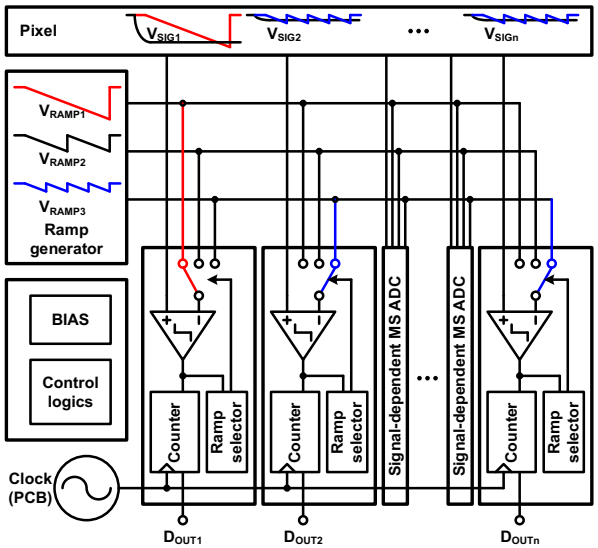

Fig. 2. Overall architecture of proposed SS-ADC with signal-dependent multiple sampling

II. Proposed Signal-Dependent Multiple Sampling

Fig. 1 shows the block and timing diagrams of the conventional SS-ADC in a single column of CIS. It consists of a comparator and an n-bit flip-flop as a memory. A digital-to-analog converter (DAC) shared with all SS-ADCs generates a ramp signal to compare with an analog value of a pixel, and a counter provides digital data to the memory accordingly. This simple architecture makes it suitable to the area-efficient column-parallel ADC at the expense of long conversion time proportional to 2^n in n-bit case. The penalty on the conversion time becomes severe when the multiple sampling is applied.

Paying attention to the conversion time of the SS-ADC, which is linearly proportional to the light intensity, we devise a multi-ramp SS-ADC in that each pixel chooses its ramp signal according to its analog output as shown in Fig. 2. Multiple ramp signals with identical slope and various durations are provided and shared to the column-parallel SS-ADCs. One ramp is the same as the conventional ramp signal while the others would be reset in the middle of the conversion time and go downward again. A ramp selector in each column controls the connection of the ramp signals to a corresponding SS-ADC depending on the pixel output level.

Fig. 3 shows the simplified timing diagram of the operation with four ramp signals. There are mainly two phases, a ramp selection phase and a conversion phase. In the first phase, all SS-ADCs compare pixel outputs with V_{RAMP1} that is the typical ramp signal represented by a blue dot line in Fig. 3. Once comparators are toggled before resetting the shortest ramp signal, V_{RAMP4}, which implies the light intensity is dark in the pixels, the SS-ADCs with them change the ramp from V_{RAMP1} to V_{RAMP4} to activate the multiple sampling. After resetting V_{RAMP4}, their operating phase moves to the second while the others stuck to the V_{RAMP1} are still in the first phase plotted with gray background in Fig. 3. Like the SS-ADC with dark pixels (V_4 in Fig. 3), some SS-ADCs with the pixel signals of V_2 and V_3 select their ramp signals of V_{RAMP2} and V_{RAMP3}, respectively in the following selection phases and change the ramp accordingly. The remained SS-ADCs connected to the pixels with bright light convert the signals compared with V_{RAMP1}. Since the duration of the next ramp signal is doubled from the previous one, the number of the multiple samplings would be half of that of the previous conversion. Considering no conversion in the reset selection phase, the number of the multiple samplings, M_k, is given by

$$M_k = 2^n / 2^{(n-k)} - 1 = 2^k - 1 \qquad (1)$$

where n is the resolution of the SS-ADC and k is the index of the ramp signals. The conversion time in the SS-ADC with the k-th ramp is given by

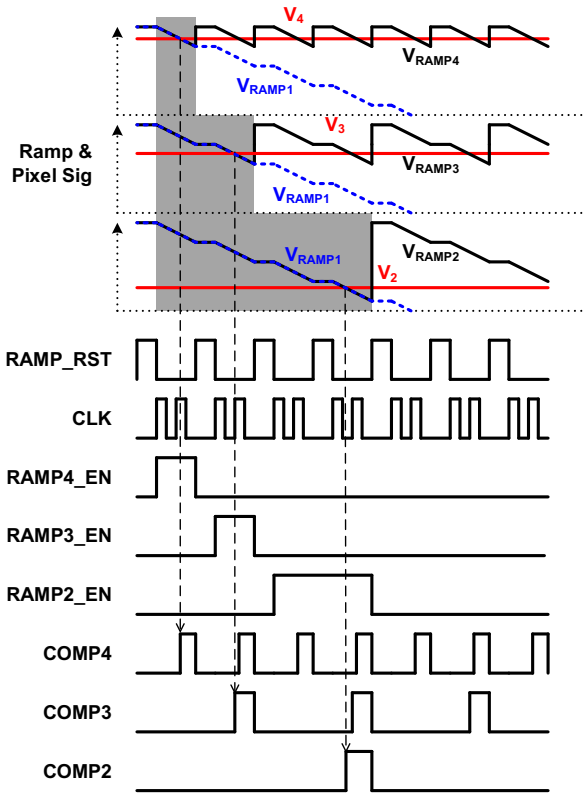

Fig. 3. Simplified timing diagram of the proposed SS-ADC (Signal duration is not properly scaled.)

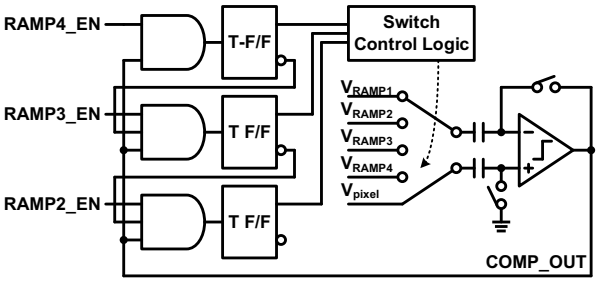

Fig. 4. Schematic of the ramp selector in the SS-ADC

$$T_{ADCk} = T_{clk} \times (M_k + 1) \times 2^{(n-k)} = T_{clk} \times 2^n. \qquad (2)$$

Consequently, the proposed SS-ADC can offer weighted suppression of RN with minimal degradation of the frame rate due to the reset period of the ramp signals. Furthermore, the compensation between the number of samples and the converting range forbids the counter overflow. We employed 10 and 4 as n and k, respectively in this work. The darkest pixel is converted 15 times whereas the brightest one is done once.

The ramp selector is implemented with simple digital circuits as shown in Fig. 4. All toggle flip-flops (T-F/Fs) are reset to low initially. The outputs of the T-FFs go to high only when an enable signal (RAMP_EN) and the comparator output are high, which indicates the SS-

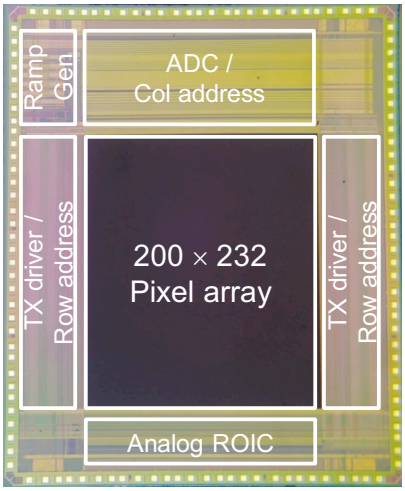

Fig. 5 Die photograph

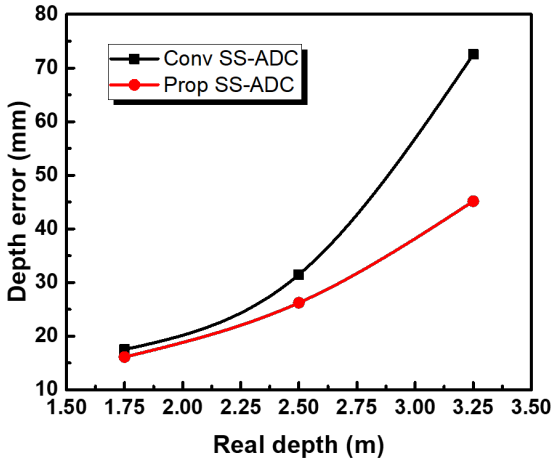

Fig. 6 Measured depth error with conventional and proposed SS-ADC operations

ADCs find their target ramp signals. The inverted output of the T-FF prevents the following T-FF from being toggled in the next ramp selection phase.

III. Measurement Results

The prototype CIS with the proposed signal-dependent SS-ADC was fabricated using 0.11-µm CIS process. Fig. 5 shows a die microphotograph of the chip. The size of the proposed SS-ADC is 7.2 µm × 800 µm, which is slightly larger than the conventional one due to the ramp selector. A 200 × 232 indirect time-of-flight (I-ToF) pixel array is integrated with it. The I-ToF pixel with 14.4 µm pitch based on a pinned-photodiode (PPD) employs the split and binning structure of our previous work [5].

To verify RN reduction using the multiple sampling, we measured a depth error of the prototype chip. The depth error is one of the most ciritical parameters in the performance of I-ToF pixels and deteriorated by RN of the readout channel in long distances where photon shot noise is not dominant [6]. Fig. 6 shows the measured depth error with and without activating the signal-dependent multiple sampling scheme. The improvement of the depth error is clearly observed as the distance increases. Limited optical power and short integration time prevent the sensor from extending the distance, but it should be enough to evaluate the proposed scheme. The multiple sampling in both signal and reset values reduces the depth error by 38% at the maximum range of 3.25 m, while only 6% improvement is achieved at a short distance where photon shot noise would be more significant than RN of the circuitry.

IV. Conclusion

In this paper, the signal-dependent multiple sampling scheme is presented to suppress RN effectively. The proposed column-parallel SS-ADCs incorporate four ramps with the same slope and different durations, enabling to control their signal-dependent number of conversion times simultaneously. The prototype chip with the I-ToF pixel successfully mitigates RN and improves the depth error by 38% at the maximum range.

Acknowledgement

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