P23

Optimization of fully-depleted gated PPD pixel for achieving high-speed charge transfer

Yun-Tzu Chang[1,2], Pierre Boulenc[2], Linkun Wu[2], Maarten Rosmeulen[2], Pol Van Dorpe[1,2], Chris Van Hoof[1,2], Andreas Süss[2, 3]

[1] KU Leuven, ESAT, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium
[2] Imec, Kapeldreef 75, B-3001 Leuven, Belgium
[3] now at OmniVision Technologies, Santa Clara CA 95054, USA

[1] Corresponding author phone: +32(0) 16 28 36 04, E-mail: yun.tzu.chang@imec.be

***Abstract* – A design of experiments (DOE) technique using Taguchi's orthogonal arrays is successfully applied to a gated PPD pixel design with different pixel sizes for optimizing the charge transfer speed. A 15 µm pixel achieving 2.5 ns, and a 5 µm pixel achieving 1 ns in collecting 90% of carriers from the backside to the storage node with a fully-depleted epi-layer of 30 µm are presented. An initial evaluation of a test vehicle employing 5 µm pixels is also given.**

Introduction

Because of high sensitivity, fast photocarrier transport and CMOS process compatibility, fully-depleted CMOS image sensors are attractive for various advanced applications such as ultra-high-speed imaging [1-3], time-of-flight [4], and direct X-ray detection [5].

This work presents a fully-depleted gated Pinned-Photo-Diode (PPD) pixel based on the technology described in [3]. A dedicated P-well biased at ground potential insulates in-pixel circuitry against the substrate. The doping profile of the P-well is crucial for fast photo carrier transport [1]. In order to obtain optimum speed, the doping profile, doping position, transfer gate length and gate position are studied with TCAD simulation using a design of experiments (DOE) technique. Taguchi's orthogonal arrays [6] are applied to reduce the required DOE TCAD runs.

Parameters and Optimization

In this paper the vertical and lateral transport of gated PPD pixels are studied separately for 15 µm pixel and then extended to 5 µm pixel. The design parameters considered in each DOE are listed in Fig. 1. The model for vertical transport

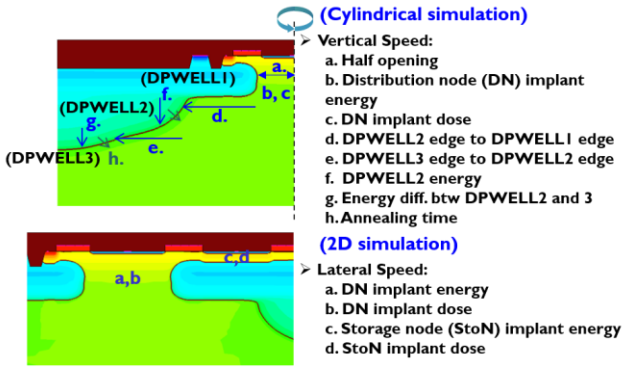

Figure 1. Design parameter lists for vertical and lateral transport TCAD DOE.

exploits cylindrical symmetry around the Z axis at the center of the distribution node (DN) to weight the electron density for different distances from the center. The lateral transport model is a standard 2D simulation. A short light-pulse (90 ps at 550 nm wavelength) is used to stimulate the pixel in either case. The performance criterion used in this study is the time needed to collect 90% of the carriers in the storage node (StoN).

Simulation Results of DOE

A. 15 µm pixel optimization

From the results of the vertical and lateral transport DOE, the optimum value of each design parameter can be obtained by calculating the mean value of the related response characteristic in the Taguchi design [6]. Fig. 2 shows the DOE results with the P-well half opening of 1.4 µm. 1.7 µm P-well half opening (not shown here) exhibits the same trend as 1.4 µm, meaning monotonous trends remain monotonous for the considered parameter range and optima such as for DPWELL2 to DPWELL3 distance did not

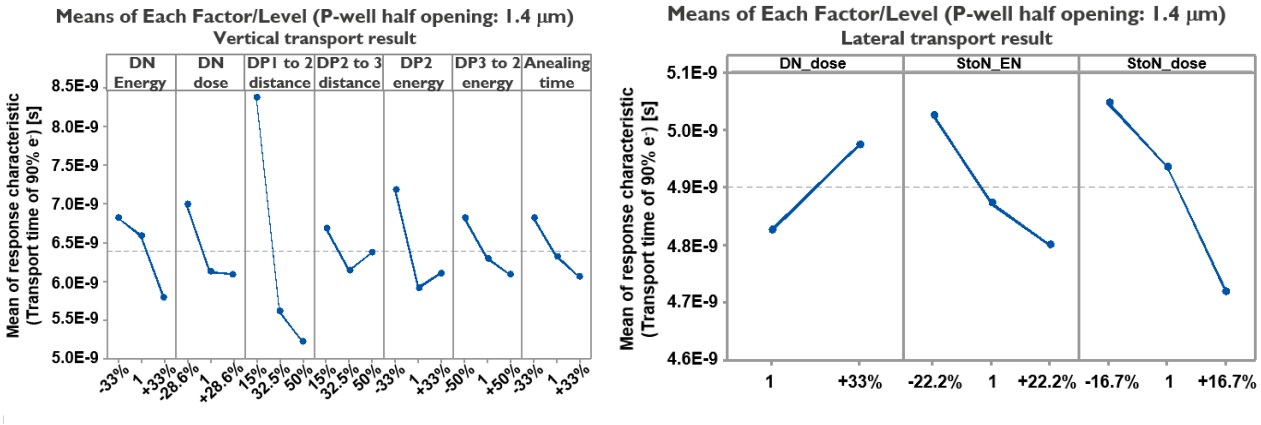

Figure 2. Results of vertical and lateral transport DOE with 1.4 µm P-well half opening. (Pixel size: 15 µm, DN implantation energy: +33% in lateral DOE)

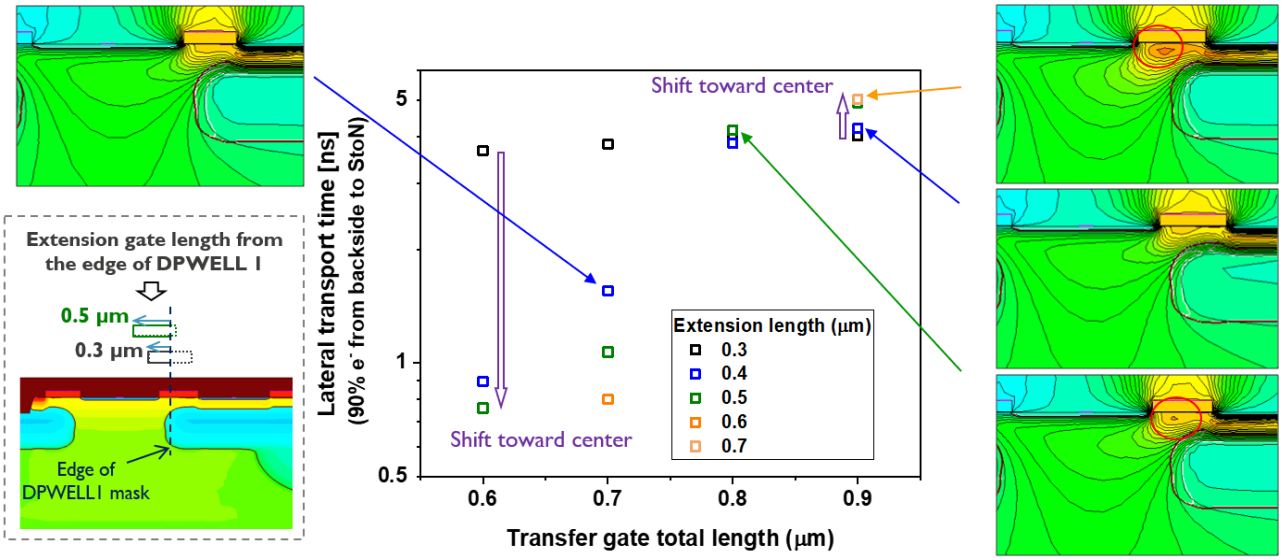

Figure 3. Electron transport time of different transfer gate lengths and positions with optimum doping conditions (P-well half opening: 1.4 µm)

change when varying the half opening from 1.4 µm to 1.7 µm. However, DN implantation dose condition shows reverse trend in vertical and lateral transport simulations. Therefore, both the vertical and lateral optimum combinations are considered, and optimization is done in order to reduce the dominating transfer bottleneck.

Optimizations of the transfer gate size and location were performed after doping conditions have been fixed (Fig. 3). As shown in Fig. 3, the formation of a potential pocket can be avoided when the transfer gate length is smaller than 0.8 µm. Moreover, the electron lateral transport time can be smaller than 1 ns by shifting the gate towards the center, yielding a more monotonous potential profile underneath the transfer gate.

Fig. 4 shows vertical and lateral transport time versus half opening size and transfer gate size and position. These plots are given for optimum DN implantation dose. It is indicated that 2.5 ns transport time is possible for a 15 µm gated PPD image sensor. Note that the optimum DN implantation dose is different for different gate lengths, since a potential pocket may be formed underneath the transfer gate for non-optimal DN implant dose.

B. 5 µm pixel optimization

DOE of transfer gate layout and implant condition was applied in order to design a 5 µm pixel with optimum photocarrier transport speed.

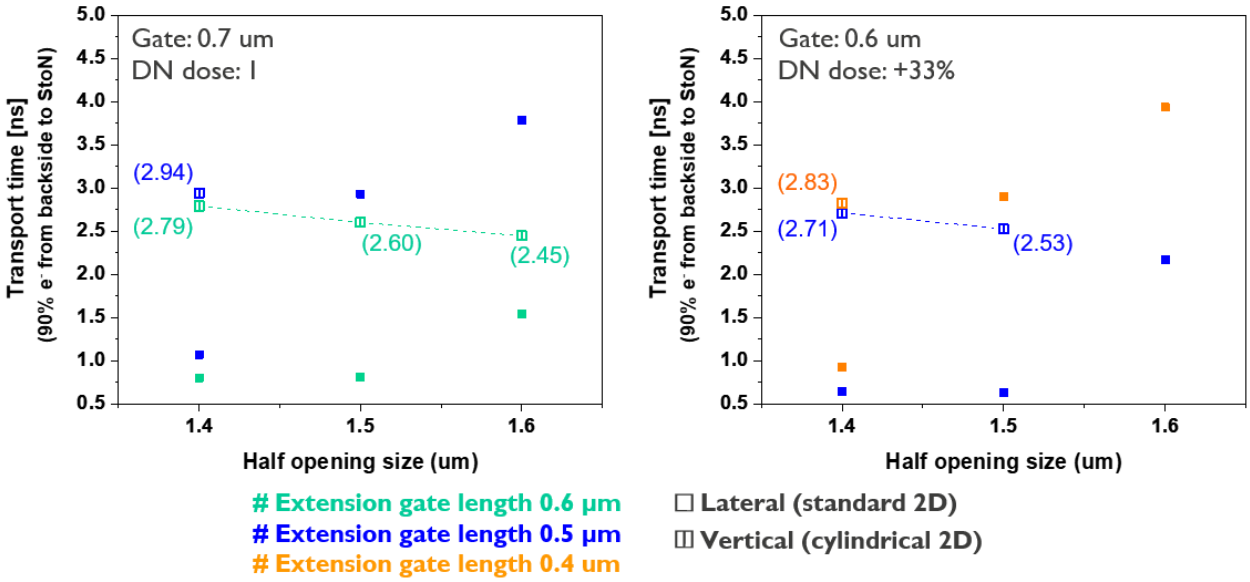

Figure 4. Vertical and lateral results of 15 µm pixel with different gate length and position.

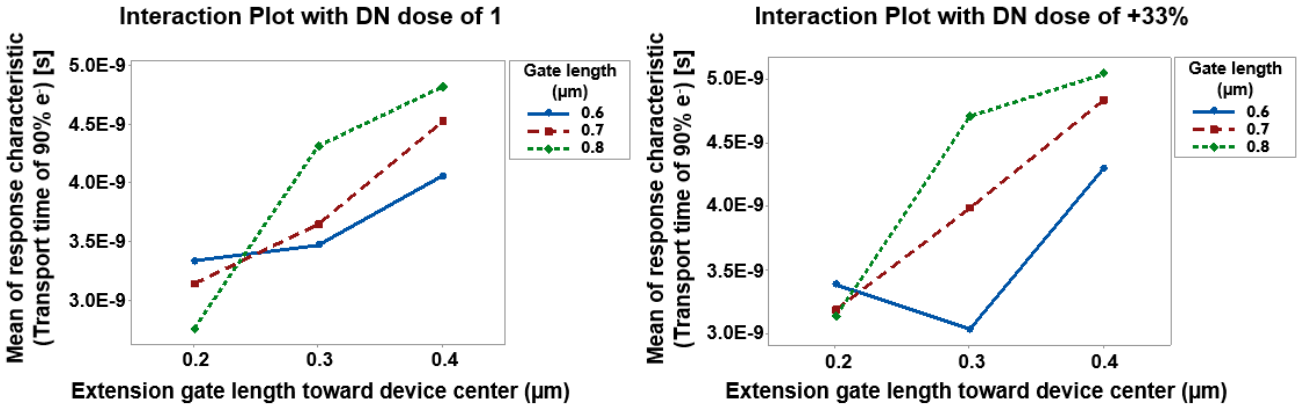

Figure 5. DOE interaction plots of 5 µm pixel lateral transfer with different DN implantation doses.

In the vertical transport DOE of the 5 µm pixel, DN dose shows the same trend as the 15 µm one. The optimum DPWELL2 to DPWELL3 edge distance was increased. The optimum DPWELL2 energy, DPWELL3 to DPWELL2 energy difference and the annealing time were decreased compared to 15 µm. Fig. 5 presents the interaction plots between total gate length and the extension gate length of the lateral DOE results with two different DN implant doses. It indicates that 0.8 µm gate length with 0.2 µm extension and 0.6 µm gate length with 0.3 µm extension are the optimum gate conditions for DN dose of 1 and +33%, respectively. After optimizing the storage node doping conditions, the best combination yielded optimal lateral transfer speed of 0.24 ns and was further simulated in 3D TCAD to yield an accurate performance estimate. Here 0.5 ns and 1 ns transfer time were needed in order to collect 90% of the generated carriers at -18V and -10V back bias, respectively. At these bias conditions hole injection currents from the P-well to back bias in the order of 1.8 µA and 0.27 µA were observed which are still tolerable for high resolution imagers.

Device Evaluation

A test vehicle with 5 µm pitch gated PPD pixels has been fabricated, and the photon transfer curves have been measured at room temperature as shown in Fig. 6. A conversion gain of 58 µV/e^-, a storage node full well capacity of about 10000 electrons, and 12 e^- read noise are extracted. The shutter efficiency, QE and electron

transport will be characterized when the currently ongoing BSI processing is finalized.

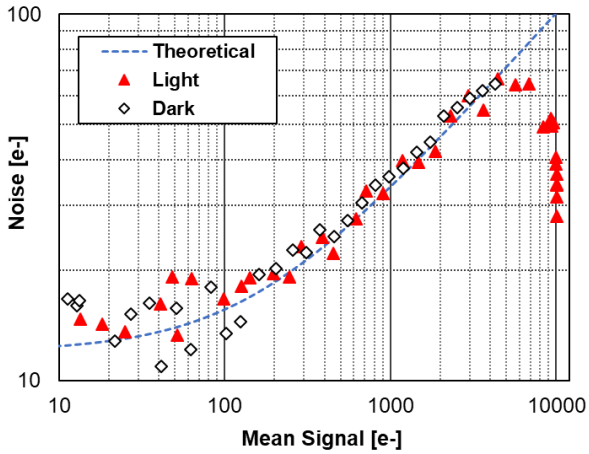

Figure 6. Photon transfer curves measured on 5 µm pitch gated pixels.

Conclusion

The DOE presented in this study can be applied to different pixel sizes. A 15 µm and a 5 µm pixel were designed with DOE. The 5 µm pixel has been verified with 3D TCAD simulation. It was shown that 90% of electrons can be collected in 1 ns at -10V back bias. By adjusting the dedicated P-well profiles, both the electron transport speed and the required minimum back bias can be optimized.

In contrast to CCD pixels [1], the optimized gated PPD pixel requires lower voltage levels while being CMOS compatible. All periphery was monolithically integrated on-chip. Table 1 compares expected performance for the reported 15 µm and 5 µm gated pixels to state of the art literature.

References

[1] V. T. S. Dao et al., "Toward 10 Gfps: Factors Limiting the Frame Rate of the BSI MCG Image Sensor," IISW 2015, June 2015.

[2] T. Resetar et al., "Development of Gated Pinned Avalanche Photodiode Pixels for High-Speed Low-Light Imaging," Sensors 2016, 16, 1294, Aug. 2016.

[3] A. Süss et al., "A Fully Depleted 52 µm GS CIS Pixel with 6 ns Charge Transfer, 7 e-rms Read Noise, 80 µV/e- CG and >80 % VIS-QE," IISW 2017, June 2017.

[4] A. Payne et al., "A 512x424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130 MHz and 2GS/s ADC," ISSCC 2014, pp. 134-136, Feb. 2014.

[5] S. Shrestha et al., "A Silicon-on-Insulator-Based Dual-Gain Charge-Sensitive Pixel Detector for Low-Noise X-ray Imaging for Future Astronomical Satellite Missions," Sensors 2018, 18, 1789, June 2018.

[6] G. Taguchi et al., "Taguchi methods: orthogonal arrays and linear graphs - tools for quality engineering", American Supplier Institute, 1987.

Parameter	Microsoft [4]	Shizuoka Univ. [5]	Ritsumeikan Univ. et al. [1]	IMEC [3]	This study (TCAD simulation)	
Technology	0.13 µm CIS	0.2 µm SOI-CIS	CCD	0.13 µm CIS	0.13 µm CIS	
Pixel Pitch	10 µm	36 x 18 µm^2	~10.6 µm	52 µm	15 µm	5 µm
GS	yes	n.a	yes	yes	yes	yes
Read noise	12.3 e-	n.a	n.a.	7 e-	n.a	12 e-
speed	130 MHz	n.a	~ 1ns	typ. 6 ns (TCAD)	~2.5 ns (quasi-3D TCAD)	1 ns (3D TCAD)
Back bias	n.a.	-30V	~-30V	-21V	-15V	-10V
epi	n.a.	200 µm	30 µm	30 µm	30 µm	30 µm

Table 1. Comparison of the state-of-the-art fully-depleted image sensors