Large Format Global Shutter CMOS Image Sensors

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This paper describes a large format sensor technology with a 3.2um storage gate pixel supporting charge based CDS operation. The CMOS image sensor platform, designed in a 130nm process, can support up to 45 Megapixels and has a line time of 3.56us. This allows capturing UHD-4K at 120fps (2160p) and UHD 8K video at 60fps (4320p) at a low power of <1W and <2W respectively.

Until recently, [1, 2] had been reporting the highest resolution global shutter CMOS sensors. Since 2017 [3, 4], higher resolution global shutter imagers have been published. This paper brings a capability to achieve higher resolution than [1, 2, 3] and achieve a similar resolution as [4] in a smaller optical format (no stitching).

The design has a column parallel 12-bit split-reference SAR A/D converter performing analog and digital CDS, keeping the unity gain noise at <5e- at full speed over a >10ke- FWC. The split-reference allows to optimize the capacitor array by leveraging centrally calibrated reference voltages. In order to ensure exact matching between top and bottom references, which needs to be even more accurate as mismatch would cause odd-even patterns, a mixed signal calibration scheme was introduced that refreshes on every line time.

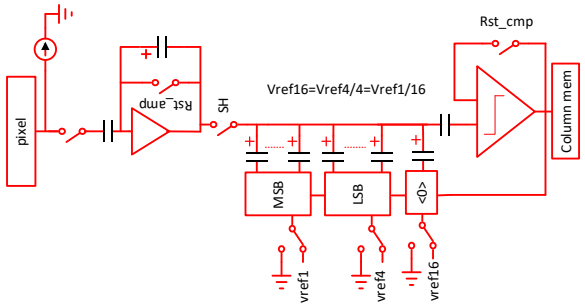

Figure 1: Split-Reference SAR ADC

When running at half rate, the sensor allows to capture two signals from each pixel and from the same integration period so as to achieve a ~7dB DR improvement. For this, each pixel is read twice, once using a high gain in the column, once using a low gain setting. For every pixel, both values are recombined off-chip as shown in Figure 2.

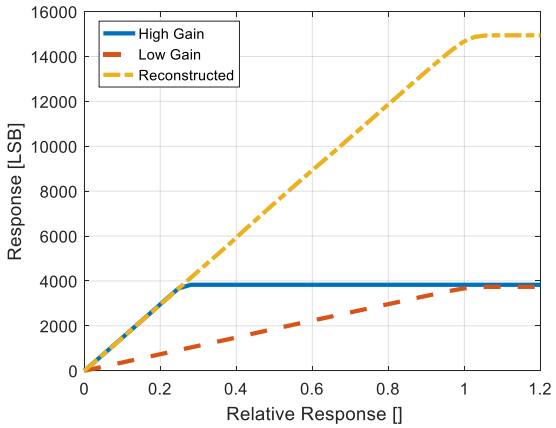

Figure 2: Dual Gain Reconstruction

The reconstruction either outputs only the high gain signal well before the high gain signal saturated, or a scaled version of the low gain signal after the high gain signal saturates. In a small transition region, the weights of these two signals are gradually changed for 0 to 1 and vice versa, so as to obtain a smooth transition. The resulting image has a <2e- noise floor over a 10ke- FWC.

In order to enable multiple applications running at varying speeds, a 'rush-to-idle' approach was implemented to optimize the power consumption. This involves the sensor finishing up its line operations in the minimally achievable time (3.56 µs) regardless of the frame and line rate required by the application, and subsequently powering down any blocks that no longer need to operate.

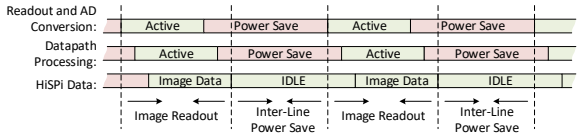

Figure 3: Power Save Methodology

In order to minimize the aggregate data rate in these operating modes, at reduced line rates, the number of SLVS lanes can be progressively reduced to ¾, ½ or ¼ of the original lane count. This technique is preferred over optimizing bias currents for specific line rates which would be less effective and risks affecting the analog behaviour of the critical circuits.

The combination of techniques applied results in a 2160p120 capture at <1W and 4320p60 at less than 2W.

Despite the high speed operation and large optical format, the structured noise is kept substantially below the temporal noise floor, thereby offering highly uniform images without the need for external corrections. This is made possible by a distributed architecture.

Up to 4096 columns, a traditional readout structure is maintained, but at higher column counts, a redistribution layer is added in between two nuclei allowing to keep the performance trade-offs, IR drops and RC delays to remain the same as in the original design, while doubling the number of columns that can be supported. This is shown in Figure 4.

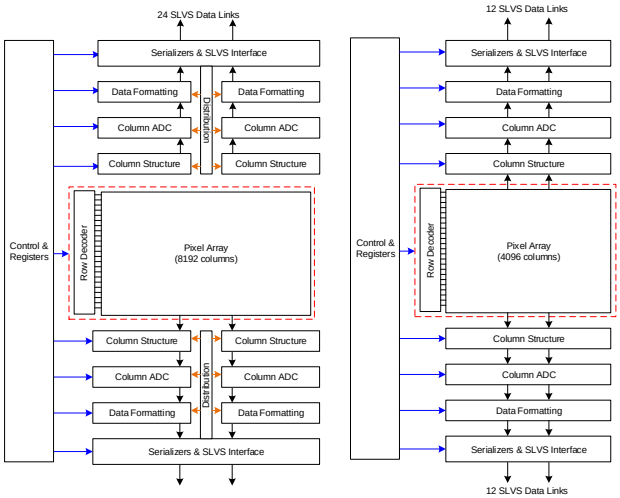

Figure 4: Architectural Block Diagram for 8192 & 4096 columns

The centre portion repeats common structures such as bias generators, reference buffers and control signals as well as power distribution. On the higher resolution sensor, in order to overcome RC delays on the horizontal control lines, all of the pixel control signals are repeated on both left and right side of the array. This reduces the settling time by 4x compared to a scenario with single-sided drive capability only and as such makes up for the longer wire length.

All power management for the pixel array is integrated on-chip by means of positive and negative charge pumps for control signals outside the power rails. All timing for the sensor is provided by a configurable sequencer that supports various advanced trigger and shutter modes and up to 64 independent ROI. Different integration time per ROI can be supported for a better setup of the scene in factory automation or inspection applications. The data is transmitted off-chip through up to 48 SLVS lanes @ >700Mbps each.

The pixel is a 2x1 shared Storage Gate Pixel as shown in Figure 5. The storage gate enables global charge storage, which allows to achieve a 1.9e- noise floor and has a dark current as low as 20e-/s, while achieving a >13ke- storage capacity. The optical stack consists of an optical structure to maximally guide the light towards the photodiode and a tungsten light shield protects the storage gate. This leads to a GSE of >4000:1. The GSE angular response in the horizontal direction is similar to [6], but in the vertical direction has been maintained quite well. (Figure 6)

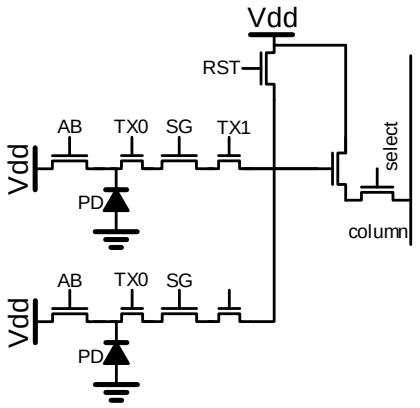

Figure 5: 2x1 shared Storage Gate Pixel

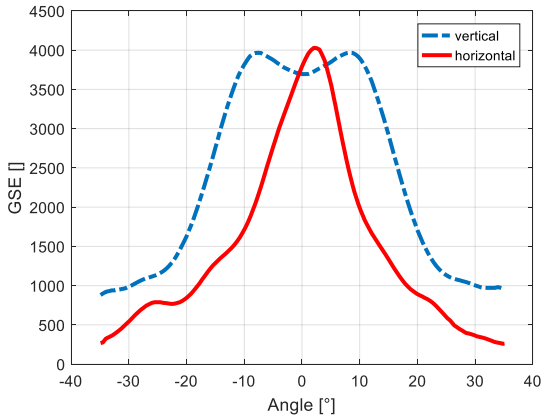

Figure 6: GSE angular response

A 5, 12, 16 and 45 Megapixel sensor have been demonstrated on this scalable platform, with 16 lanes on a 2560x2048 resolution, 24 lanes supporting a 4096x3072, 4096x4096 resolution as

well as a 48 lane sensor with 8192x5460 resolution. Due to the increased column loading, the 5460 rows sensor has a line time limited by the array up to 3.77us, still enabling 60fps@4320p.

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Table 1: key specifications

Parameter	Value	Remark
Pixel size	3.2 x 3.2 µm^2	
Pixel array	2048 - 8192	columns
Pixel type	Storage Gate	
Frame Rate	90fps@12M 120fps@2160p 60fps@4320p	- UHD-1 UHD-2
Power Consumption	<1W <2W	12M@90fps UHD2@60fps
Line Time	3.56/3.77µs	(longer LT for higher row counts)
Power Supplies	3, 2.8, 1.2 V	
QE	>65%	peak
Dark Current	80&20e-/s	PD & SG @60C
Full Well Charge	10 ke$^-$	
Temporal noise	<5 e-, <2e-	@ unity gain, high gain
DR	67dB (74dB)	Increased DR @ half rate
ADC	12-bit	Split-Ref SAR

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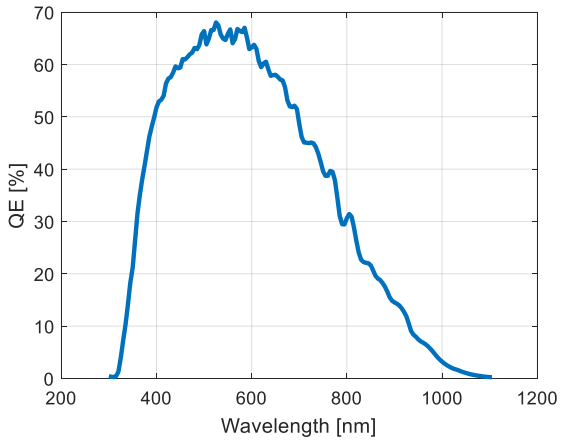

Figure 7: QE for 3.2µm Pixel

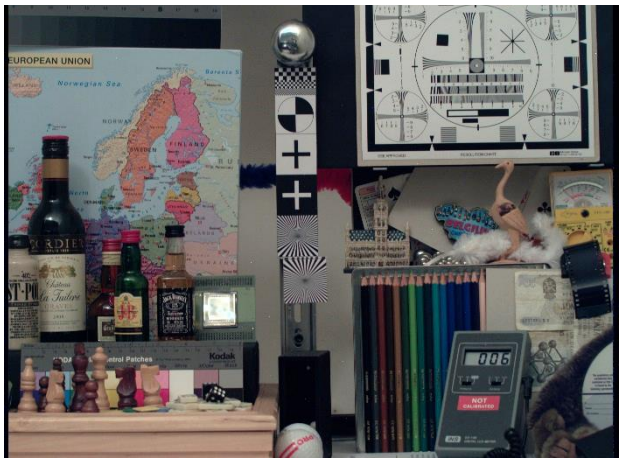

Figure 8: 12 Megapixel Color Image

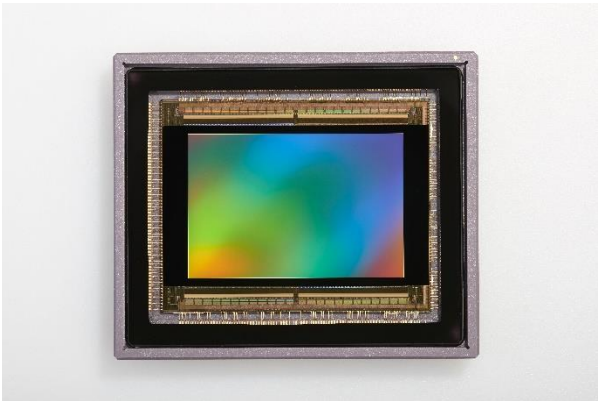

Figure 9: 45 Megapixel Image Sensor