Leakage Current Non-Uniformity and Random Telegraph Signal in CMOS Image Sensor Floating Diffusions used for In-Pixel Charge Storage

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I. Introduction

TRENDS in imaging manufacturing over the last decade was an accelerated rate for integration by seeking a reduction of pixel pitch, an increase in pixel resolution, and an increase in pixel performances. Nowadays, as the successor to charge-coupled devices (CCD), CMOS image sensors (CIS) comprise an array of active pixels. High-end consumer grade CIS are four-transistor (4T) pinned photodiode (PPD) structure. 4T pixels include a photosensitive region (pinned photodiode), a charge transfer transistor, a sense node, a reset transistor, a source follower transistor for in-pixel amplification, and a column bus transistor. Essentially, generated charges are collected and converted to the voltage domain within each pixel, and ultimately read out. To enable both still and motion photography, in-pixel charge storage in Sense Node (SN) Floating Diffusions (FD) is considered in global shutter and burst CIS. Before being converted to the voltage domain, the charge retention time in the FD varies depending on the pixel position in the sensor array. Typically, the longer retention time corresponds to the array readout time. Consequently, the performances of high-resolution CIS, implying a long readout time, using in-pixel charge storage in FD are closely related to mechanisms occurring in the FD as it plays a major role in the detection chain. As the FD leakage current is more influent when long storage times are concerned, the signal of the last pixels can be drastically impacted. The required long storage time in FD make high-resolution CIS very sensitive to FD leakage current and FD leakage current Random Telegraph Signals (RTS) as reported in [1], [2]. Still, the fundamental motivations for shrinking pixel size include increasing the resolution for a given camera module size. But it makes the in-pixel charge storage efficiency a prominent parameter to reach high pixel performances. Therein lies the fundamental challenge of the high-resolution CIS using long duration charge storage in FD such as CIS operated in global shutter mode or burst mode as discussed in [3], [4].

In this study, the leakage current non-uniformity, as well as the leakage current RTS sources, are investigated in FD. This study provides another vision and complete other investigations such as [5] led on the output voltage temporal noise. Here, results point out that high magnitude electric field regions could explain the high FD leakage current non-uniformity and its fluctuation. Additionally, high magnitude electric field effects, such as transfer-gate-induced leakage current, are investigated to further understand the phenomena involved in FD while giving new insights on the electric field enhancement of the charge generation mechanisms.

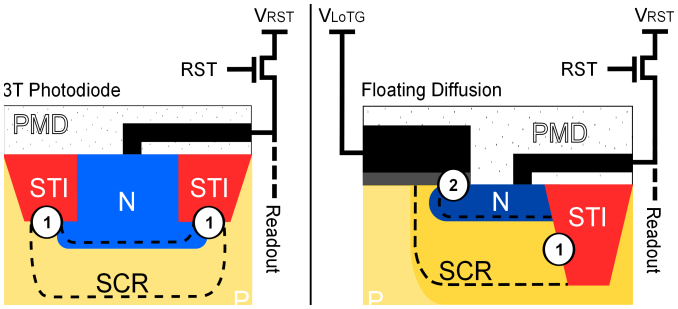

Fig. 1. Cross section illustrations depicting the structural differences between a conventional 3T photodiode (left) and a FD (right). Si/SiO_2 interface defects located in the depleted regions are referred to as ①. The Gate Induced Leakage (GIL) current is referred to as ②. SCR: Space Charge Region. PMD: Pre-Metal Dielectric. STI: Shallow Trench Isolation.

II. Experimental Details

The CIS under test is a 512×512 4T PPD custom imager manufactured in a commercially available $180\,\mathrm{nm}$ CIS technology. The CIS is operated as a 3T CIS where the transfer gate (TG) is kept at its low bias level and variable FD integration time is inserted between the signal and the reference samples. This FD integration time is directly linked to the charge retention time in the case of a global shutter configuration as well as in the case of any application where the generated charges are stored in-pixel in a FD. This CIS has been designed allowing modifying both the TG bias (i.e. V_{LoTG}) as well the reset voltage (i.e. V_{RST}). Fig. 1 illustrates the cross-section of the considered FD structure (right). To explore the FD leakage current sources as well as the technological levers which can influence it, several bias

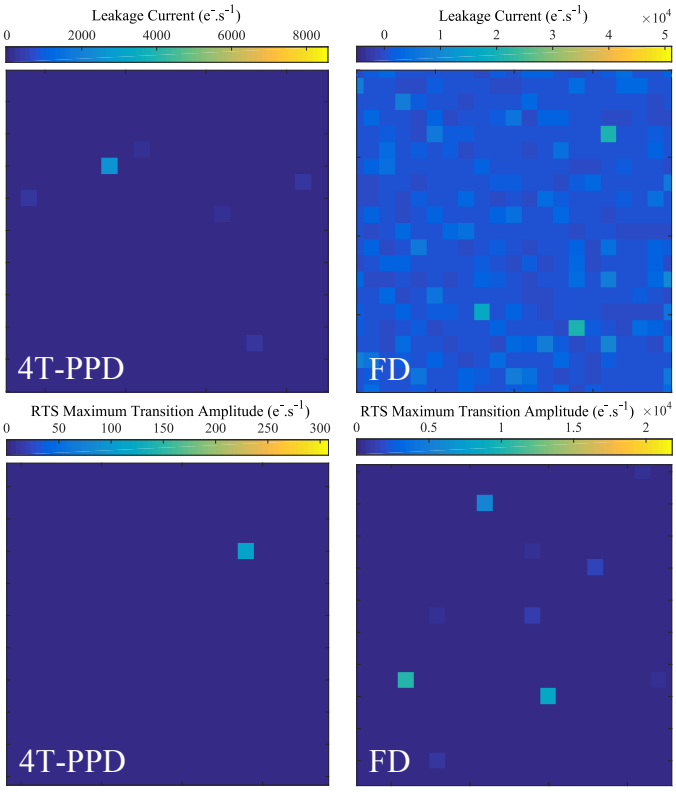

Fig. 2. Leakage current and RTS maximum transition amplitude over a small part of the sensor array in 4T-PPD (left) and in FD (right) (V_{RST} = 3.3 V ; V_{LoTG} = 0 V).

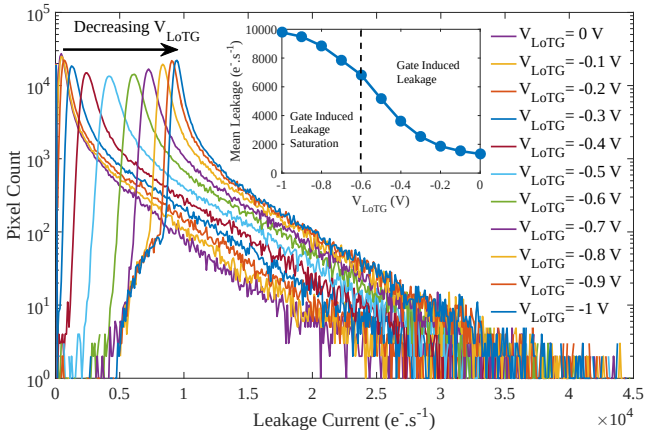

Fig. 3. Evolution of the mean and the distribution of the FD leakage current with the V_{LoTG} bias (V_{RST} = 3.3 V).

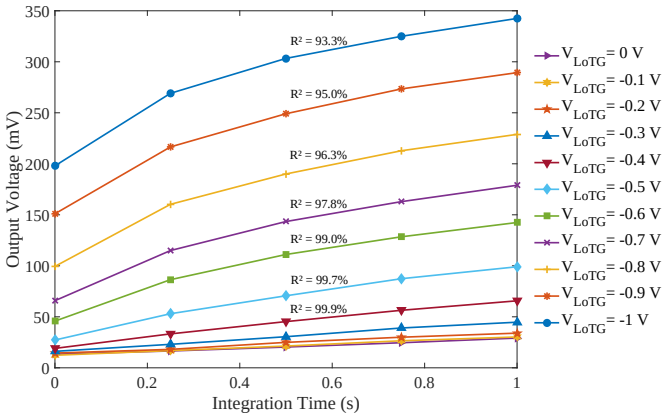

Fig. 4. Evolution of the output voltage of a single representative FD of the sensor array with the integration time for different V_{LoTG} bias (V_{RST} = 3.3 V).

conditions at room temperature have been tested by following both the FD leakage current non-uniformity as well as the FD leakage current RTS.

III. FD Leakage Current Non-Uniformity

The leakage current over a small and representative part of the sensor array both in the 4T-PPD (left) and in the FD (right) are reported in the upper part in Fig. 2. In the FD, the leakage current is about three orders of magnitude higher than the ones observed in the 4T-PPD. The observed FD leakage currents are even higher than the ones commonly observed in conventional 3T photodiode whose structure might seem similar [6]. To better understand the possible leakage current sources in FD, a comparison to the conventional 3T photodiode is proposed. As illustrated in Fig. 1 depicting the cross-sections of a conventional 3T photodiode (left part) and a FD (right), the FD structure presents several particularities. First, the Si/SiO_2 interface located in the depleted regions and referred to as ① presents a larger surface contact in the FD structure than in the 3T photodiode structure. When depleted, the STI sidewalls are known to be a high defect concentration region and have been identified as the dominant leakage current source in [7]. Results reported in Fig. 2 suggest the existence of a multitude of generation centers located at the Si/SiO_2 interfaces like the TG oxide and the shallow trench isolation (STI) sidewalls which are directly in contact with the FD depleted regions. Moreover, due to the transistor-based N-implant constituting the FD junction, a higher electric field is expected to be found in the FD depleted region compare to the one in the 3T photodiode. Consequently, an electric field effect on the FD leakage current can be expected [7].

The mean and the distribution evolution of the FD leakage current with the TG bias are visible in Fig. 3. Results highlight a gate induced leakage (GIL) current which increases the mean leakage current with decreasing TG bias as already observed in [8], [9]. This GIL current is related to the TG overlap with the N-implant referred to as ② in Fig. 1. Regarding the leakage current distribution, this GIL current leads to a shift of the entire histogram toward higher leakage current without any change in the leakage current tail. The impact of the TG-induced electric field on the leakage current results in a uniform leakage current increase over the sensor array.

The evolution of the output voltage of a single representative FD with the integration time for different TG bias is reported in Fig. 4. With increasing TG bias, the leakage current (i.e. proportional to the slope) is increasing as already observed in Fig. 3. However, the induced TG electric field degrades the FD linearity which is followed by the linear correlation

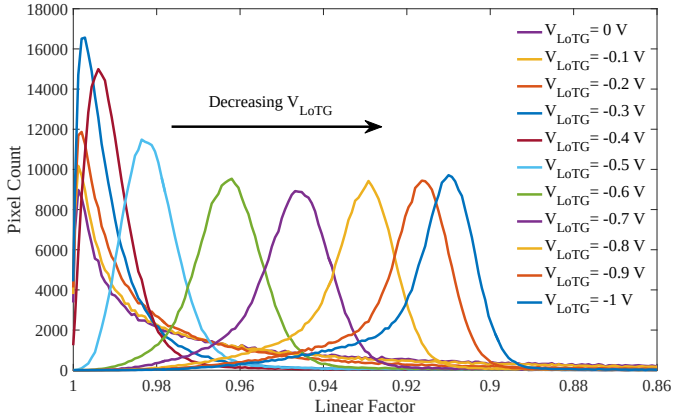

Fig. 5. Evolution of the FD linear factor histogram over the sensor array with the V_{LoTG} bias ($V_{RST} = 3.3\,V$).

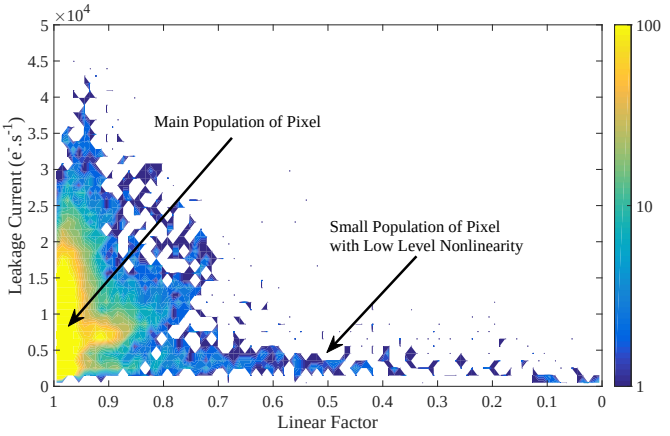

Fig. 6. Two dimensions histogram showing the FD linear factor as a function of the leakage current ($V_{RST} = 3.3\,V$; $V_{LoTG} = 0\,V$).

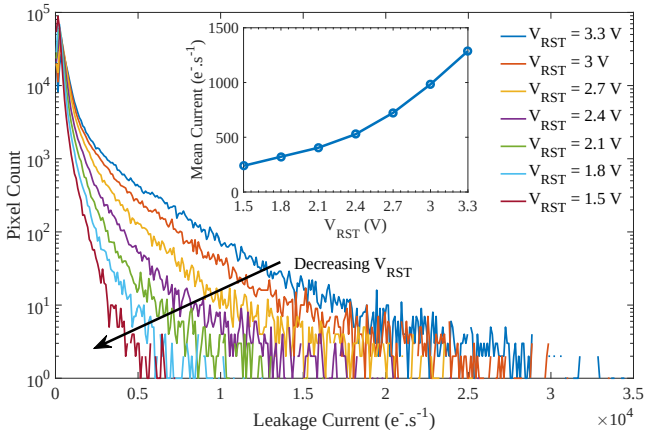

Fig. 7. Evolution of the mean and the distribution of the FD leakage current with the V_{RST} bias ($V_{LoTG} = 0\,V$).

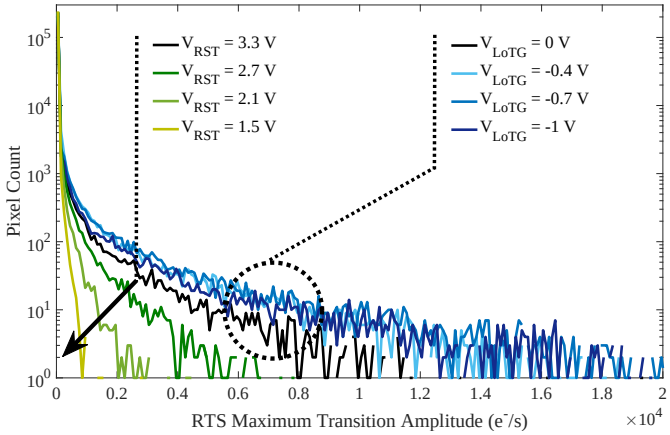

Fig. 8. Histograms of the RTS maximum transition amplitude in FD over the sensor array for different bias conditions. The impact of V_{LoTG} is followed with $V_{RST} = 3.3\,V$ and the impact of V_{RST} is followed with $V_{LoTG} = 0\,V$.

factor referred to as R^2. The observed non-linearity could be explained by the reduction of the field-assisted GIL current with decreasing FD potential during the charge integration. The reset voltage evolution does not induce any non-linearity in the FD.

The evolution of the FD non-linearity over the sensor array with the TG bias is reported in Fig. 5. As seen on the distributions, the majority of the FD over the sensor array are impacted by the TG-induced non-linearity. It empathizes that the TG low-level bias has to be considered for long duration charge storage in FD. Fig. 6 shows the two dimensions histogram showing the FD linear factor as a function of the leakage current at $V_{LoTG} = 0\,V$. Although the main population of pixel discloses good linearity as observed in Fig. 5, a small population of low leakage current pixels reveals poor linearity. The previously observed non-linear FD in Fig. 5 at $V_{LoTG} = 0\,V$ could be attributed to low FD leakage current non-linearity or FD presenting low signal to noise ratio (SNR).

The evolution of the mean and the distribution of the FD leakage current with the reset voltage is reported in Fig. 7. The mean leakage current decreases with the decreasing reset voltage for which the linearity of the electrical transfer function is ensured. Regarding the FD leakage current distribution, the reset voltage induced electric field only impacts the leakage current tail conserving the same leakage current for the majority of the FD over the sensor array. The leakage current tail is extended with increasing reset voltage. Results suggest the existence of an electric field enhancement (EFE) of generation centers located in high magnitude electric field regions corresponding to a small population of FD as discussed in [10], [11]. This evolution, which cannot be highlighted by the mean leakage current evolution, can not be attributed to a simple depleted region extension since it would have led to a shift of the whole histogram. Therefore, the FD electric field distribution also needs to be addressed to ensure long duration charge storage in FD.

IV. FD Leakage Current RTS

RTS analysis is performed using a rising edge algorithm [12] and following the maximum transition amplitude [13].

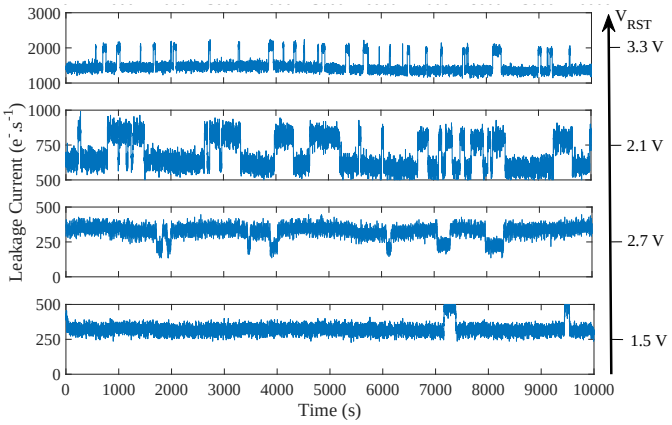

Fig. 9. Leakage current evolution with time of on single pixel for different reset voltages operated with $V_{LoTG} = 0\,V$.

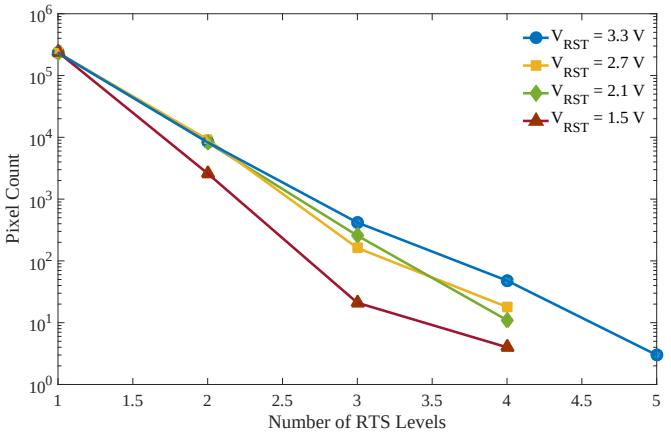

Fig. 10. Histograms of the number of RTS level in FD for different reset voltages with $V_{LoTG} = 0\,V$.

The histograms of the RTS maximum transition amplitudes in FD over the sensor array for different bias conditions are reported in Fig. 8. The TG induced electric field does not lead to a strong impact on the RTS maximum transition amplitude distribution. However, decreasing V_{RST} clearly reduces the RTS distribution tail. Results suggest that defects responsible for the RTS behavior in FD are impacted by the reset voltage which tends to enhance RTS amplitudes with increasing V_{RST} bias. The observed RTS amplitude enhancement is also reported in Fig. 9 showing the leakage current evolution of a FD presenting an RTS center impacted by the reset voltage. Once again, the RTS amplitudes increase cannot be attributed to a simple depletion region extension in the FD since RTS amplitudes analysis lies in the evolution of the strongest RTS center [6]. However, the depletion extension explains the mean leakage current increase with the reset voltage visible in Fig. 9. As previously introduced in Fig. 7 for the leakage current, results highlight the role of the reset voltage induced electric field into the FD PN junction both on the leakage current and the RTS amplitudes.

Fig. 10 shows the RTS levels histogram evolution with the reset voltage. Results show that the reset voltage induced electric field reduces the number of detected RTS levels probably due to the RTS amplitude enhancement or the activation of field-assisted RTS centers. As mentioned for the leakage current, it suggests the existence of high magnitude electric field regions which play a major role in the FD leakage current RTS. The TG bias evolution does not induce any RTS level change in the FD.

V. Conclusion

The main conclusion of this study is that in FD, the GIL current is the major contributor to the overall leakage current whereas the main mechanism that enhances the RTS amplitude is the electric field induced by the reset voltage. Results empathize the existence of high magnitude electric field regions in the FD inferring that electric field profiles must be addressed for high-resolution CIS using long duration charge storage in FD such as CIS operated in global shutter mode or burst mode.

References

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