Demonstration of Monolithically Integrated Pixel Sensors Based on Optical Back Biasing in 28nm node FDSOI Technology

L.Kadura[1], O.Rozeau[1], A.Ayres[1*], L.Grenouillet[1], N.Rambal[1], A.Chelnokov[1] and M.Vinet[1]
[1]Univ. Grenoble-Alpes, CEA, LETI, 17 Avenue des Martyrs, 38000 Grenoble, France
[*] Now with STMicroelectronics, Crolles, France
Contact email: laurent.grenouillet@cea.fr

Abstract A monolithically integrated pixel sensor, consisting in co-integrating a photodiode in the substrate of a Fully Depleted Silicon-On-Insulator (FDSOI) transistor, is proposed. The operation principle of this so-called FDPix sensor is based on a Light Induced V_T Shift (LIVS) due to optical back biasing of the FDSOI transistor under photodiode illumination. Using this FDPix concept, a light sensitive inverter is demonstrated. Two different pixel designs relying on the variation of the Voltage Transfer Characteristic (VTC) of the inverter with light intensity are proposed and fabricated in 28nm FDSOI technology, aiming at either analog or digital applications, respectively. The proposed 2T analog pixel uses a saturated load inverter architecture to convert LIVS to output voltage shift. Experimental results demonstrate an LIVS gain obtained on the analog output voltage as high as ×4. A pulse width modulation (PWM) based pixel is designed using light sensitive CMOS inverters. By comparing the output of a standard inverter with a light sensitive one, a variation of the output pulse width of about 180µs is measured, keeping a high dynamic range of 120dB.

I. Introduction

CMOS pixel sensors market kept growing in the recent years [1]. New applications are emerging in the automotive, security, medical and machine vision domains where the Dynamic Range (DR) and power consumption are key parameters to be optimized [2], [3]. A relevant pixel architecture developed for high DR and high speed applications is the Digital Pixel Sensor (DPS) where analog voltage variation is converted to time domain output variation [4]. DPS are usually based on Pulse Modulation (PM) techniques [5], in which the output voltage is compared to a reference voltage locally in each pixel. Since the output signal swing does not depend on the power supply, the DR is extended, and the power consumption can be reduced.

Recently, we proposed a light sensitive FDSOI transistor (FDPix) that exhibits a Light Induced V_T Shift (LIVS) [6]–[9]. It has been investigated using TCAD simulations and experimentally demonstrated using 28nm FDSOI technology. SPICE modeling was developed to reproduce FDPix transient characteristics and demonstrate the reset of this one transistor (1T) pixel sensor. It is also used to explain the Lin-Log dual response experimentally observed for this sensor. The logarithmic response at high intensities results in a dynamic range of 120dB while the linear response at low intensities improves performance under low illumination. In this paper, we demonstrate new circuit architectures based on light sensitive inverters employing the FDPix, where the Voltage Transfer Characteristic (VTC) of the inverter varies according to the light intensity. These architectures lead to important advantages regarding size, sensitivity, power consumption and DR. An analog pixel based on a saturated load inverter, as well as a Pulse Width Modulation (PWM) based pixel using CMOS inverters are designed and experimentally demonstrated on silicon. The circuits are designed using FDPix dedicated SPICE model and fabricated using STMicroelectronics 28nm FDSOI technology.

II. FDPix & CMOS inverter

The FDPix sensor consists in an FDSOI transistor with a photodiode monolithically integrated under the Buried Oxide (BOX) by means of ion implantation (Fig.1). Under illumination, photogenerated charges separated by the junction electric field, accumulate at the BOX/substrate interface and modify the potential (Fig.2a). Due to a capacitive coupling between the channel and the BOX/substrate interface, the V_T of the transistor shifts with light intensity. This Light Induced V_T Shift (LIVS) is the main parameter of our device, as illustrated in the experimental I_DV_G curves in Fig.2b. Depending on the transistor type and diode orientation, complementary responses are obtained which are summarized in Fig.3.

When the CMOS inverter (i.e. NOT gate, here referred as CMOS inverter) is designed using FDPix, its VTC becomes sensitive to light illumination as depicted in Fig.4. This results from the complementary LIVS exhibited by the Pull Up (PU) PMOS and Pull Down (PD) NMOS transistors, on which depends the VTC and its switching threshold (V_M). Increasing optical power results in higher shift of V_M. The shift direction depends on the photodiode orientation. Hence, different responses are possible based on the available configurations shown in Fig.3, which offers multiple design options depending on application. A back bias applied to the electrical back gate of the PU and PD transistors can also be used to shift the VTC towards either higher or lower V_M values. This property allows the tuning of the nominal inverter' V_M. The CMOS inverter has the particularity of consuming very low power since current flows only when it switches. Therefore, it can be used and implemented as a logic gate, to obtain a PWM signal for low power pixel sensor, as demonstrated in section IV. Also, by changing the PU transistor with a saturated load, the inverter can be used as an analog amplifier as presented next.

III. Analog readout: Saturated load inverter

We designed a 2T FDPix sensor with a Light Induced V_{out} Shift ($LIV_{out}S$) analogous to the LIVS of the 1T FDPix. The circuit is shown in Fig.5.a and consists in a diode-connected PMOS transistor used as a saturated load in an inverter. Both the load PMOS and driver NMOS are FDPix. In this first realization, we use front side illumination of the pixel. As can be seen in the layout (Fig.5.b), the length of the transistor active region (S_a/S_b) are here larger than minimum dimensions to maximize the light absorption. Note that under back side illumination, this architecture would also maximize the fill factor since both transistors are sensitive to light. As for the CMOS inverter, the saturated load inverter VTC (V_{out} vs V_{bias}) depends on both transistors' threshold voltages. When biased in the transition region where both transistors are in saturation, V_{out} can be expressed as follows:

$$V_{out} = \sqrt{\beta_n/\beta_p} * (V_{bias} - V_{Tn}) + V_{DD} - V_{Tp} \quad (1)$$

where $\beta_n = C_{ox} * \mu_n * W_n/L_n$, and $\beta_p = C_{ox} * \mu_p * W_p/L_p$, are the gain factors of N- and PMOS respectively, and V_{Tn} and V_{Tp} are their threshold voltages. V_{DD} is the supply voltage. Each FDPix of the inverter will exhibit an LIVS under illumination, which in turn will shift the VTC. Therefore, a $LIV_{out}S$ will be induced. This is demonstrated in Fig. 6, where the experimental VTC of an inverter with NP oriented junction (Fig.5.a) is plotted for different light intensities. The light source used is a wide band Xe lamp. To identify the optimal bias point that results in maximal gain, Fig.7 shows the $LIV_{out}S$ vs V_{bias} as deducted from Fig.6. Fig.8 shows the LIVS vs light intensity (P_{opt}) for individual N- and PMOS transistors and for the inverter at a V_{bias} of 0.45V. A gain of almost x4 is obtained, and the intrinsic logarithmic response is kept thus resulting in high dynamic range of 120dB. The gain of the amplifier can be modulated by changing the beta ratio, i.e. the transistors' dimensions. This is shown in Fig.9, where it increases from 4 to almost 5.5 at V_{bias} 0.45V using a higher beta ratio. However, the higher gain is obtained at the expense of a narrower operation range for V_{bias}. This tradeoff is shown in Fig.10.

As previously mentioned, depending on the diode orientation, complementary VTC variations can be obtained. The light sensitive saturated load inverter can thus be used as an efficient high DR, and high sensitivity 2T FDPix sensor.

IV. Time domain readout: Pulse Width Modulation

The proposed PWM circuit is presented in Fig.11. By comparing the output of a light sensitive CMOS inverter with a standard inverter, using a common applied input signal, the comparator output pulse width is modulated with light intensity. A layout view of the first configuration using a XOR gate as a comparator is depicted in Fig.12. The advantage of using a XOR is that it guaranties an output whether the V_M of the inverters are matched or not. Fig.13 demonstrates the DC opto-electrical characteristics from hardware measurements showing the output of both inverters and the XOR. The pulse output width is clearly reduced under light illumination. In addition, a back bias can be applied on the non-sensitive inverter to calibrate or tune the initial output signal. As presented in Fig.14 and Fig.15, a positive or negative back bias changes the width of the initial pulse output. Thus, the back bias allows choosing whether to increase or decrease the pulse width with light illumination. As was mentioned in section II, changing the photodiode orientation will result in a complementary effect where the shift under illumination is measured in the opposite direction as illustrated in Fig.16. Fig. 17 shows the case of NAND gate used as a comparator, reducing the number of transistors per pixel (8T/pixel vs 12T/pixel using a XOR gate). The output shows a shift of the rising edge. By performing transient characterization shown in Fig. 18 at different light intensities, the difference of pulse width between dark and light output signals of the NAND gate are plotted vs P_{opt} and depicted in Fig.19 for different V_{DD}. The circuit can operate at low voltages, which makes this sensor ideal for low power applications. The DR depends on V_{DD}; however, using back bias, it can be extended to the FDPix DR at all V_{DD}.

This circuit presents the advantage of generating the reference signal locally, which leads to reduced process variability related errors. In addition, by representing the LIVS in time domain, the signal is immune to voltage level variations achieving high Signal to Noise Ratio (SNR), high DR, and low power pixel sensor. Table 2 summarizes the different pixel architectures presented with their respective readout scheme.

V. Conclusion and perspectives

In this paper, based on the FDPix sensor, we presented circuit implementation based on light sensitive inverters. A 2T analog pixel sensor was demonstrated using a saturated load inverter, allowing improved sensitivity, and high DR. We also proposed a PWM-based FDPix sensor by comparing the output of a light sensitive CMOS inverter with a non-sensitive one. The PWM scheme allows high SNR, low power consumption and high DR. This study shows the potential of using the FDPix as a light sensitive inverter and paves the way to circuit demonstration using 28nm FDSOI for low power, high DR and high sensitivity sensing applications.

Acknowledgment

The authors would like to thank STMicroelectronics for wafer processing in Crolles facilities.

References

[1] Yole Developpement, 2018.
[2] N. Katic *et al.*, *IEEE Sensors Journal*, Jul. 2015.
[3] E. Artyomov *et al.*, *Inf. Theor. Appl.*, Jan. 2007.
[4] O. Skorka *et al.*, in *Nanosensors, Biosensors, and Info-Tech Sensors and Systems 2014*, 2014, p. 90600G.
[5] D. G. Chen *et al.*, *IEEE Transactions on Biomedical Circuits and Systems*, Feb. 2011.
[6] L. Grenouillet *et al.*, in *2014 IEEE S3S*, 2014, pp. 1–2.
[7] L. Kadura *et al.*, in *2016 IEEE IEDM*, 2016, pp. 32.6.1-32.6.4.
[8] L. Kadura *et al.*, in *2018 SSDM*, 2018, pp. 589–590.
[9] L. Kadura *et al.*, *IEEE Transactions on Electron Devices*, May 2019.

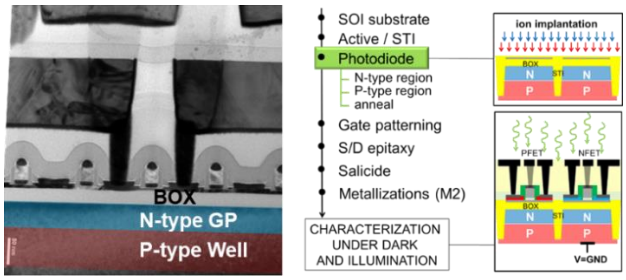

Fig.1: FDPix TEM image and process flow, illustrating the diode implementation (here BOX/NP) below the buried oxide of FDSOI transistor.

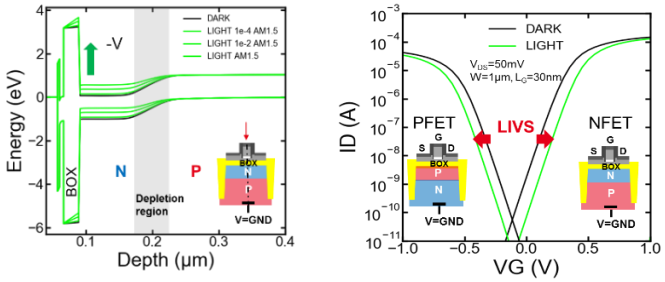

Fig.2: a) band diagram under dark and different diode illumination for a MOS / BOX / NP diode structure b) I_DV_G curve of NMOS and PMOS in dark and under illumination when NP and PN diode is implemented below the BOX, respectively.

Configuration below the BOX					
Light effect	NFET	none	negative back bias	none	positive back bias
FET Light-Induced V_T-Shift (LIVS)	NFET	none	reverse BB	none	forward BB
LIVS amplitude	NFET	none	Increases w/ P_{OPT} and BF	none	Increases w/ P_{OPT} and BF
Light effect	PFET	none	negative back bias	none	positive back bias
FET Light-Induced V_T-Shift (LIVS)	PFET	none	forward BB	none	reverse BB
LIVS amplitude	PFET	none	Increases w/ P_{OPT} and BF	none	Increases w/ P_{OPT} and BF

Fig.3: N- and P-FET with different junction configuration and the expected Light-Induced Vt Shift (LIVS) showing the complementary effect with diode orientation and FET-type.

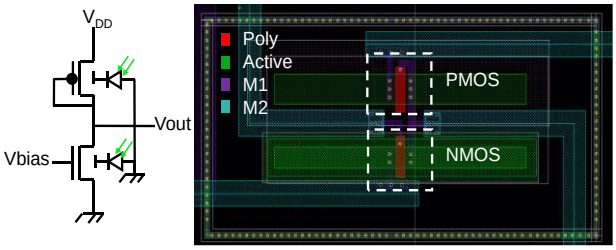

Fig.5: a) Schematic and b) layout of saturated (sat.) load inverter sensitive to light using the FDPix

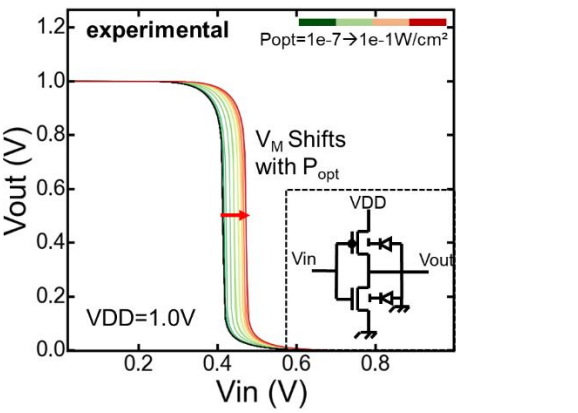

Fig.4: Light sensitive CMOS inverter voltage transfer characteristics VTC at different light intensities

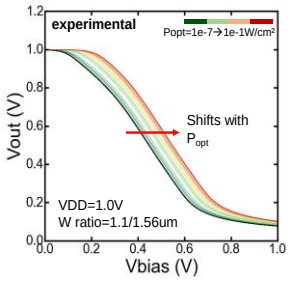

Fig.6: Voltage transfer characteristic (VTC) of sat. load inverter for different light intensities

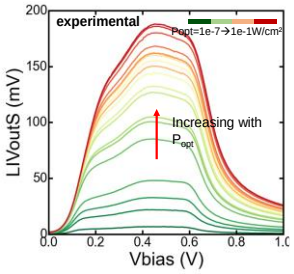

Fig.7: $LIV_{out}S$ for sat. load inverter under different light intensities

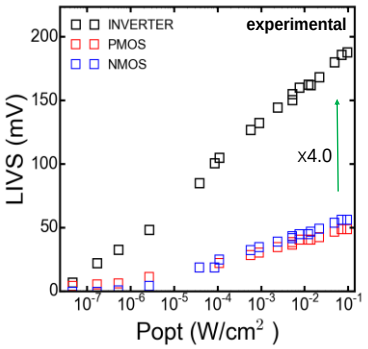

Fig.8: LIVS vs P_{opt} for N- and PMOS transistors and sat. load inverter at V_{BIAS}=0.45V

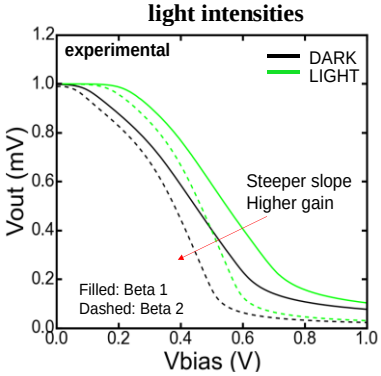

Fig.9: sat. load inverter VTC in dark and under illumination for two beta ratios

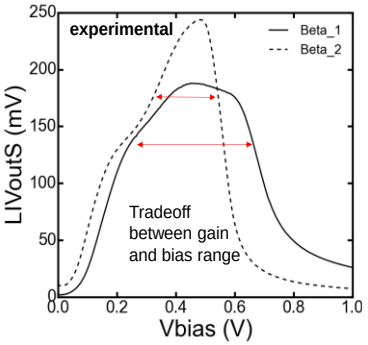

Fig.10: $LIV_{out}S$ of sat. load inverter vs V_{bias} for two beta ratios

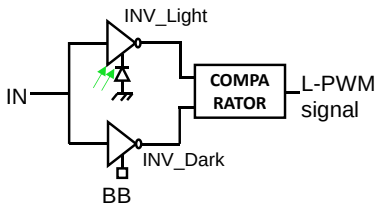

Fig.11: Schematic of the proposed L-PWM pixel sensor comparing the output of two inverters: INV_L sensitive to light, and INV_D not sensitive to light

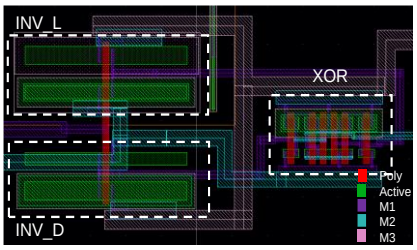

Fig.12: Layout view of the proposed L-PWM pixel sensor. The comparator is a XOR gate

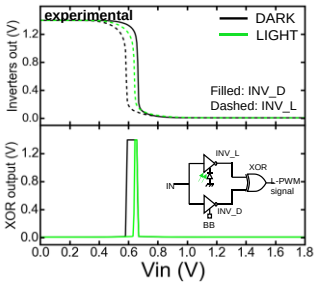

Fig.13: L-PWM pixel response showing the inverters output and the XOR gate output used as a comparator

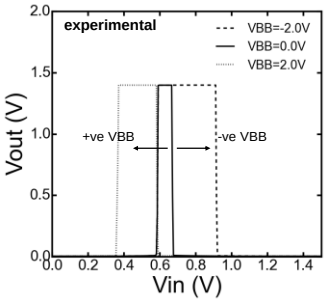

Fig.14: XOR output signal in dark applying forward and reverse back bias on INV_D

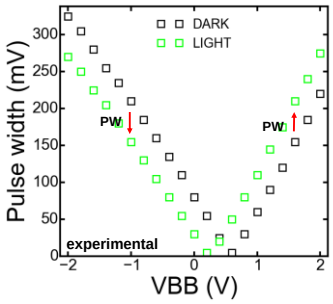

Fig.15: XOR output pulse width in dark and under illumination while applying forward and reverse back bias

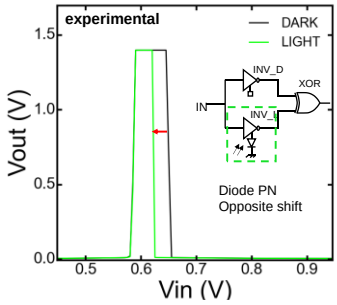

Fig.16: Complementary effect on XOR gate output using a PN oriented junction (vs Fig 13 config.)

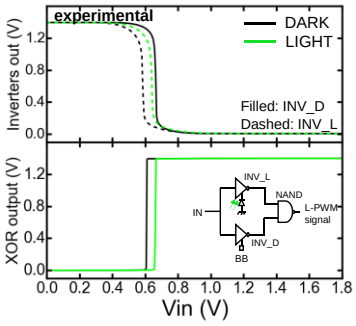

Fig.17: L-PWM circuit response showing the inverters output and the NAND gate output used as a comparator

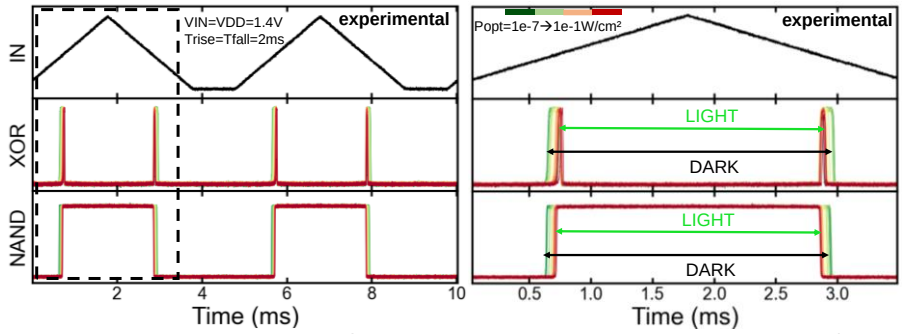

Fig.18: Transient characteristics of L-PWM circuit showing input signal, output of XOR and NAND gate for different light intensities

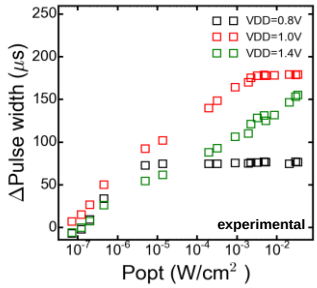

Fig.19: ΔPulse width vs Popt for the NAND output signal at different VDD

	Circuit comp.	#of T/pixel	Readout signal	Gain	Tunability using VBB
FDPix	N-or PMOS transistor	1	Current	x	+
Analog	Sat. load inverter	2	Voltage	++	+
L-PWM	2 inv+XOR	12	Rising edge-to-Rising edge	x	++
	2 inv+NAND	8	Pulse width	x	++

Fig.20: Summary of light sensitive inverter based pixel configurations