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A 2.5µm 9.5 Mpixel high framerate CMOS imager with hybrid output multiplexer and 58Gb/s datarate

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Abstract: **The imager presented in this paper demonstrates an architecture with high spatial, 4kx2k, and high temporal, 360fps, resolution and a high output datarate, 58Gb/s. A targeted pixelrate of 3.6Gpix/s makes the requirements for pixel addressing, ADC conversion time and output multiplexing challenging. We discuss the chip architecture and measurement results for a prototype chip are given. The image sensor is manufactured in a 110/180 nm CMOS process.**

I. Imager Architecture

The block diagram for the image sensor is given in figure 1. The array consists of 4224 (H) x 2248 (V), 2.5 µm, 4T-4shared pixels as drawn in figure 2. An external programmable timing generator is used, to have flexible vertical addressing, to support different readout modes and different binning or quincunx readout schemes [1]. The pixel array is driven by on-chip digital shift registers followed by levelshifters. To reduce the number of levelshifters, a cross connected topology is used as in [2]. The rowdriver and pixel connections are shown in figure 3. Each column of shared pixels has one charge-domain multi-slope column ADC [3]. Placing the ADCs on top and bottom yields a width of 10 µm per ADC per side. To enable the highest possible framerate [4], processes like light integration, column sampling, AD Conversion and output multiplexing run in parallel. Every ADC on the column is sampling on one capacitor, while converting on a second capacitor to maximize the column settling time and maximizing the ADC conversion time per row readout. The 2112 ADC outputs generate 16b data at max 1.7MS/s/ADC. The ADC output multiplexing topology is a hybrid architecture, as explained in section III. With a pixelrate of 3.6 Gpix/s and a resolution of 16b from the ADC, the output datarate is 58 Gb/s. The imager has 32 LVDS outputs with programmable serialization factors. The maximum output datarate is 1.8 Gb/s per LVDS-channel.

II. Vertical Row addressing

To suppress kTC-noise, off-chip digital CDS is used in the form of Digital Double Sampling (DDS). This scheme requires a doubling of the (raw) datarate. Alternatively, differential DDS is possible, reducing the required raw datarate from 2x to 1.5x [2]. A full charge transfer from photodiode to floating diffusion in the shared pixel, typically needs a transfer time of 1µs. For high framerate at full resolution, the available time for column settling and A/D conversion makes it impossible to meet this requirement without addressing multiple rows [5]. With 1124 rows of 4 shared pixels, the available time to read a sample at 360 fps is 618 ns. A feasible transfer time of 1µs therefore requires two rows of pixels to be addressed concurrently. While one row is being selected another one is being transferred. To minimize the number of individual shiftregisters, an innovative row addressing scheme has been developed with use of dynamic forward/backward shifting of the tokens in the vertical digital shiftregisters. With the proposed vertical

addressing scheme, a high framerate can be achieved while maintaining a transfer time of 1µs and allowing the column to settle during the full rowtime. A detailed timing diagram is given in figure 5.

III. Hybrid output multiplexer

An analog tristate multiplexer is compact with low power, but the long wires result in low bandwidth. A full digital shift register is fast but, since $P = C.V^2.a.f$, it is not power efficient due to the high frequency (f) for all data and it leads to routing congestion due to the high number of inputs.

The multiplexer, Figure 6, is implemented as a topology of hybrid analog tristate multiplexers (blue) and digital shiftregisters (purple). A first stage of 11:1 analog tristate multiplexers is followed by a register stage to latch the current tristate multiplexer values and to allow the next value for the tristate multiplexer to settle. A 6:1 multiplexer is used to switch between six 11:1 stages. The output of the 6:1 multiplexer loads a two register deep shiftregister. This last stage also enables daisy chaining to trade the required output bandwidth with the number of active output lanes.

The benefit of this topology is that only two registers per 132:1 multiplexer run at the highest clockrate and 12 registers run at the clockrate divided by 12 compared to 132 registers running at the highest clockrate for a full digital shiftregister.

IV. Measurement results

The chip with the proposed architecture was designed and fabricated. It is packaged in a custom ceramic 215 pin µPGA package. Lag in this imager is verified with a LED flash in frame 1, and measuring the output response in the following frames. The result is a lag performance smaller than $1e^-$ as shown in figure 4. The measurement results for the shotnoise curve are shown in figure 7. An expected $75uV/e^-$ was measured with a readnoise of $5.5e^-$. The darkcurrent histograms for various temperatures are shown in figure 8. A chip photograph is shown in figure 9. The key characteristics for this chip are summarized in table 1.

V. Conclusion

With the proposed architecture for the hybrid output multiplexer and readout schemes for the vertical shiftregisters, we realized a 9.5Mpixel CMOS imager with 3.6Gpix/s enabling high framerate. The prototype chip successfully demonstrated read out at 360fps resulting in 180fps after DDS with a lag performance $<1e^-$.

VI. Acknowledgements

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References:

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[4] J. Bogaerts et al. “High speed 36 Gbps 12Mpixel global pipelined shutter CMOS image sensor with CDS” R60, IISW 2011.

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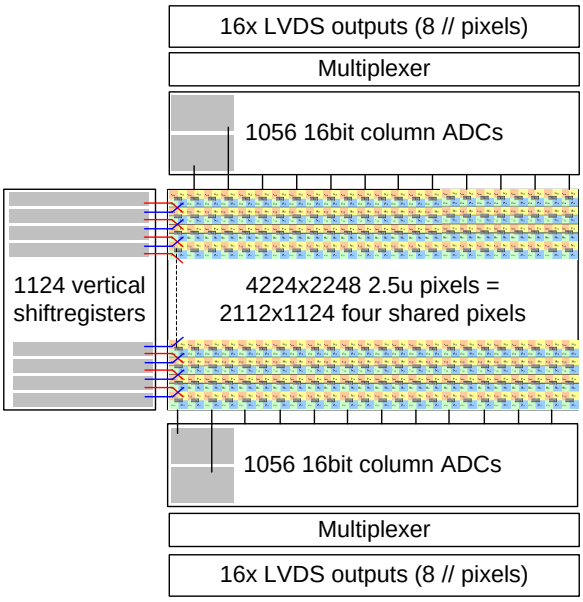

Figure 1: Imager block diagram

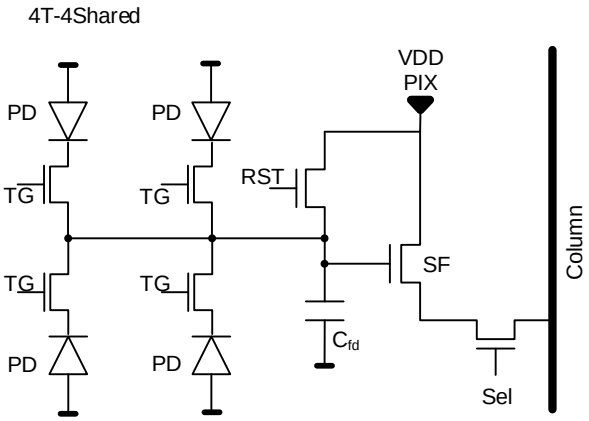

Figure 2: Pixel schematic

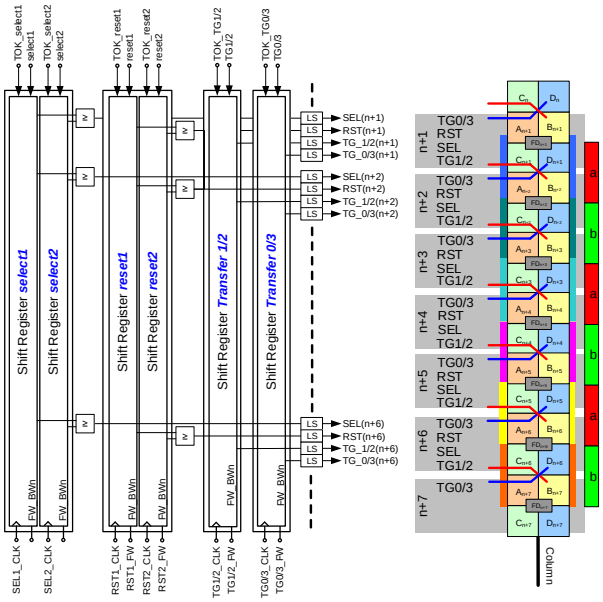

Figure 3: Rowdriver arrangement & pixel connections

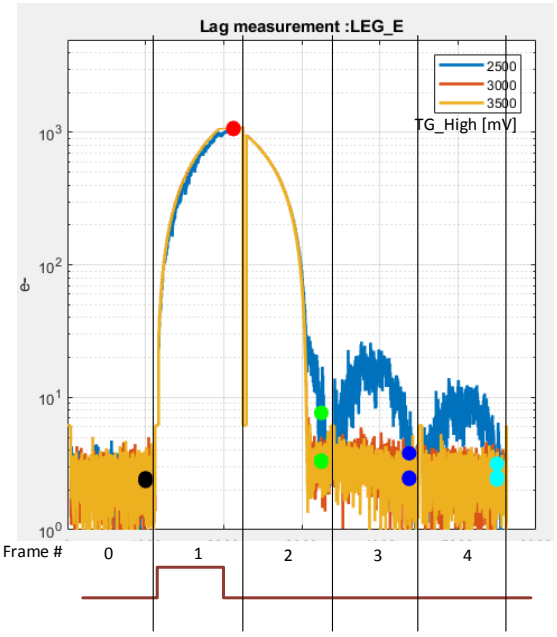

Figure 4: Lag measurement

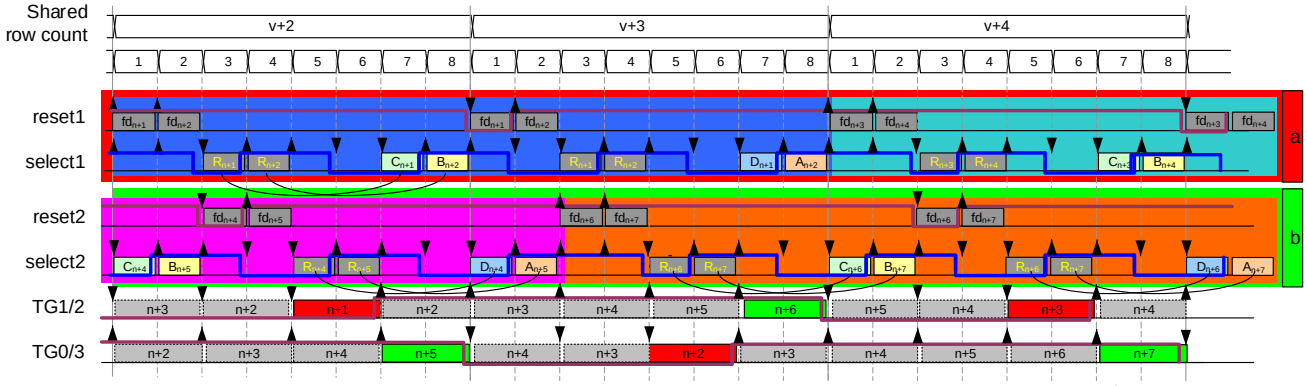

Figure 5: Timing diagram

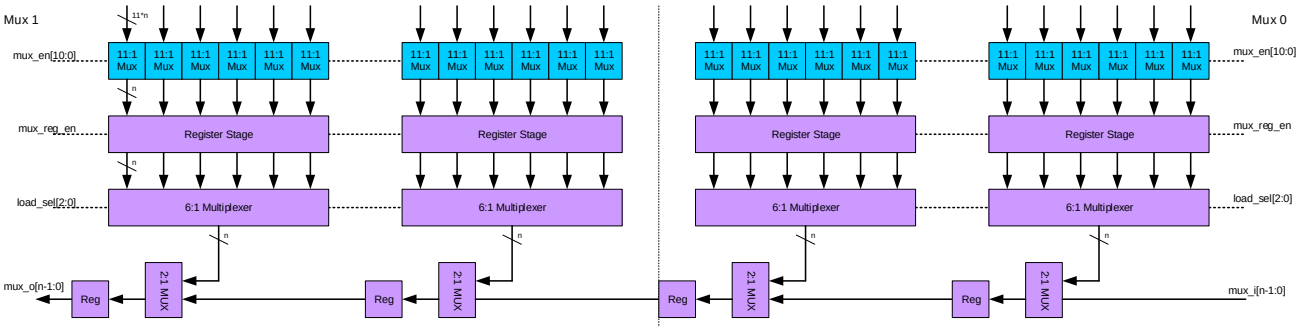

Figure 6: Column hybrid output multiplexer

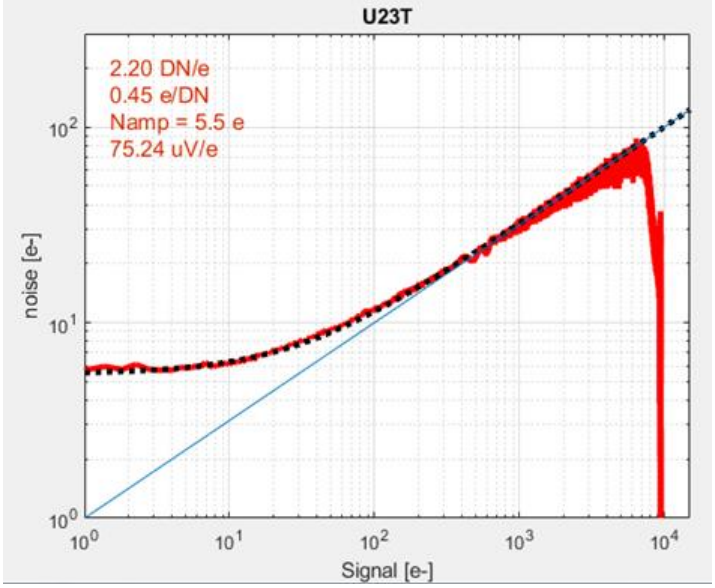

Figure 7: shotnoise curve

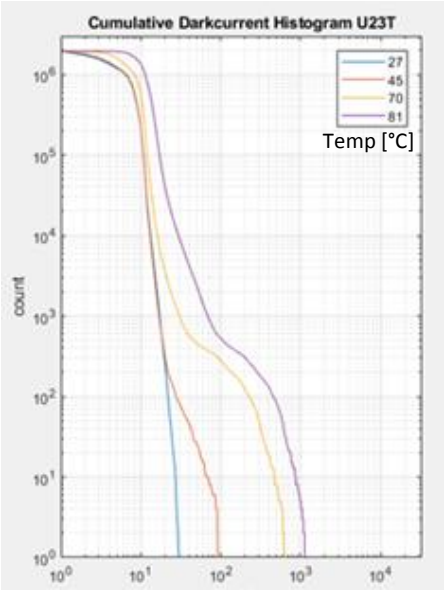

Figure 8: Measured darkcurrent tails

Parameter	value		remark
Process technology	CMOS 1P4M		
pixel	110nm		
periphery	180nm		
Chip size [mm2]	197		
Number of pixels (Total)	4224x2248		Incl black ref pixels
Number of pixels (effective)	4096x2160		
Supply voltage	1V8, 2V5, 3V3		
Pixel	4T 4shared		
Pixel size [µm x µm]	2.5 x 2.5		
Saturation [e-]	10k		
random noise [e-]	5.5		
Lag	<1e-		
Outputs	LVDS, 32 lanes		
Total output datarate [Gbps]	58		
Framerate [fps]	120	360	raw, unprocessed
ADC resolution [#bit]	16	12	selectable
Power [W]	3.5	4.8	
Package	ceramic, 215 µPGA		

Table 1: Chip parameters

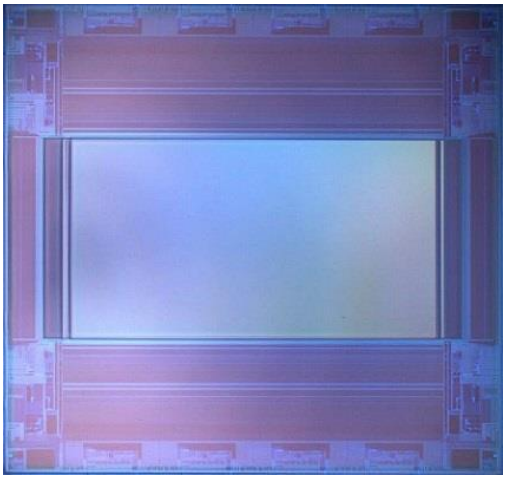

Figure 9: Chip photograph of the prototype image sensor