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High speed 25M global shutter image sensor with 2.5μm pixel

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Abstract
In this paper we present a 1.1 inch 25M global shutter (GS) image sensor with 2.5μm pixel for high speed industrial applications. Thanks to the high performance small pixel designed by TPSco, this GS sensor provides the largest resolution for the given optical size. Low power double edge clock counting ADC is used to convert image signal into 10/12 bit digital word. With this, the power consumption can reach less than 1.5W with full speed of 150fps.

Pixel and Operation
Low noise voltage domain GS pixel is not easy to shrink due to the limitation on size of in-pixel sampling capacitor. Talking about small GS pixel, the technology trend goes to charge domain in recent years. TPSco has successfully developed so far the world's smallest charge domain GS pixel [1]. Figure 1(a) shows the schematic of this 2.5μm pixel, with in-pixel charge transfer to the memory node (MN) for pipelined global shutter operation. In order to increase the full well, pixels need to be diagonally shared to maximize the area of photodiodes (PD) and MN.

Not only the readout path, also several control signals are shared between vertical neighbor pixels to maximize the active and metal opening for best electrical and optical performance. Operation of the pixel during exposure and row readout is illustrated in Figure 1(b). Unlike the timing diagram shown in [2], GRST transistor which is used to globally clear the charges stored in PD is kept high before exposure.

Sensor Design
Because of the small pixel size, double pitch (5μm) readout circuits are placed on both top and bottom of the array. This helps to lower the routing constraints for column level power hungry blocks such as amplifiers and counters. In the mean time, it also allows larger space in layout for less electrical crosstalk among columns.

Figure 2 gives the image sensor architecture. Like many other Gpixel sensors, the pixel bus signal is first sent to a PGA for amplification and then sampled in the column S&H stage. This process happens simultaneously with previous row signals being converted into digital domain by the ADC array. CDS can be done both in analog (PGA) and digital (ADC). Odd columns will be readout through circuits on top and even columns will be readout through circuits placed at bottom side.

We have presented before the low power counting Ramp ADC in [3]. Two clocks counting can dramatically lower the power consumption of the counters but not the conversion speed. In order to reach the targeting speed of 150fps at 10-bit, both edges of the high speed counting clock need to be used. A modified lower power counting is incorporated to achieve this as like in Figure 3. Only a small change in the counter logic and a few extra counters are needed without doubling neither the area nor the power consumption as like in [4, 5]. Similar as in [3], signal MSB_EN and LSB_EN are generated for lower speed clock counting (CNT_MSB) and high speed clock counting (CNT_LSB). This LSB_EN signal is again delayed by rising and falling edge of the high speed clock, and a simple logic is added to generate extra bit counting which we called CNT_EB. Note CNT_EB has maximum of 4 pulses during each conversion so added power in counting is negligible. The final ADC value is given by equation (1) below.

$$DN = 2 \times K \times N_{CNT\_MSB} + 2 \times N_{CNT\_LSB} + N_{CNT\_EB} \quad (1)$$

While K is the frequency ratio of high speed counting clock CLK_H and low speed counting clock CLK_L. N_{CNT_MSB}, N_{CNT_LSB} and N_{CNT_EB} are the counter outputs of MSB, LSB and extra bit respectively.

Once counting finished, the counter outputs are then multiplexed and input to a data block to extract the final value of the ADC with equation (1). Besides, data block also handles the channel multiplexing, test pattern generation, and parallel to serial conversion, etc. Serialized data will then be sent out to the surrounding system though on-chip placed sub-LVDS drivers running at maximum 960Mbps.

Characterization

Figure 4 shows the image of fabricated sensor using TPSco 65nm CMOS image sensor process. The die is housed in 226-pin LGA package. Total size of the sensor is 22.3mm x 22.2mm, with optical center coincidence with the mechanical center. This allows for compact camera design. Figure 5 shows the horizontal and vertical angular response. More than 12^{o} at 80% peak QE can be achieved in both directions. Figure 6 shows the PLS degradation with different angles, given the fast readout speed, this sensor can be used for most of the industrial applications. Table 1 summarized the sensor specs. All performance are measured with x1 PGA gain, degraded noise performance in 10-bit is due to the higher bandwidth in readout circuits. Higher dynamic range can be achieved with higher PGA gain setting.

Conclusion

A 150fps high speed 25M GS image sensor was successfully developed and characterized. It integrates so far the smallest GS pixel with size down to 2.5μm. More than 6.5Ke- of full well can be achieved with PLS of -80dB for the developed sensor.

Acknowledgement

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Reference

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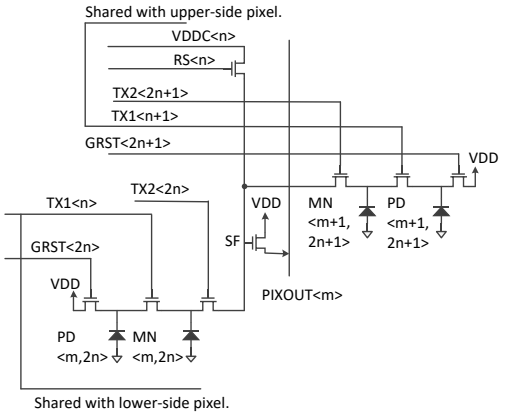
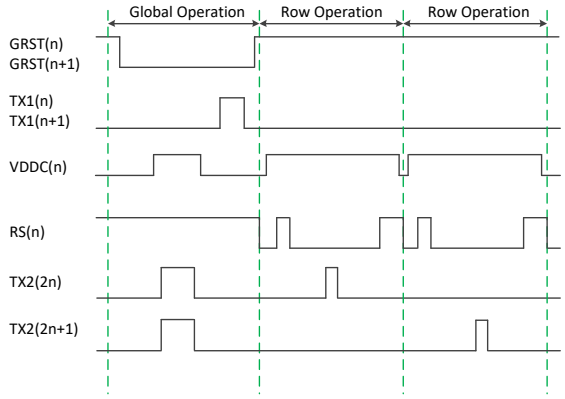
[5] J. Bogaerts, et al., “105x65 mm2 391 Mpixel CMOS Image Sensor with >78 dB Dynamic Range for Airborne Mapping Applications”, ISSCC, 2016: p. 114-115.



(a)



(b)

Figure 1 (a) Schematic and (b) timing diagram of the GS pixel

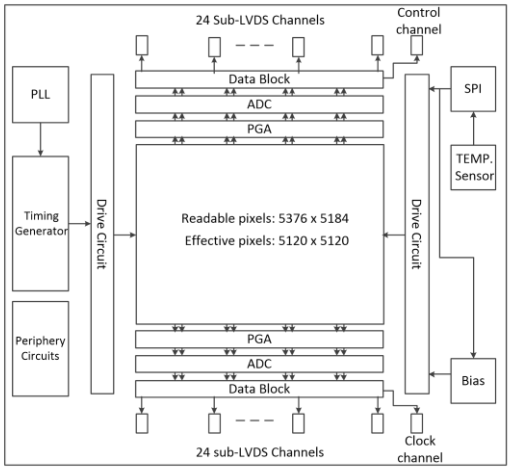


Figure 2 Image sensor architecture

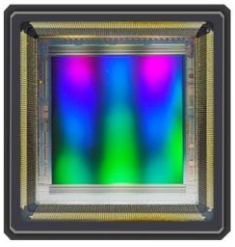
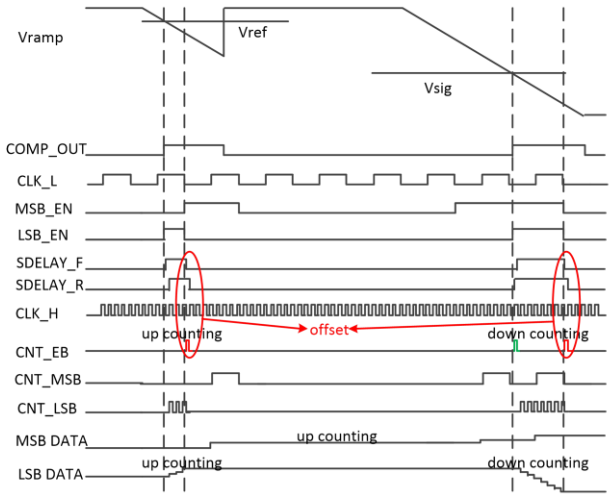
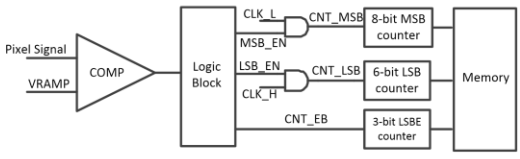


Figure 4 Image of the fabricated sensor



(a)



(b)

Figure 3 (a) Timing and (b) block diagram of the proposed double clock and double edge counting ADC

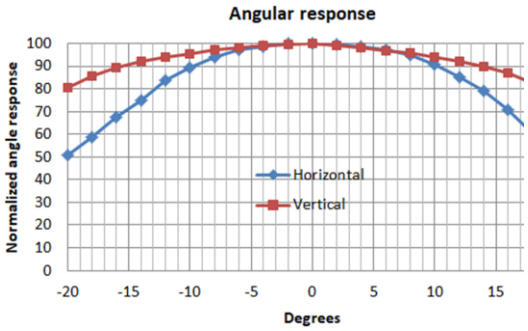


Figure 5 Angular response of the sensor

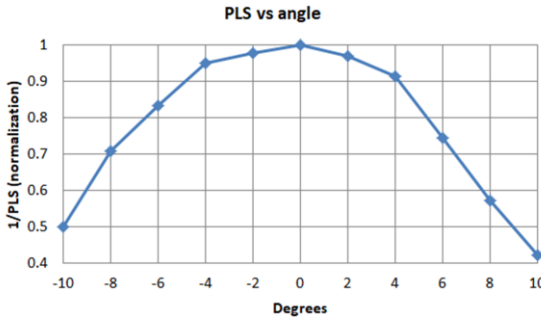


Figure 6 Angular dependence of PLS

Table 1 Image sensor performance summary with PGA gain set to x1

Parameter	**Value**	
Process	TPSco 65nm 1P4M CIS Process	
Pixel Size	2.5μm	
Supply voltage	3.3V/1.8V/1.2V	
PLS	< - 80dB(collimated light)	
Dark Current	<1e-/pixel/s @30°C die temperature	
Peak QE	65.5%（Mono@500nm）	
ADC Depth	10	12
Frame Rate	150fps	40fps
Read Noise	<9e-	<4.8e-
Full Well	>6.5Ke-	>6.5Ke-
Dynamic Range	>57.1dB	>61.4dB
Linearity	<0.6%	0.2%
FPN	20e-	2.5e-
PRNU	1.1%	0.7%
Power	<1.5W	<1.1W