A Small-size Dual Pixel CMOS Image Sensor with Vertically Broad Photodiode of 0.61 ㎛ **pitch**

Jungbin Yun¹, Kyungho Lee¹, Junghyung Pyo¹, Kyungduk Lee¹, Seungjoon Lee¹, Masato Fujita¹, Kyoung Mok

Son², Junseok Yang², Younguk Song², Hyejung Kim², Younghwan Park¹, Sungsoo Choi¹, Eun Sub Shim¹, Jeongjin

Cho¹, Seungjin Lee¹, Seogky Yoon¹, Sangil Jung², Takashi Nagano¹, Chang-Rok Moon¹, and Yongin Park¹

¹System LSI Division, Samsung Electronics Co., Ltd, ²Foundry Division, Samsung Electronics Co., Ltd.

Yongin-city, Gyeonggi-do, Korea. TEL:+82-31-8000-2428, e-mail:jungbin.yun@samsung.com

Abstract― We developed a CMOS image sensor (CIS) with phase detection auto-focus (PDAF) in all pixels. The size of photodiode (PD) is $0.61 \mu m$ by 1.22 μ m, the smallest ever reported and two PDs compose a single pixel. Our dual pixel shows a superior performance to the single pixel CIS by virtue of new technologies such as vertically broad PD, In-Pixel deep trench isolation (DTI) and the lossless optical grid, while supporting the accurate AF performance in the extremely low light of 1lux.

Introduction

As a result of growing demand of the higher resolution and the new functions of CIS, pixel structures evolved continuously. Furthermore various technologies have been developed in order to overcome the performance degradation and to improve the image quality from the previous or conventional pixels [1-3]. The dual pixel CIS, a CIS equipped with PDAF in all pixels offers the favorable solution for AF performance without defect correction of AF pixels [4]. However, as shown in figure1, the isolation region for the electrical and optical separation of AF signals leads to the smaller PD size/full well capacity (FWC) and

inevitable optical loss compared with the single pixel CIS.

Figure 1. Comparison of structure between single and dual pixel. (a) Optical separation and (b) PD layouts

In this paper, we have developed $1.22 \mu m$ dual pixel with superior performance compared with single pixel using the advanced process technologies.

Structure and performance of dual pixel

Advanced technologies have been developed in dual pixel structures to improve low FWC, high random noise (RN) and AF performance.

A. Full Well Capacity

First of all, we implemented vertically broad PD with 0.61 μ m pitch and ~2 μ m depth (Figure 2) to compensate the reduced PD area. The dual pixel structure consists of left PD and right PD in one microlens to output the PDAF signal, so the PD area decreased by about 20% compared with a single pixel. In order to overcome the low FWC, high-aspect-ratio photoresist (PR) and two-step patterning technique were developed. As a result, the ion implantation was optimized at $0.61 \mu m$ pitch to form a vertically broad PD well. This process development has improved not only FWC but also white spot (WS) through strong passivation of the DTI region. Vertically broad PD was optimized using TCAD simulation, and was confirmed by scanning capacitance microscopy (SCM) as shown in figure 3. In addition, boron implantation was implemented in maximum potential region of PD to optimize electron transfer and to extend the PD in a lateral direction. As a result, we obtained FWC of 7500e- which was 10% higher than the 1.22 μ m single pixel, and was comparable to $1.4 \mu m$ dual pixel, while we were able to maintain low WS level (Figure 4).

Figure 2. Vertically broad PD and lossless optical grid

Figure 3. (a) Doping profile and SCM image of vertically broad PD. (b) Comparison of potential profile between single and dual pixel

Figure 4. Comparison of (a) full well capacity and (b) white spot

B. Readout Noise

Secondly we changed readout scheme to reduce RN. Since the two PDs are divided into left and right signals, they necessarily read two signals separately for PDAF information. The conventional readout scheme requires two ADC data to obtain image signal (L+R) which resulted in increased temporal noise by $\sqrt{2}$ times. To avoid degradation of noise, we employed Reset-Signal-Signal (RSS) readout method. After reading the left signal, the right signal is read without further floating diffusion (FD) reset, and the signal is combined in the FD as L+R. Furthermore, the image signal is processed by one ADC, so there is no noise degradation in RSS method. The RN was maintained low level (Figure 5). And the PDAF information can be obtained from the calculation of the first signal (L) and the second signal (L+R), respectively, after the ADC. In addition, the engineering of source follower (SF) transistor was applied to reduce the random telegraph signal (RTS), and the RTS was obtained less than a single pixel, such as the result of the RN histogram.

Figure 5. (a) RSS readout of dual pixel CIS and (b) histogram of random noise

C. Quantum Efficiency and Auto-Focus performance

Finally, we improved our optical structure. The dual pixel CIS used In-Pixel DTI for optical separation between two PDs. In-Pixel DTI acts as the total reflection layer inside the silicon and increases the absorption of lights effectively. However, optical crosstalk is slightly increasing, so we are developing a new technology of In-Pixel DTI. With the lossless grid, the total sensitivity increases by 3% which results in the improvement of SNR 0.1dB compared with the single pixel (Figure 6).

Figure 6. Comparison of QEs

Angular responses in figure 7 show the AF performance of 0.61μm dual PDs for all channels. At the center of image, the AF contrast is about 3.5 at incident angle of 10 degrees, and the cross point of all channel is perfectly aligned to around zero. Also, at the edge of image, the cross point between dual PDs are perfectly aligned with each colors. In the case of no In-Pixel DTI, even though the focal point is adjusted to the Si surface at the edge of image, the cross point is different because the absorption coefficients of each colors in Si are different. However, our In-Pixel DTI can divide incident light of each colors in half. Therefore our dual pixel CIS delivers the better AF performance for all image area.

Figure 7. AF angular responses of (a) image center and (b) image edge

Conclusion

In summary, the smallest dual pixel CIS with $0.61 \mu m$ by 1.22 μ m PD was developed, which had superior pixel performances to $1.22 \mu m$ single pixel CIS (Table I). The vertically broad PD and lossless grid contribute higher FWC of 7500e- and SNR of 29.7dB, respectively. In addition, optimization of SF transistor and RSS readout keep the low RN of 1.7e- and improve RTS of <10ppm. These technologies can provide further development of scaled pixel with accurate AF performance.

Table I. Pixel performance summary

Characteristics	Unit	Single pixel	Dual pixel
FWC	$e-$	6800	7500
SNR	dB	29.6	29.7
WS	ppm	60	50
RN	$e-$	1.8	1.7
RTS	ppm	30	5
AF		N/A	3.5

References

[1] K. Lee, *et al., Int. Image Sensor Workshop*, 2011.

[2] JC. Ahn, *et al., Int. Solid State Circuit Conference*, 2014.

[3] Y. Kim, *et al., Int, Solid State Circuit Conference*, 2018.

[4] S. Choi, *et al., Symp. on VLSI Technology*, 2017.

[5] M. Kobayash, *et al., United States patent, 20140320690*, 2014