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Digital Pixel Image Sensors with Linear and Wide-Dynamic-Range Response Developed by Pixel-Wise 3-D Integration

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Abstract

We report a digital pixel image sensor developed by using pixel-wise 3-D integration technology. The pulse-frequency modulation (PFM) analog-to-digital converter (ADC) provides in-pixel digital output, which overcomes signal saturation due to the well capacity of a photodiode (PD). We have designed a CMOS image sensor (CIS)-type PFM-ADC suitable for pixels with a pinned PD. PDs, logic circuits, and counters were integrated into two silicon-on-insulator (SOI) layers via hybrid bonding using 5-μm-diameter Au electrodes. The developed sensor exhibited a linear and wide dynamic range response ranging more than 96 dB, demonstrating the high-fidelity image sensing. We also have developed triple-layer technology to further reduce the pixel footprint.

Introduction

The importance of CIS has increased with the development of image input devices for the Internet-of-Things era. Conventional CIS limits its dynamic range to approximately 60–70 dB [1] owing to the PD well capacity. Moreover, recent trends of shrinking pixels [2] further reduce the dynamic range. Pixel-level image sensing with PFM-ADC is a promising candidate for enhancing the dynamic range without PD saturation [3-4]. However, the large area of pulse counters degraded sensor resolution. To solve the problem, we have developed a pixel-parallel 3-D integrated image sensor as shown in Fig. 1 [5-8], which achieves both wide dynamic range and high resolution.

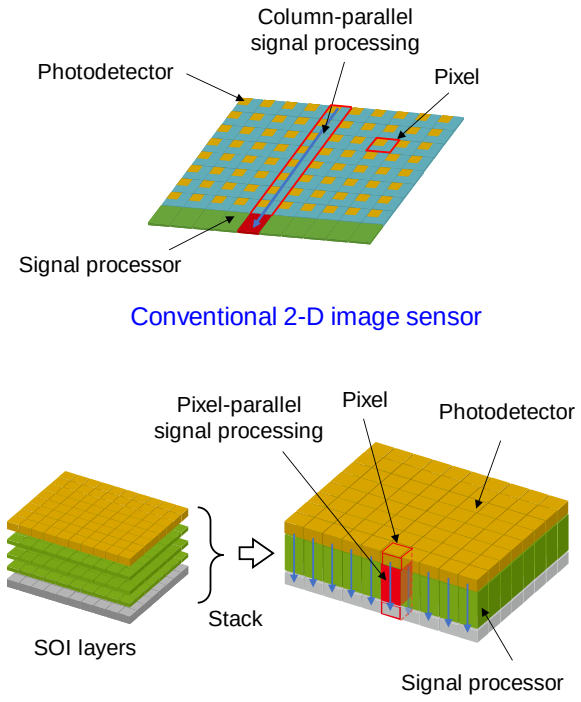
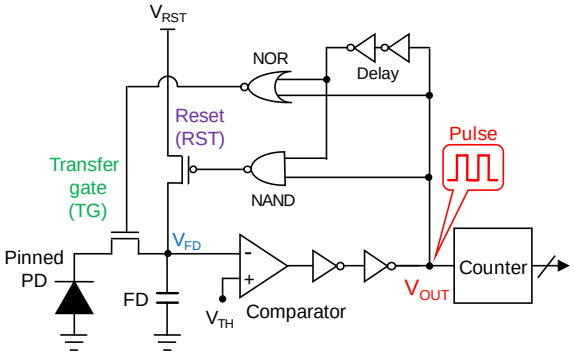


Figure 1: Pixel-parallel 3-D integrated image sensor compared with the conventional 2-D image sensor.

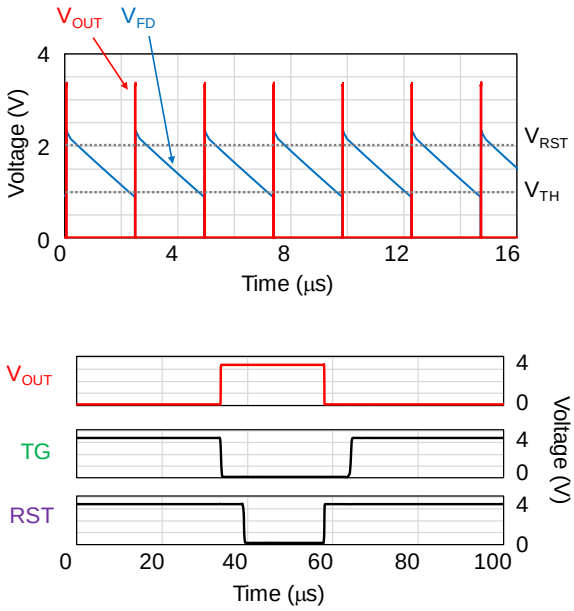
Design and Implementation

Figure 2 shows the newly designed CIS-type PFM-ADC. The transfer gate is switched ON during the charge storage period and OFF during the reset

period for the floating diffusion (FD) to keep the potential gradient between the PD and the FD. Logic circuits provides event-driven operation, which generates triggers for TG and RST by a pulse output signal. Figure 3 shows a schematic of the sensor. The upper PD and the logic array are developed by CIS process. The lower 16-bit counter array is by fully-depleted SOI process. All pixels are interconnected with Au electrodes via Au/SiO_2 hybrid bonding. Photographs of the developed sensor are shown in Fig. 4, which confirms 1-μm-alignment accuracy.

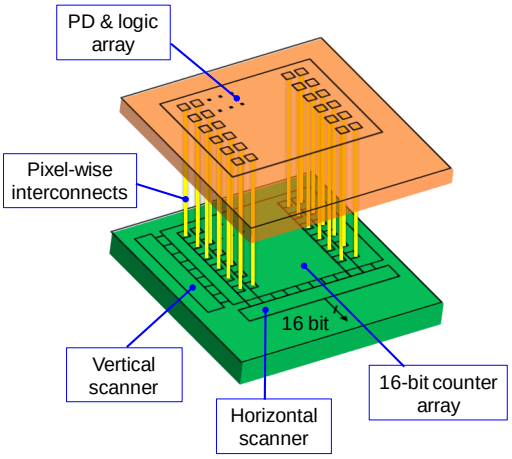


(a)

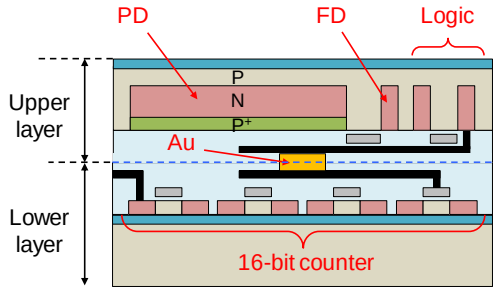


(b)

Figure 2: (a) Circuit diagram and (b) simulation results for CIS type PFM-ADC.

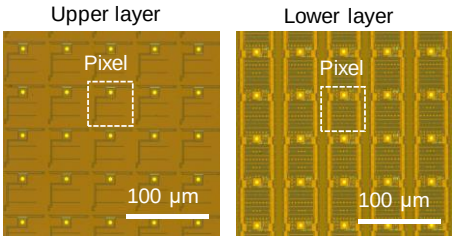


(a)

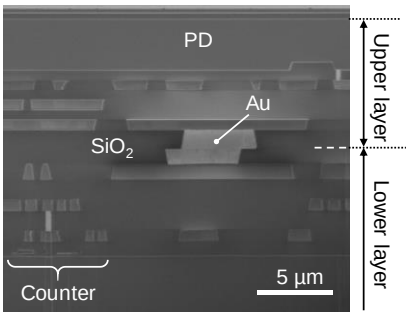


(b)

Figure 3: (a) Schematic of the 3-D integrated sensor and (b) cross-sectional diagram of the pixel.



Before bonding

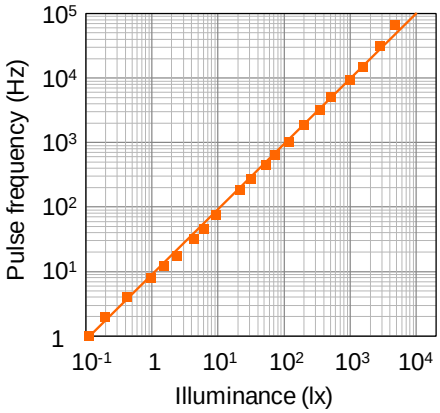


Cross-sectional interface of bonded chip

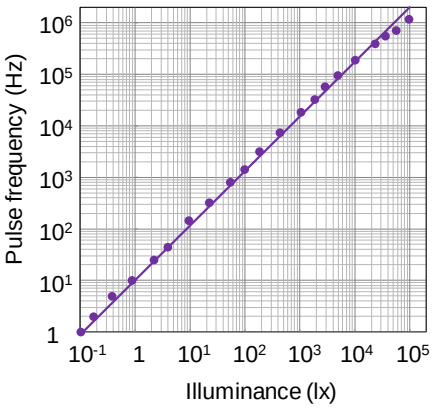
Figure 4: Photographs of the developed sensor.

Measurement Results and Discussion

Figure 5 shows the measured output of the sensor as a function of the illuminance. We confirmed an excellent linearity and a wide dynamic range of 96 dB as shown in Fig. 5 (a), which corresponds to the in-pixel 16-bit counter. The response was also examined using an off-chip 20-bit counter, showing a wider dynamic range of 120 dB as shown in Fig. 5 (b). Figure 6 shows captured images. Figure 6 (a) shows a 256-gradation image from the lower 8-bit signals, whereas Fig. 6 (b) is from the higher eight bits. Figure 6 (c) shows a 256-gradation image composed from the above two images after histogram equalization, thereby demonstrating the ability for capturing the full range of illuminance.



(a)



(b)

Figure 5: Measured output of the developed sensor by using (a) in-pixel counter and (b) off-chip counter.

(a)

(b)

(c)

Figure 6: Examples of captured images. (a) Image from lower 8 bits. (b) Image from higher 8 bits. (c) Composed image after histogram equalization.

The SOI-based 3-D integration can increase the number of stacked layers to increase the resolution and to improve multifunctionality. We are now developing triple-layer sensors, wherein 16-bit counters are separated into two layers, whose schematic and simulation results are shown in Fig. 7.

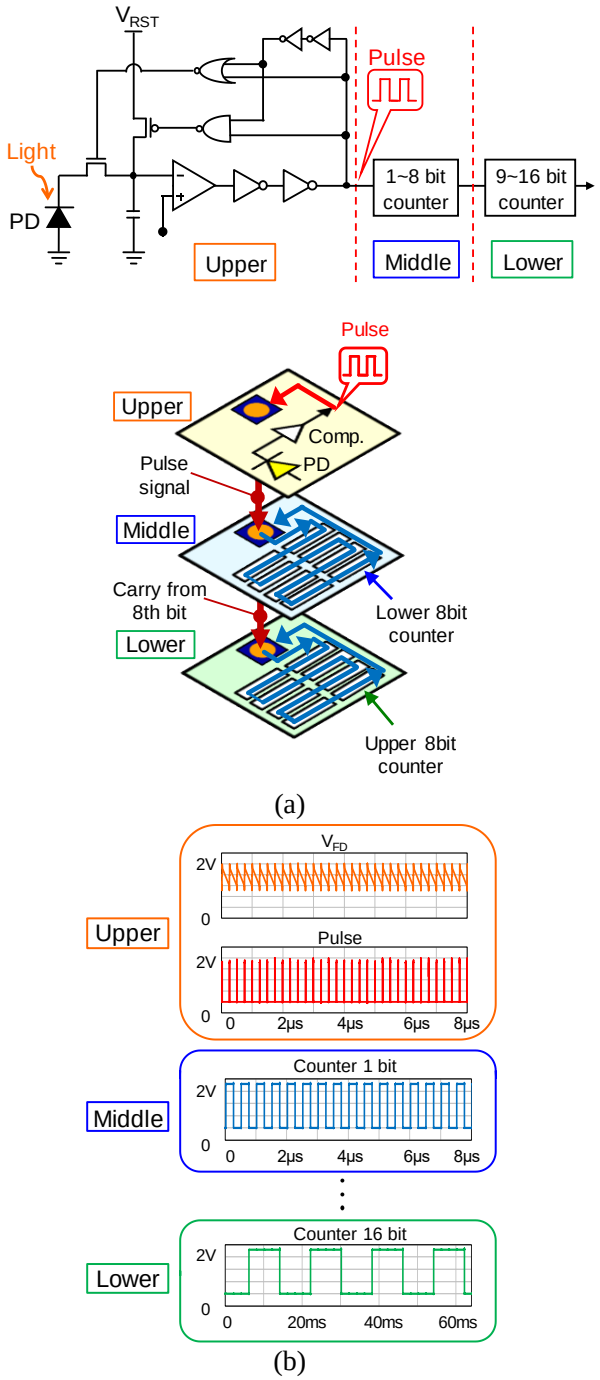


Figure 7: (a) Schematic and (b) simulation results of pixel for the triple-layer sensor.

Conclusion

We developed digital pixel image sensor by using in-pixel PFM-ADCs and pixel-wise 3D integration. Measurement results demonstrated both linearity and a wide dynamic range of more than 96 dB. The sensor is promising for next-generation video systems because it can capture precise information in the real world.

References

[1] J. Ohta, Smart CMOS Image Sensors and Applications. Boca Raton, FL, USA: CRC Press, 2007, pp. 187–188.

[2] P. Chou *et al.*, "A 1.1μm-Pitch 13.5Mpixel 3D-Stacked CMOS Image Sensor Featuring 230fps Full-High-Definition and 514fps High-Definition Videos by Reading 2 or 3 Rows Simultaneously Using a Column-Switching Matrix," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, pp. 88–90, Feb. 2018.

[3] W. Yang, "A Wide-Dynamic-Range, Low-Power Photosensor Array," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, pp. 230–231, Feb. 1994.

[4] F. Andoh, H. Shimamoto, and Y. Fujita, "A Digital Pixel Image Sensor for Real-Time Readout," IEEE Trans. Electron Devices, vol. 47, no. 11, pp. 2123–2127, 2000.

[5] M. Goto *et al.*, "Three-Dimensional Integrated CMOS Image Sensors with Pixel-Parallel A/D Converters Fabricated by Direct Bonding of SOI Layers," in *IEEE Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 2014, pp. 4.2.1–4.2.4.

[6] M. Goto *et al.*, "A Three-Dimensional Integration Technology with Embedded Au Electrodes for stacked CMOS Image Sensors," in *Proc. 2015 Int. Image Sensor Workshop (IISW)*, 2015, pp. 48–50.

[7] M. Goto *et al.*, "Quarter Video Graphics Array Full-Digital Image Sensing with Wide Dynamic Range and Linear Output Using Pixel-Wise 3D Integration," in *IEEE Int. Symp. Circuits and Systems Dig. Tech. Papers (ISCAS)*, pp. 1–4, 2018.

[8] M. Goto *et al.*, "Quarter Video Graphics Array Digital Pixel Image Sensing With a Linear and Wide-Dynamic-Range Response by Using Pixel-Wise 3-D Integration," IEEE Trans. Electron Devices, vol. 66, no. 2, pp. 969–975, 2019.