Several Process Techniques & Pixel Source Follower Schemes to improve the Pixel Temporal Noise

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Abstract— **Several Process Techniques are introduced to improve the Pixel Temporal Noise. These techniques focus on the Pixel Source Follower Transistor. The first is to apply the Fluorine Implantation, and through this process, the Blinking pixels are decreased so effectively. The second is to add the UV curing process. This process decreases the Dit in whole pixel transistors and photodiode but the noise improving effect becomes less than expected. The third is to use the LPRO (low pressure radical oxidation) process. This process is known as an effective method to make the uniform oxide thickness and to decrease the Dit in the oxide trap due to the radical ions. But different from the expectation, the noise performance was not much improved comparing with the PNO-Gox case. The forth is the Thin Gate Oxide Source Follower. This is the most economical and simple (=No additional process) technique. The thinner gate oxide promises the better noise performance, basically independent on its threshold voltage. Using TnTk and TkTn SF Tr. scheme, the Noise analysis was done additionally and the best case was TnTk SF Tr. case.**

Keywords- Fluorine implantation, UV curing, Thin Gox Source Follower, Pixel Temporal Noise, Blinking Pixels, TkTn & TnTk SF

I. INTRODUCTION

The Temporal Noise in CMOS image sensor is the problem for a long time and so many improving methods have been suggested. The importance of the Temporal Noise and the Blinking pixel performance is because this temporal varying noise cannot be removed perfectly by the circuit-based removing architecture and so the noise makes worse the pixel dynamic range. So the effort to minimize the noise in process viewpoint is much meaningful.

This Temporal Noise results majorly from the Source Follower in the pixel, Fig.1, and basically, results from the RTS (Random Telegraph Signal) noise of this transistor [1]. Many trials have been reported to minimize the Temporal Noise by tuning of the Source Follower transistor size dependency [2]-[4]. Gate Oxide tuning process is also suggested and the conceptual explanation on this effect is explained [5]. Fig. 2 shows our own experiment result between NO-Gox and PNO-Gox process by using the Noise Histogram method. Thanks to the PNO-Gox process, the rms noise value and the Blinking pixels are improved clearly.

[5] explained the dependency of the Temporal Noise on the Source Follower's threshold voltage and so the lower threshold voltage is efficient for the noise performance, especially, in the Blinking pixel suppression. Lower Vth makes the lower voltage between the Drain and the Source in SF and so the maximal electric-field in the channel is decreased. Due to this, the probability of the electron carrier trapping to the Oxide imperfection becomes small. As an extreme case, [6] reported the Native (~0V Vth) Source Follower transistor to minimize the Temporal Noise and the Blinking pixel. And also the Buried Channel scheme is reported in Source Follower to minimize the NMOS's surface scattering [7]. PMOS-based Pixel also is reported for the same goal [8-11].

In this paper, four different techniques are introduced to improve the Pixel Temporal Noise. The first is the Fluorine Implantation and the 2nd is the UV curing process and the 3rd is the LPRO gate oxidation and lastly the Thin Gox Source Follower scheme. The 1st and 4th are only for SF and 2 items are for all devices.

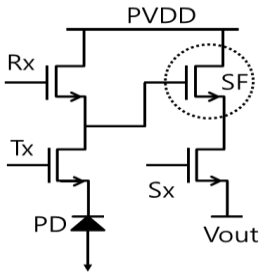

Fig.1. General 4Tr. NMOS-based Pinned APD Pixel Schematic with in-pixel Source Follower

II. EXPERIMETAL

A. *Fluorine Implantation*

Fig.2 shows the Noise Performance of the Nitrided-Oxide Gate Oxide case (NO-Gox) and Plasma Nitrided-Oxide Gate Oxide case (PNO-Gox). It shows the clear improvement in the rms noise and the Blinking pixels over some threshold level. All 4 kinds of technique are also adopting the PNO-Gox process basically in 0.11um CIS Foundry process of DB HiTek.

The Fluorine Implantation was introduced at [12, 13] firstly with the process and analysis. The representing result is the Fig. 3 and the Blinking pixels are decreased clearly. This results from the 1/F and RTS noise suppression in SF by adopting the

Fluorine implantation to the SF transistor selectively. The additional result was introduced at Fig.3. The splits are when the Fluorine implantation is applied to the whole pixel block and when it is applied to the SF ONLY. There are no remarkable difference between 2 splits and so this is another evidence to show that the main part of the noise is from the SF. But in general CIS process, there is the mask to open the whole pixel block, this mask is economical to use for the Fluorine implantation after the Gate Poly deposition.

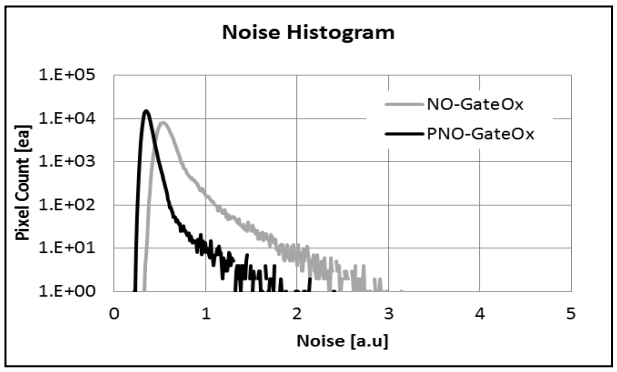

Fig.2. The Temporal Noise histogram from NO-Gox and PNO-Gox case (400x400 pixels). Vth of the Source Followers are same from 2 cases as 0.4V. (Product1: W/L=0.5/0.4um^2).

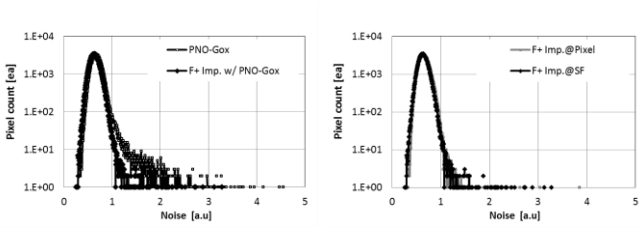

Fig.3. (a) The Temporal Noise histogram from PNO-Gox and PNO-Gox with F+ implantation case (400x400 pixels). Vth of the Source Followers are same from 2 cases as 0.25V. (Product2: W/L=0.244/0.275um^2). (b)F+ Imp. at SF and at Pixel show nearly same Noise performance.

B. UV Annealing Process

The 2nd is the UV curing process having 254nm (4.9eV) UV lamp. This process can be done after the general forming gas annealing additionally [14]. When the SiN layer is etched out or makes the cavity structures in the next to improve the sensitivity, the wafer suffers from the plasma damage and to cure this damage, the UV curing process helps to make lower and stable dark performance. [15]

By using the 1.75um pixel Tx-PD array structure, we have tested the charge pumping current and the UV curing case showed about 3~4 times lower Icp and so the Dit. But this Tx-PD structure is fully different from the normal MOS transistor; there are 2 or 3 regions of Si-SiO2 interface. One is the Tx channel interface and another is the Pinning layer Si-SiO2 interface on the PD Silicon surface. The 3rd is the pinning layer Si-SiO2 interface in the PD STI sidewall region. When the UV curing process added, the Tx transistor performance shifts to Slow, that is, higher Vth and lower Idsat as about 30%. To check the reason of this performance shift, we have checked the resistance of each implantation layer, that is, PDN, PIN, STI imp. at the real PD structure with suitable length. From Table1, the only changed part is the PIN layer and decreased resistance. This will be due to the electron injection from Silicon to SiO2 by UV bombardment. The negligible shift of SF performance also testify that this reaction happens mainly at the PIN Si-SiO2 interface, at least, more than at Tx channel interface, and so these electrons cure the Q_f & Qit (positive charges) in Oxide on the PD region and so the hole density in the PIN layer increased and so the resistance of PIN layer goes down. Finally, the Tx performance is shifted to Slow, but strictly speaking, this is not the Tx performance shift. This is the Pinning layer performance shift. These cured or accumulated holes in PIN layer suppress the probability of trapping the PD electrons and so better dark performance. The dark performance variation also become much stable when UV curing process is adopted and but, as a contrary part, the Lag can be worse slightly.

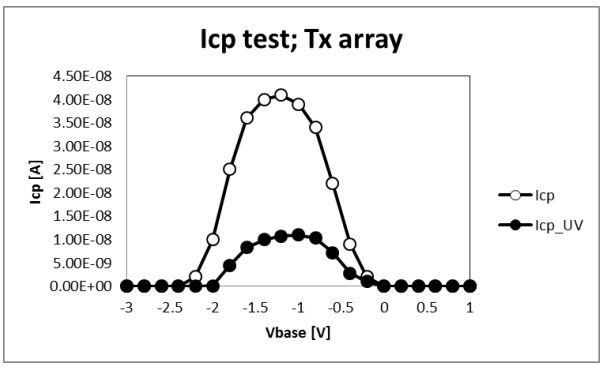

Fig.4 Comparison of charge pumping current with respect to splits. 1.75um pixel Tx-PD array (2,700ea) is used.

Table1. Performance Shift after UV curing

Device	Parameter	Skip	UV Curing	Diff.%
HV STD nMOS	Idsat	4.68mA	4.64mA	-
Tx Unit	Idsat	11.21uA	7.90uA	**-29.5%**
	Vth	1.26V	1.75V	**31.0%**
SF Unit	Idsat	142.2uA	139.9uA	-1.6%
	Vth	0.38V	0.37V	-2.6%
PDN (n-type w/ PIN.)	Resistance	9380	9842	**4.9%**
PIN (p-type imp.)	Resistance	27702	26533	**-4.2%**
STI (p-type imp.)	Resistance	2919	2912	-0.2%

Low incident angle of UV curing condition can induce the channel interface Dit immunity improvement and this was confirmed from [15]. To check the contribution of this process to the noise, the temporal noise test was done using the pixel SF as 0.18x0.32um size with Vth 0.37V. Fig. 5 is the result and the Blinking pixels decrease near 2 times. But when considering the Dit improvement in [15], the Noise improvement is lower than expectation. And this means again that the Dit improvement in Tx array test happens majorly at the PIN Si-SiO2 interface, not the Tx channel interface.

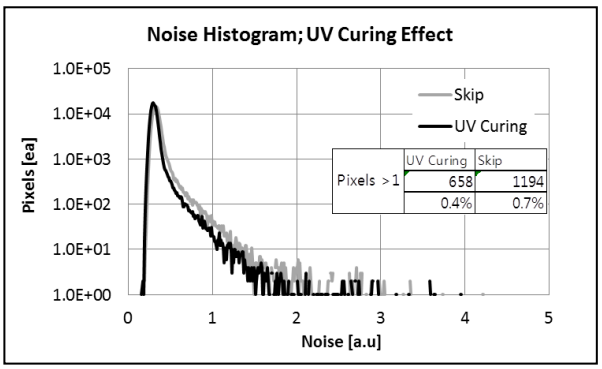

Fig.5. The temporal noise histogram of UV curing split. (Product3: SF W/L=0.18/0.32um^2, 0.37V, 400x400 pixels).

C. Low Pressure Radical Oxidation(LPRO) Process

The Hydrogen-assisted LPRO process was studied firstly to improve the CIS noise performance. Similar with the ISSG (In-situ Steam Generation) Oxidation, this LPRO oxidation gives more uniform thickness on all Silicon directional surfaces. Because of this, this process is usually used at the tunnel oxide in Flash memory and EEPROM process [17].

This oxide layer is known as lower Dit thanks to the thinner and better roughness of Si-SiO2 interface. And also the reliability performance is also better than general thermal oxide.

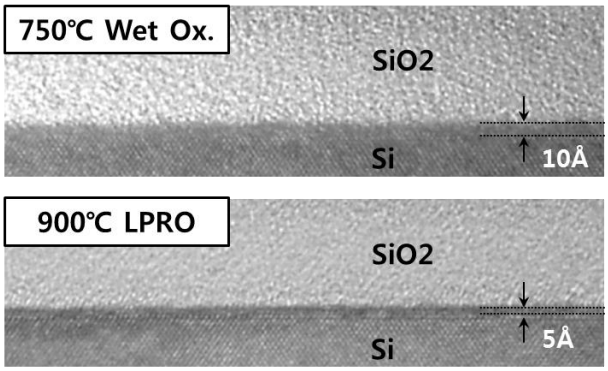

Fig.6. TEM inspection of Si-SiO2 interface for each Oxidation process. This process was used for thick Gate Oxide formation.

To check the effect on the Noise of CIS, LPRO process at 900C was done and the Logic Transistors were tuned to meet the typical performance. Fig.7 shows the Noise histogram and the Blinking pixels are reduced slightly as about 2 times lower. But this is also very small improvement compared to the effort.

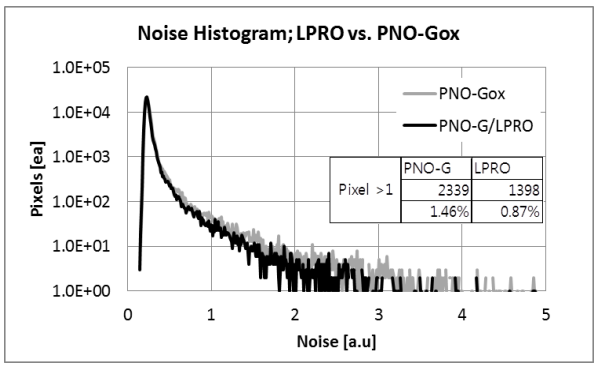

Fig.7. Noise Histogram with the Gate Oxidation splits (Product4: W/L=0.244/0.350um^2, 400x400 pixels).

D. Thin Gox Source Follower [18]

The best and economical method to improve the noise performance is to make the Source Follower as thin Gate Oxide. This method can be imagined so easily when the Eq.1 is considered (typical long channel case). Simply, to suppress the 1/f noise portion (that is, the RTS noise portion), the wider and longer device is more efficient and the higher Cox, that is, the thinner Gate Oxide is also very effective method. This scheme can be realized basically at dual gate oxide process.

$$\frac{\overline{V_n}^2}{\Delta f} = \frac{\overline{V_{n,1/f}}^2}{\Delta f} + \frac{\overline{V_{n,Johnson}}^2}{\Delta f} = \frac{K_F}{WL \cdot C_{ox}} \frac{1}{f} + \frac{2}{3} \cdot \frac{4kT}{g_m} \quad \text{--- (Eq.1)}$$

$$\frac{K_F}{WL \cdot C_{ox}} \frac{1}{f} = \frac{2}{3} \cdot \frac{4kT}{g_m} \quad \text{--- (Eq.2)}$$

$$f_{co} = \frac{K_F}{WL \cdot C_{ox}} \cdot \frac{3g_m}{8kT} = \frac{K_F}{4kT \cdot C_{ox}} \frac{1}{L} \left(\frac{g_m}{I_D} \right) \left(\frac{I_D}{W} \right)$$

But before adopting this thin Gate Oxide Source Follower scheme, the Gain Characteristics should be considered carefully. Fig.8 shows the SF Tr. and Row Select Tr. (Sx)-based circuitry. Typically, the relation between the SF and Sx's threshold voltages and SF gain characteristics were introduced so clearly at [5]. The SF gain characteristics shows the Band Pass filter shape and the gain drop point in lower region is related to the operation of the column bias circuit from the saturation region to go the cut-off region due to the lower Vfd. And this also depends on the SF's Vth. The gain drop point in the upper region depends on the Sx's Vth comparing with the SF's Vth. When Sx Vth > SF Vth, the gain drop happens at lower Vfd due to the higher SF's source voltage. To make more flat gain in Vfd.rst region, the Sx's Hi (ON) voltage should be set higher by the additional block, for example, the positive charge pump circuit. Sx's Vth have the lower limitation to prevent the off-leakage. Sx's off-leakage can induce the column line failure. Finally, to make higher & more flat gain from Dark to Saturation of optical image, the lower SF Vth is necessary and but for this, the relation and limitation with the Sx and column bias circuit should be considered firstly and carefully. In this report, 3.75V was used as Sx's Hi voltage because SF Vth decreased from 0.30 to 0.0V nearby when the SF is changed to thin Gox transistor.

Fig.9 shows the SF gain curve of Thick and Thin Gox SF cases. When the Vfd.rst is near 2.6~2.8V, the flat gain is near 0.95V/V and higher than the thick Gox case as 0.89V/V. Because of lower Vth of thin Gox SF, the gain drop point goes down but the gain flatness is enough.

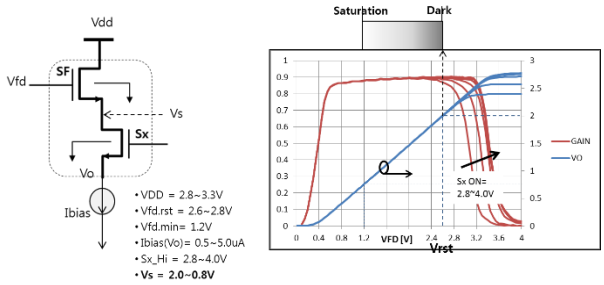

Fig.8. The SF-Sx circuit with typical bias condition. Its gain characteristic shows the Band Pass Filter shape.

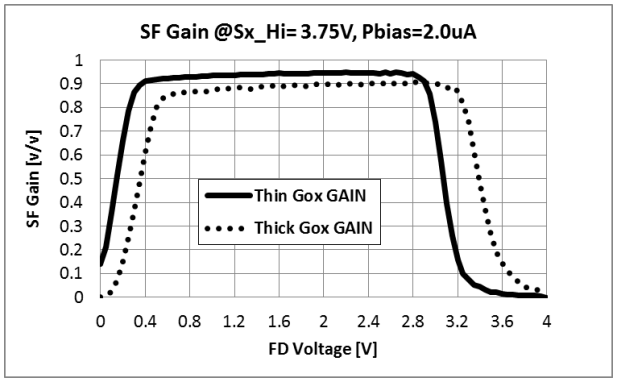

Fig.9. The Gain & Vout measurement of SF-Sx circuit with Sx Hi 3.57V and external current bias as 2.0uA. SF Tr. Vth = 0.30V at thick Gox & 0V at thin Gox case.

The temporal noise performance is measured using the typical method at Gain x8 and Fig.10 shows the comparison between thick Gox SF and thin Gox SF. The noise performance is dramatically improved and so much smaller Blinking pixels in thin Gox SF case. Because the thin Gox SF with 0.3V Vth case (adding the Vth tuning imp.) shows the same noise performance with 0V case, this improving noise portion is from the Gox thinning, not from the lower Vth. And, Fig.11, when the Fluorine implantation was added, the Blinking pixels are decreased additionally even at the Thin Gox SF. Thin NMOS SF is effective even in NO-Gox process, too, but not better than PNO-Gox process case. This is because the Plasma oxidation process has been done after the Thin Gate Oxidation process, usually.

But from the more exact inspection, the mode value of noise histogram at the thin NMOS SF case is always slightly higher than thick NMOS SF and this is also the problem. This is from the slightly lower conversion gain and to check this issue, SF scheme was split as the dual gate oxide, so called, TnTk SF and TkTn SF (incident figure in Fig.12). Fig. 12 shows the 4 cases and the best case is the TnTk NMOS SF case. This scheme shows the lower mode value and also smaller blinking pixel than TkTn SF and Thin SF cases. That means the main Trap-Detrap process of electrons happens at the Drain region of the SF mainly and so the thinner Gox (and lower Vth) at the Drain region contributes to the temporal noise and thermal noise at the same time.

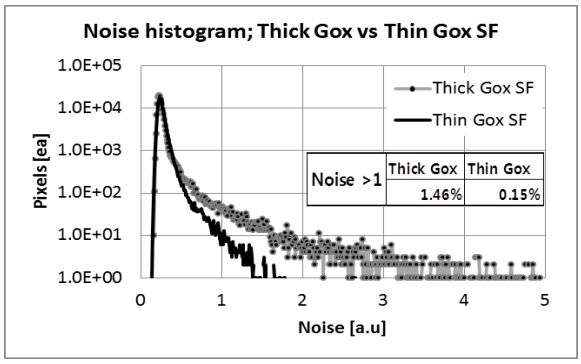

Fig. 10. Noise Histogram with thick Gox and thin Gox SF splits (Product4: W/L=0.244/0.350um^2, 400x400 pixels).

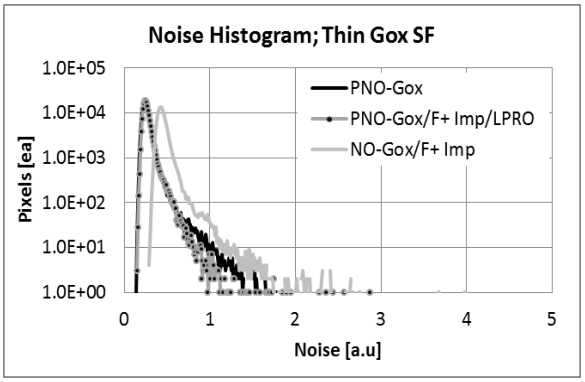

Fig.11. Thin Gox SF with process splits (Product4: W/L=0.244/0.350um^2, 400x400 pixels).

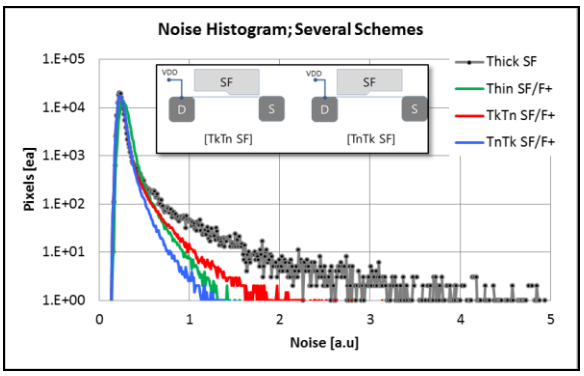

Fig.12. Several SF scheme with process splits (Product2: W/L=0.244/0.350um^2, 400x400 pixels).

Because the Thin Gox SF did not need any additional mask and photolithography process, this scheme is the most effective and economical method to improve the noise performance. [10] & [11] introduced the thin Gox PMOS SF transistor scheme. Because of PMOS's better noise performance, the read out noise can be better than thin NMOS SF pixel. But their pixel size is larger over than at least 5um and this is because the NWELL process should be included in the NMOS PD region. Therefore this is a little uneconomical and uncompetitive to the smaller pixel.

III. CONCLUSION

In this report, several methods to improve the noise performance and the Blinking pixels are introduced. The PNO Gate Oxidation, UV curing, and LPRO oxidation methodology do not have the selectivity in case of Source Follower. The Fluorine Implantation and the Thin Gox SF scheme is the selective action to improve the noise performance.

All methods are helpful to improve the noise but the best way is to make the Thin Gox SF. This method is very simple and economical even for small pixels and so not need the additional process or the change of it. TnTk SF showed the best noise performance and so the Drain edge region is much important in Noise view point. When the Fluorine implantation was added in this Thin Gox SF, the noise performance became better additionally.

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