CMOS Image Sensors and Plasma Processes: How PMD Nitride Charging Acts on The Dark Current

Y.Sacchettini[1,2], J.-P. Carrère[1], R. Duru[1], J.-P. Oddou[1],V.Goiffon[2] and P. Magnan[2],
1. STMicroelectronics, 850 rue Jean Monnet, 38926, Crolles, France
2. ISAE-SUPAERO, Université de Toulouse, 10 av Edouard Belin, 31055, Toulouse, France
Tel : +33-438922628 ; e-mail : yolene.sacchettini@st.com

I. INTRODUCTION

The dark noise of the CMOS image sensors can be affected by plasma process steps, either by purely electrical stress [1] or by the combination of photon interaction and electrical stress [2]. Focusing on the impact of a dry strip step, we study here how the dark current in a FSI sensor is linked to the interface damages and the nature of the charges appearing in the Pre-Metal-Dielectrics (PMD) stack during the plasma exposition. To characterize the impact of plasma processes, the potential and the charge are characterized in these dielectrics using the Corona Oxide Characterization Of Semiconductor (COCOS) technique [3]. Then, TCAD simulation will illustrate the link between dark current and the results on the dielectrics characterization.

II. DARK CURRENT DEGRADATION BY PLASMA STRIP

The device studied is a FSI CMOS image sensor with 4.1µm pitch, 4T pinned N-photodiode pixels. To improve the optical path and the quantum efficiency of the pixel, a cavity is etched before the color filter and microlens patterning. The pixel configuration is shown in Fig. 1. The number of silicon nitride (SiCN) layers kept between the photodiode and the cavity has been varied from none to three. Two strip plasma processes after the cavity etch are compared. The first one is a high density oxygen plasma made by a magnetic enhanced etch reactor and referred to as "strip A". The second is done in a dedicated stripping tool with a remote plasma, referred to as "strip B".

Fig. 2 shows that "strip A" induces a significant increase of active pixel dark current, while "strip B" prevents any damage, thus, matching the current of reference dark pixels, shielded by metal. This indicates that "strip A" is the cause for degradation and so it will be used as a study case thereafter. The dark current degradation decreases with the presence of SiCN layers, as shown in Fig. 3. Furthermore, there is no influence on damage of the pixel design, like the deep or shallow trench perimeter, the poly transfer gate length, as shown in Fig. 4. From these two observations, the dark current source for degraded pixel seems to be, mainly, the interface above the photodiode, under the Pre-Metal-Dielectrics (PMD) stack.

III. PLASMA IMPACT ON DIELECTRIC: EXPERIMENTAL SETUP AND RESULTS

To better understand the interactions between plasma and the dielectrics located above the pixel, we deposited, on unpatterned wafers, one or several layers of the studied stack illustrated in Fig. 5, and exposed them to the "strip A" plasma. We used a p-doped substrate at a 1×10^{15} cm^{-3} concentration. The samples are described in Table 1. Then, the samples were characterized by Kelvin probe measurements (Fig.6) and the COCOS technique [3]. Measurement of photoluminescence intensity in the 900-1300 nm band was also performed.

TABLE I. SAMPLES DESCRIPTION: DIELECTRIC TYPE AND THICKNESS DEPOSITED.

Sample number	Dielectric stack
1	Thin Bottom Oxide
2	Anti Reflective Nitride 50nm
3	Oxide 500nm
4	Thin oxide + Nitride 50 nm
5	Oxide + Nitride + Oxide

After the plasma exposure, the potential at the surface of the dielectric stack (V_{CPD}) increases, as illustrated in Fig. 7. The samples with nitride layers exhibit both polarity voltages whereas the samples with only the oxide layer show only positive ones. The potential mapping, shown in Fig. 8, indicates a clearly non-uniform process. This non-uniformity creates positive charges at the wafer center and negative charges at the edge of the wafer, as shown in Fig. 10. The measurement of the silicon barrier potential, Vsb, illustrated in Fig. 9, highlights that these charges can accumulate or deplete the p-substrate under the dielectrics, as in Fig. 11. This mapping illustrates that there are enough positive charges at the center to inverse the silicon and in the edge enough negative charges to have an accumulation. Furthermore, the silicon barrier measurement was carried out 48 days after the plasma exposure. After this delay, the surface potential, V_{CPD}, decreased as shown Fig. 12b. compared to previous results in Fig 7. For sample 5 with the thick oxide on top, it went back to positive potential even lower than initial ones whereas the sample 4 still have both polarity voltages. However, the silicon barrier measurement shows similar results for the two samples. We can

deduce from these observations that there is about the same equivalent interface charge (seen from the silicon) in sample 4 and 5, that it is mainly originating from the nitride layer, and that the thick oxide layer on the top of sample 5 is screening this charge when measuring V_{CPD}.

The measurement of photoluminescence in the 900-1300nm corresponds to the band to band emission in the silicon. The intensity of this signal decreases when the non-radiative recombination increases. Hence, this measurement allows to estimate the density of recombination centers, and thus the intensity of the dark current generation. In our samples, we can assume that the signal is only modulated by the recombination at the interface between the silicon and the dielectric of the sample. Fig.13 shows that for the sample 4, the photoluminescence intensity is high at the center of the wafer and low for some spot in the edge. This result is well correlated with the fact that in the center we have an SiO2/Si interface in inversion, highlighted by the Vsb results, with a low recombination rate. The measured spots with an interface in accumulation show also a high photoluminescence intensity whereas those in depletion, have a weak signal, in good agreement with previous study [4].

IV. Discussion: Plasma Interaction Mechanism

The dielectric stack characterization indicated that the plasma process induces a buildup of trapped charge in the nitride layer. It has been previously shown [5] that silicon nitride can trap both charges polarity by applying an electrical stress via corona charging. However, in our case, due to the fact that the presence of SiCN layers modulates the degradation and that shielded pixel are unaffected, it is unlikely that a pure electrical stress is causing the charge trapping. UV radiation can generate charge in the nitride [6] or in the silicon oxide [7] and can increase conductivity in the dielectrics [8]. These phenomena associated with the electric field induced by the non-uniform plasma allows the trapping of either positive or negative charges, as illustrated Fig. 14, similar to what is obtained in silicon-nitride structures exposed to ionizing radiation with polarization applied [9]. Furthermore, band energy configuration in the PMD dielectric stack helps the charge trapping in nitride. The silicon dioxide is actually a barrier for both electrons and holes, as illustrated Fig. 9.

The positive charge in the nitride causes the dark current increase. Indeed, we have shown a clear correlation between the spatial distribution of the total charges and the value of dark current, as illustrated in Fig. 15. A 6×10^{12} cm^{-2} charge allows to deplete or even weakly inverse the photodiode pinning p-layer close to the silicon-oxide top interface, as shown by TCAD simulation in Fig. 16. The depletion region extends under the spacer of the gate, or at STI and DTI interfaces. According to the SRH theory [10], dark current generation is maximum at depleted interface, explaining the large measured dark current. Finally, the high photoluminescence intensity at the wafer center shows that for samples with a lower p doping, the interface under the positive charge is fully inverted, which blocks the SRH recombination during the measurement.

V. Conclusion

We have seen that an oxygen plasma strip can induce a large increase in the dark current of a FSI sensor pixel. By characterizing dielectrics stack after plasma exposure, we identified that positive and negative charges were trapped mainly in the PMD nitride layer. These trapped charges are modifying the oxide/silicon interface passivation, and the generation activity, as highlighted by Vsb and photoluminescence measurement. In particular, depletion of the interface induced the large dark current increase. The good correlation between the results obtained on the dielectrics characterization, the measured dark current, and the TCAD simulation validates the proposed mechanism.

References

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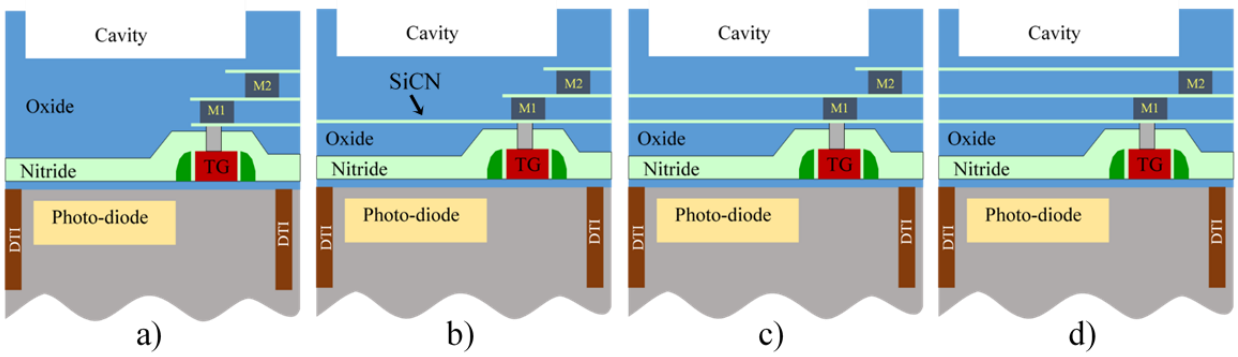

Figure 1 Schematic representation of the pixel cross section for a) the standard process, with 1 (b), 2 (c) or 3 (d) layers of SiCN left above the pixel and under the cavity.

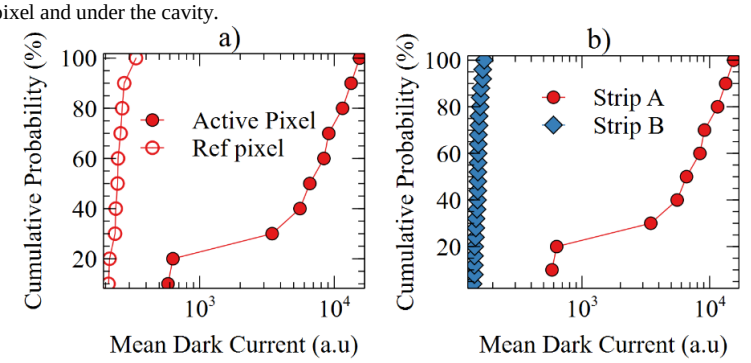

Figure 2 Mean dark current for a) active pixel of the matrix and dark reference pixel processed with strip A, b) active pixel process with the two cavity strip processes used in this study. "Strip A" is a high density oxygen plasma created in the cavity etch reactor and "Strip B" is done in a dedicated stripping tool with a remote plasma.

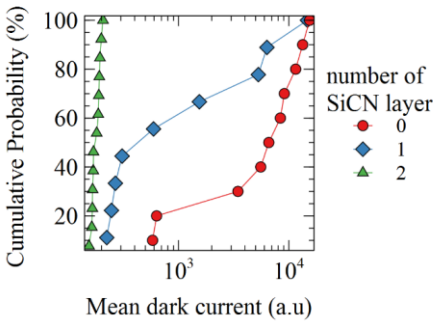

Figure 3 Mean dark current for active pixel of the matrix with varying number of SiCN layers between the photodiode and the cavity and processed with "strip A".

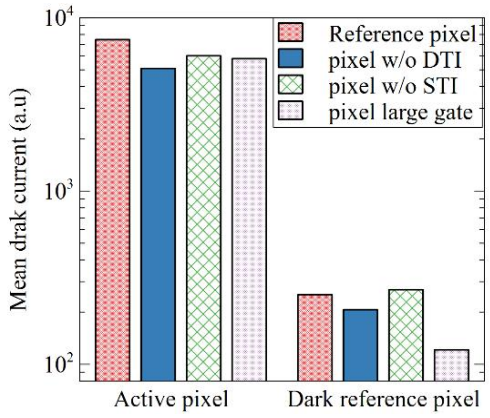

Figure 4 Mean dark current for active pixel of the matrix and dark reference pixel processed with "strip A" . Comparison of four pixel version, the reference pixel with DTI as pixel isolation, the other with implant as pixel isolation, one without STI and one with a larger tranfer gate. The degradation of dark current is the same for all the versions.

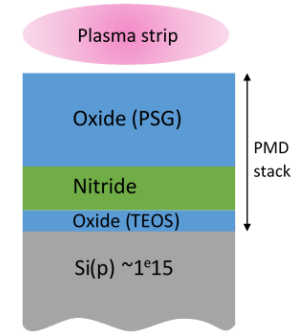

Figure 5 Studied dielectric stack: Oxide-Nitride-Oxide of Pre-Metal Dielectric layers.

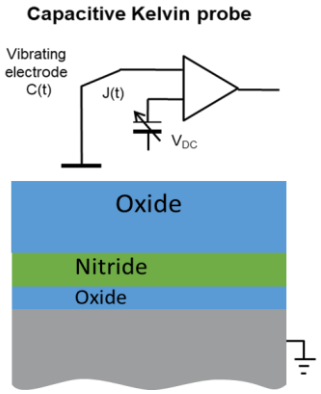

Figure 6 Kelvin probe measurement setup.

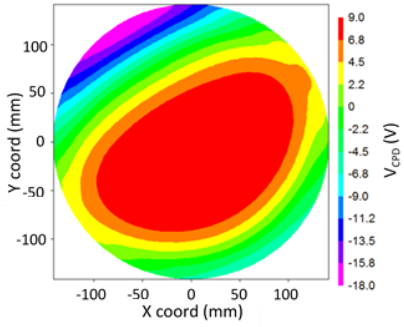

Figure 8 Mapping of V_{CPD} value for sample 4 with oxide and nitride layer.

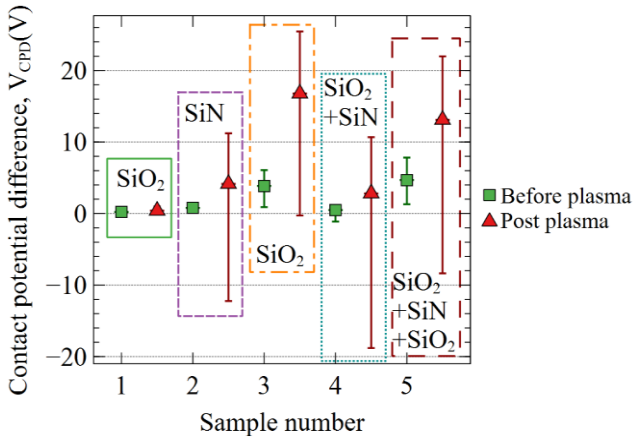

Figure 7 Surface potential (V_{CPD}) of the dielectric stacks as deposited and after plasma exposure.

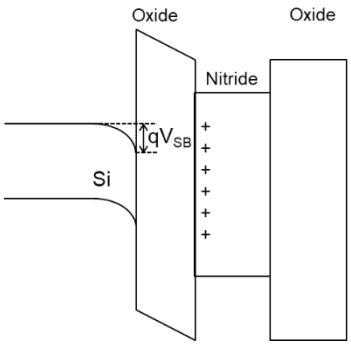

Figure 9 Band diagramm of the oxide + nitride + oxide stack. Illustrated with positive charges in the nitride layer.

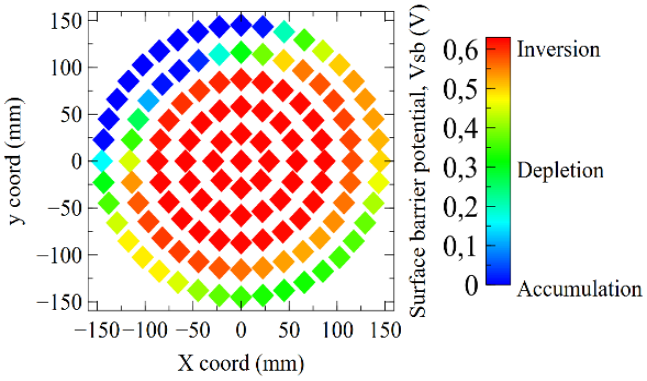

Figure 11 Mapping of the surface barrier potential, Vsb, measured on sample 4 with oxide+nitride layers.

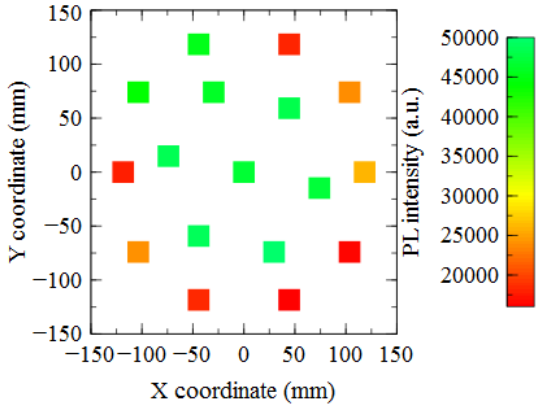

Figure 13 Mapping of the photoluminescence intensity measured on sample 4.

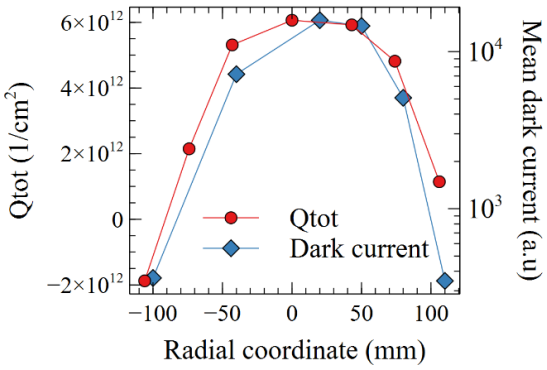

Figure 15 Total charge and mean dark current as a function of the radial coordinate (0=center of the wafer).

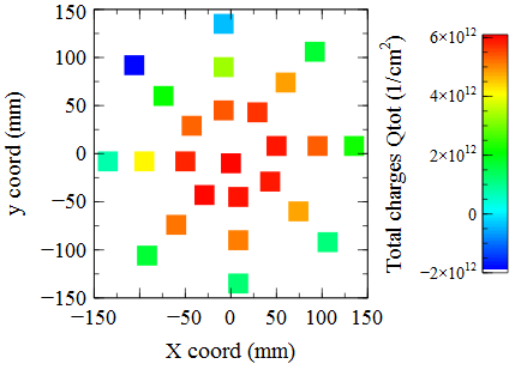

Figure 10 Mapping of the total charges measured on sample 4 with oxide+nitride layers. Charges are positive in the center of the wafer and negative at the edge.

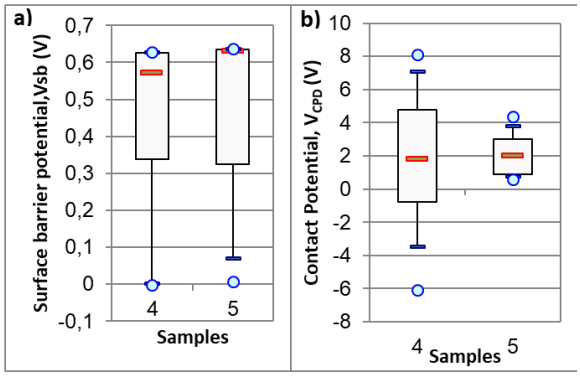

Figure 12 a) Surface barrier potential (Vsb) obtained for samples 4 and 5. Measurement done 48 days after plasma exposure. b) Contact potential difference measured in the same time that Vsb.

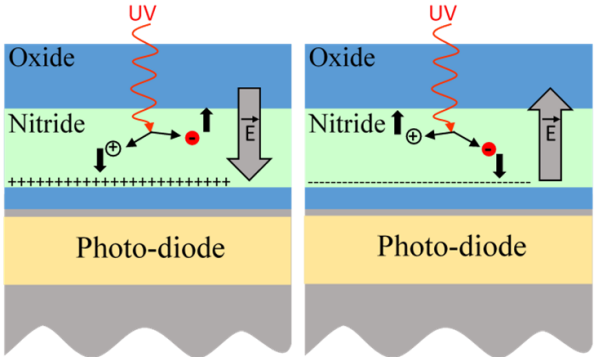

Figure 14 Schematic representation of positive and negative charges creation in the nitride layer of the pixel under plasma exposure.

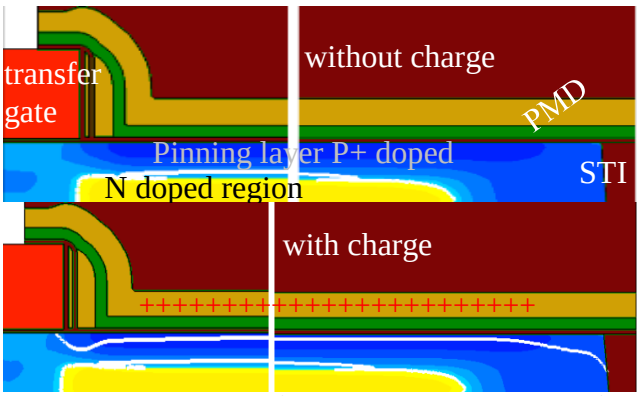

Figure 16 TCAD simulation of the photodiode with and without fixed positive charge in the nitride. The white line shows the depletion region. Transfer gate side and STI side are shown.