Random Telegraph Noise Caused by MOSFET Channel Traps and Variable Gate Induced Leakage with Multiple Sampling Readout

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***Abstract*—A study of the effect of correlated double sampling (CDS) and multiple sampling (MS) readout for random telegraph noise (RTN) is presented in this work. A 3-transistor, 1300 x 800 test cell array fabricated in 40 nm low power technology is developed to investigate MOSFET channel RTN and the RTN due to variable gate induced leakage (or GIDL RTN). All transistors in the test cell array are standard I/O devices. In CDS operation, GIDL-RTN near the reset gate-edge is primarily responsible for most of the DUTs in the RTN long tail of inverse cumulative distribution function (ICDF) distribution. The GIDL-RTN can be improved by increasing RSTL voltage. When RSTL is increased to 1.2 V, the main RTN source becomes the source-follower (SF) channel RTN. In MS operation, we found that MS readout has no effect on GIDL-RTN. In MS operation, the RTN amplitude ratio between main and side peaks is about half, compared to that of the CDS operation. A simple circuit model is used to explain this result. The SF–channel RTN can be reduced by MS operation.**

Keywords—Random telegraph noise (RTN), correlated double sampling (CDS), multiple sampling (MS), Gate induced drain leakage (GIDL)

I. INTRODUCTION

Random noise (RN) is a key performance parameter in CIS. To reduce the RN, a circuit design technique using multiple sampling (MS) is reported [6]. However, random telegraph noise (RTN) in CIS, which is caused by traps in different locations of pixel devices such as source follower (SF) [1,2], reset gate [3] and transfer gate [5,6,8], has various kinds of behaviors and may or may not be reduced by MS. The first RTN type is due to the trapping and de-trapping of channel carriers by oxide traps in pixel SF, which affects channel conductance [1,2]. The second could be due to trap-assisted tunneling (TAT) mechanism, which happens in the lightly doped drain (LDD) region of reset gate and generates discrete values of leakage current at floating diffusion (FD) [3]. The RTN in gate-induced drain leakage (GIDL) in DRAM devices could be of the similar mechanism [4]. The third type could be due to the meta-stable oxide interface SHR generation center located in the transfer gate depletion region and causes discrete values of leakage current at the FD [8].

In this work, a 3-transistors (3T) test cell array and readout circuits are developed to investigate MOSFET channel RTN and reset transistor gate-induced drain leakage RTN in 40 nm low-power process. The effects of MS for these two RTN sources are studied as well.

II. TEST CHIP STRUCTURE

Fig.1 shows the test chip schematic diagram. All the transistors in the test cell array are standard I/O device. Fig. 2 shows the timing diagram. The designed column circuit can support two modes: CDS and MS operations. In CDS operation, sense node potential (V_{SN}) is sampled twice by SHR (= SHR_d) and SHS (= SHS_d), similar to conventional CDS operation in CIS. In MS operation, V_{SN} is sampled four times by SHR, SHR_d, SHS and SHS_d. T_d is the time delay between the falling edge of SHR (SHS) and SHR_d (SHS_d). Because the outputs of two PMOS SFs in one buffer are tied together and share same current source (IB), both the V_{R1} and V_{R2} (V_{S1} and V_{S2}) will affect the buffer output, as expressed in (1).

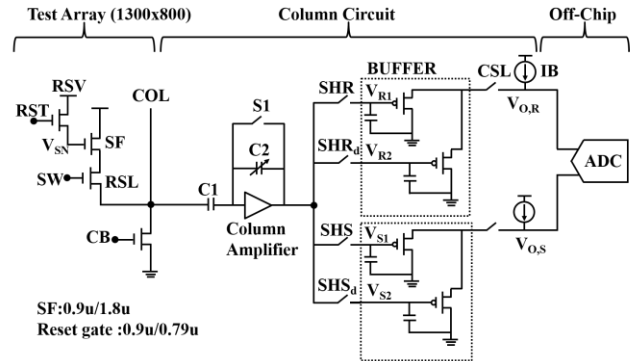

Fig.1 Test chip schematic diagram.

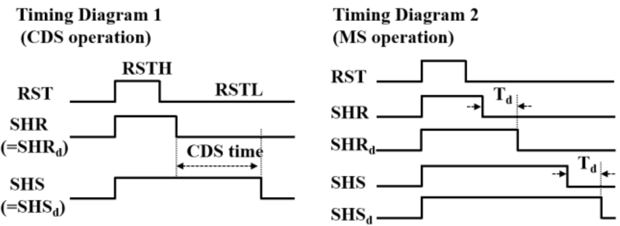

Fig.2 Timing diagram.

$$V_{O,R} = \frac{V_{R1}+V_{R2}}{2} + V_{tp} + \frac{1}{2}\sqrt{-(V_{R1}-V_{R2})^2 + \frac{4\times IB}{\mu_p C_{ox}(W/L)}} \quad (1)$$

$$V_{O,S} = \frac{V_{S1}+V_{S2}}{2} + V_{tp} + \frac{1}{2}\sqrt{-(V_{R1}-V_{R2})^2 + \frac{4\times IB}{\mu_p C_{ox}(W/L)}}$$

where μ_p is charge mobility of PMOS SF, C_{ox} is the oxide capacitance and (W/L) is PMOS SF size. From the result, $V_{O,R}$ ($V_{O,S}$) is the average of V_{R1} and V_{R2} (V_{S1} and V_{S2}) approximately. Finally the differential output ($V_{O,R}$-$V_{O,S}$) is read by off chip ADCs.

III. RESULTS AND DISCUSSION

A. Measurement results with CDS operation

Fig. 3 depicts the inverse cumulative distribution function (ICDF) of the RN under CDS time = 25us, RSV = 2.8V, RSTH = 3.8V and several RSTL biases with CDS operation. Fig. 4

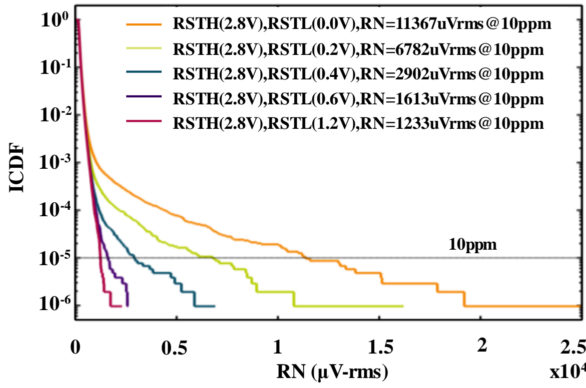

Fig. 3 The ICDF of the RN under CDS time = 25us, RSV = 2.8V, RSTH = 3.8V and several RSTL biases with CDS operation (timing diagram 1 in Fig. 2).

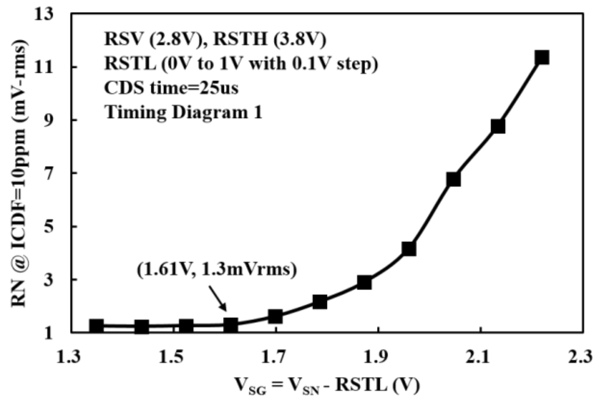

Fig. 4 The RN (at ICDF = 10ppm in Fig. 2) versus V_{SG} (= V_{SN} – RSTL). RSTL sweeps from 0V to 1V with step = 0.1V (in 0.1V steps).

shows the RN at ICDF = 10ppm in Fig.3 versus V_{SG} (= V_{SN} – RSTL). The RN decreases while V_{SG} decreases, and becomes saturated when $V_{SG} \leq 1.61$V. This implies that the RN long tail is mostly contributed by GIDL RTN of the reset gate because it is mainly affected by reset transistor source to gate voltage difference (V_{SG}). The mechanism of GIDL RTN could be trap-assisted tunneling (TAT) [3] or meta-stable energy level of traps [4].

Fig. 5 shows the correlation between the RN at RSTL = 0V and the RN at RSTL = 1.2V with a RN range of 0 ~ 2000uV-rms. The RN long tail is strongly affected by RSTL voltage because it is dominated by GIDL RTN at reset gate edge [3]. For the SF channel RTN, it is not affected by RSTL voltage.

Fig. 6 shows the 5000-frames noise waveform of 3 selected DUTs under CDS time = 10us, 20us and 25us, respectively. DUT A shows clear two discrete levels, and DUT B shows clear multi-discrete levels. DUT C shows a main peak with two symmetric side peaks which are caused by SF channel RTN [2]. The amplitude between main and side peaks of SF channel RTN is not affected by CDS time [7]. For DUT A and B, capture and emission time constants seem to be much longer than the time constant of DUT C.

Fig. 7 shows the amplitude of two discrete levels of DUT A with CDS time = 10us, 20us and 25us, respectively. The values of two discrete levels have a linear dependence on CDS time.

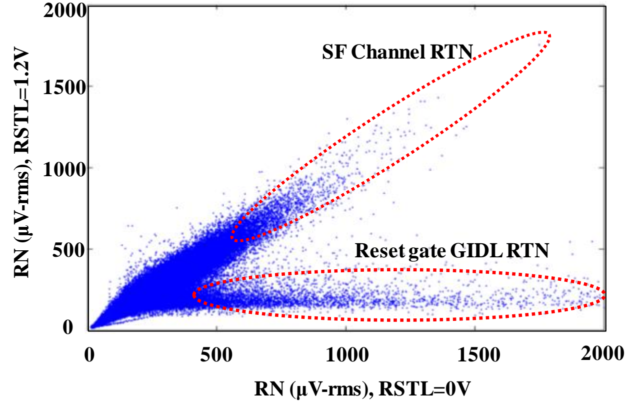

Fig. 5 The correlation between the RN at RSTL = 0V and the RN at RSTL = 1.2V with a RN range of 0~2000uV-rms.

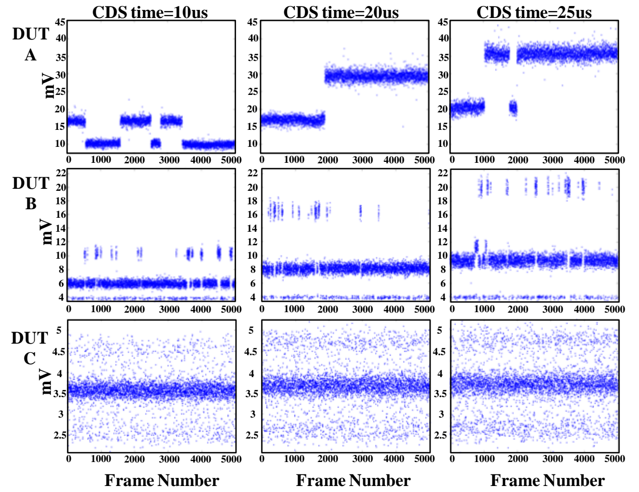

Fig. 6 The 5,000-frame noise waveforms (captured at 1fps) of 3 selected DUTs under RSV = 2.8V, RSTH = 3.8V, RSTL = 0V and CDS time = 10us, 20us and 25us, respectively.

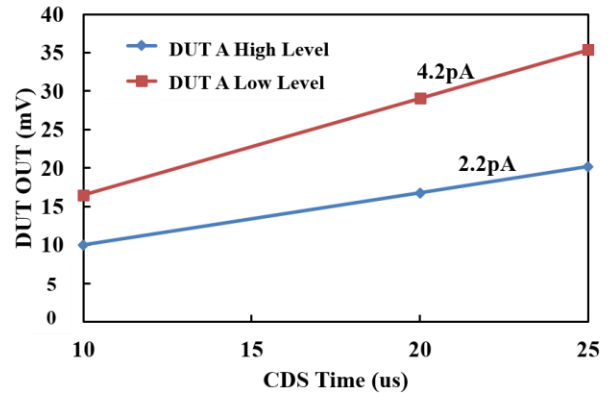

Fig. 7 The amplitude of the two discrete levels of DUT A in Fig.6 versus CDS time = 10us, 20us and 25us, respectively.

The leakage current of the low- and high-level are 2.2pA and 4.2pA, respectively. The estimated sense node capacitance (C_{SN}) is around 3.3fF. For DUT A and B, the discrete voltage levels are caused by variable reset gate induced sense node leakage [8].

Fig. 8 shows a comparison of the noise compositions of the noisiest 1,000 DUTs between two conditions. One is under GIDL-enhanced voltages (RSTH, RSTL) = (3.8V, 0V), and the

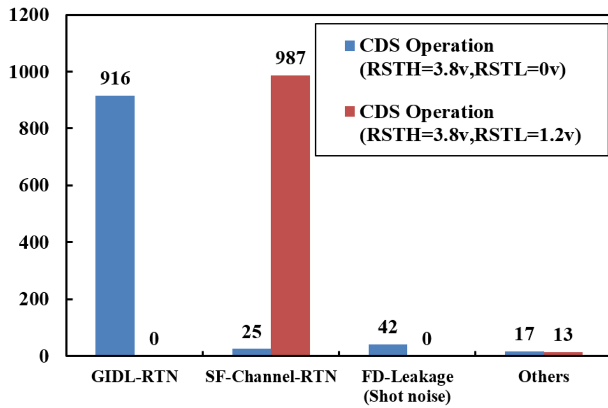

Fig. 8 Comparison of the noise compositions of the noisiest 1,000 DUTs. One condition is under GIDL-enhanced voltages (RSTH, RSTL) = (3.8V, 0V), and the other is under GIDL-reduced voltages (RSTH, RSTL) = (3.8V, 1.2V). Both uses CDS operation (timing diagram 1 in Fig. 2).

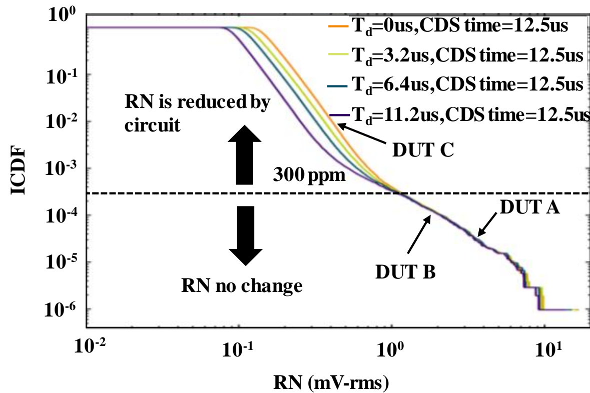

Fig. 9 The ICDF of the RN under CDS time = 12.5us, RSV = 2.8V, RSTH = 3.8V and RSTL = 0V with MS operation (timing diagram 2 in Fig. 2).

other is under GIDL-reduced voltages (RSTH, RSTL) = (3.8V, 1.2V). Both use CDS operation. In GIDL-enhanced condition, GIDL-RTN is the major noise source from top 1,000 noisiest DUTs. In contrast, in GIDL-reduced condition, SF-channel RTN becomes the major noise source for top 1,000 noisiest DUTs.

B. Measuement results with MS opeartion

Fig. 9 illustrates the ICDF of the RN with MS operation. The shape of the RN long tail (below 300ppm) in ICDF almost remains the same as T_d changes. Only the low noise portion (above 300ppm) of the ICDF shifted towards lower values as T_d is increased. Because RN long tail is mainly dominated by GIDL RTN at reset gate edge, this implies that MS has no effect on GIDL RTN, and could only reduce thermal noise and channel RTN of the SF.

Fig. 10 illustrates the 5,000-frame noise waveforms of 3 selected DUTs. The RN location of these 3 DUTs are shown in the Fig. 9 as well. DUT A and B are GIDL RTN cases, and DUT C is MOSFET channel RTN case. For DUT A and B, each discrete level keeps its original value, and time domain waveforms are similar as T_d changes from 0us to 11.2us. This can explain why the shape of RN long tail is the same as T_d changes. From the result, the MS operation has no effect on

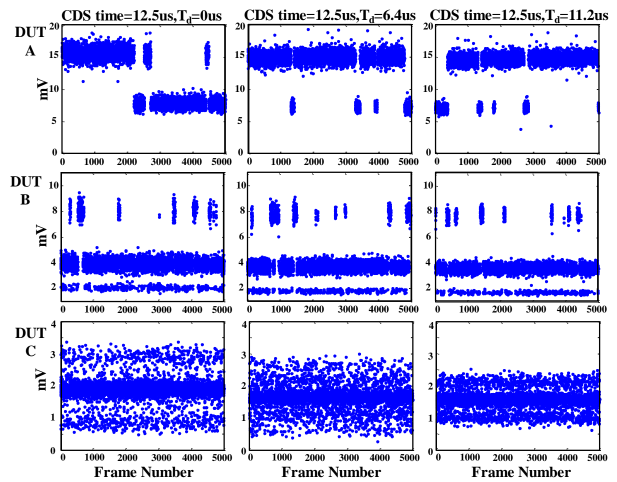

Fig. 10 The 5,000-frame noise waveforms (captured at 1fps) of 3 selected DUTs under CDS time = 12.5us and T_d = 0us, 6.2s and 11.2us, respectively.

GIDL RTN. This phenomenon can be explained in next two paragraphs. For DUT C, the RTN amplitude between main peak and symmetric side peak becomes smaller gradually as T_d increases. We will discuss it later.

Fig. 11(a) shows GIDL RTN (two leakage states in this example) with MS operation. Here we assume that there is only one trap near the reset gate edge. Charge trapping or de-trapping in the trap will affect GIDL behavior and induce two-level leakage currents. The capture and emission time constants are assumed to be longer than readout time. For T_d = 0us case, the sampled sense node voltage (V_{SN}) is determined by the falling edge of SHR and SHS, and the ΔV_{SN} represents leakage voltage during CDS time. Since leakage current has two discrete states in this example, the ΔV_{SN} will have two states. The mechanism can explain the measurement result in Fig.6 DUT A case. For the case of a single trap with multiple energy states or multi-traps at reset gate edge, multiple discrete levels should be obtained.

For $T_d \neq$ 0us case, the sampled V_{SN} is determined by the falling edges of SHR, SHR_d, SHS and SHS_d. V_{SN1} corresponds to the average voltage of the sampled V_{SN} determined by SHR and SHR_d. V_{SN2} corresponds to the average voltage of the sampled V_{SN} determined by SHS and SHS_d. Because sense node leakage voltage has a linear dependence on time, the leakage voltage (ΔV_{SN}) with different T_d settings in the same leakage state should have the same result. This explains that each discrete level of DUT A and B in Fig. 10 remains unchanged as T_d changes from 0us to 11.2us. Due to the characteristic, MS operation has no effect on GIDL RTN.

Fig. 11(b) shows the measured median RN with MS operation for the 1300x800 test cell array. The median RN is mainly dominated by thermal and flicker noise of the source follower in the array, and it can be reduced by the MS operation, as reported in the literature [9].

In order to explain the behavior of SF-channel RTN with MS operation, a simple model is proposed in Fig. 12. The circuit output histogram and the probability of each state with CDS and MS operations are illustrated. In the simple model, capture and emission time constants are assumed much shorter

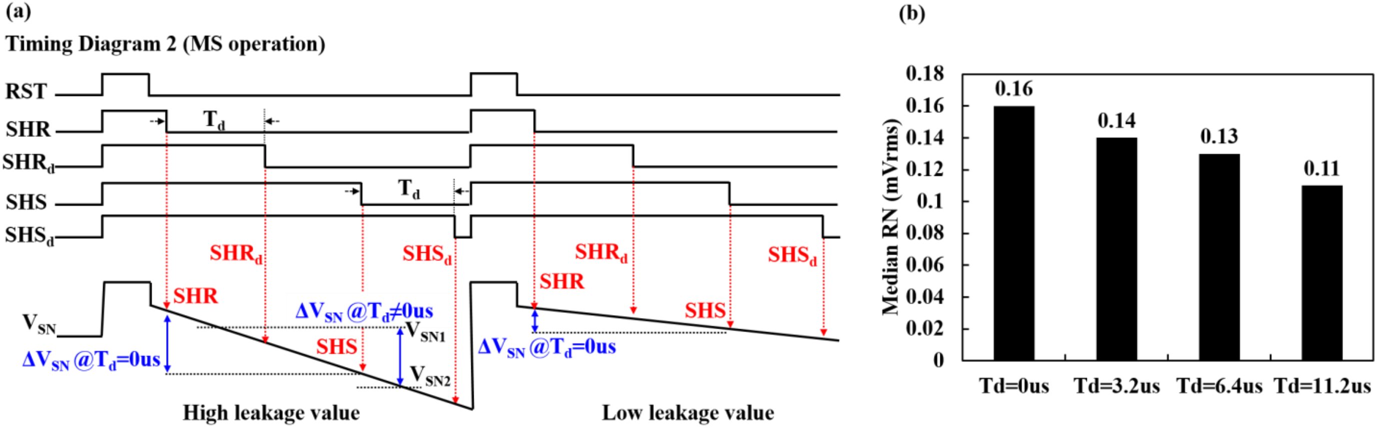

Fig. 11 (a) The GIDL-RTN (two leakage states in this example) with MS operation in timing diagram 2 in Fig. 2. The values of ΔV_{SN} in the same leakage state with different T_d show the same result. (b) The measured median RN under CDS time = 12.5us, RSV = 2.8V, RSTH = 3.8V and RSTL = 0V with MS operation (timing diagram 2 in Fig. 2).

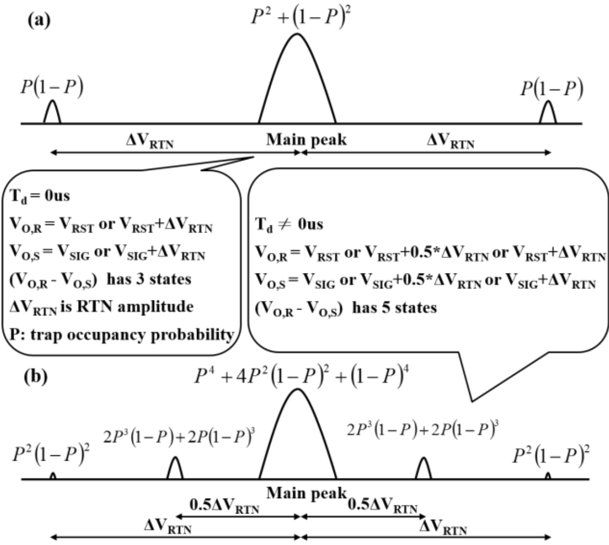

Fig. 12 Ideal circuit output histogram and the probability of each state with timing diagram 2 in Fig. 2; (a) T_d = 0us, (b) $T_d \neq$ 0us. (RTN capture and emission time constants are assumed to be much smaller than T_d).

than the CDS time and T_d value. In the case of T_d = 0us, sensor output with three states has been reported [2]. In the case of $T_d \neq$ 0us, because both the circuit output terminals ($V_{O,R}$ and $V_{O,S}$) can have three discrete states, the final signal swing ($V_{O,R}$-$V_{O,S}$) can have five discrete states. The RTN amplitude (ΔV_{RTN}) between the main peak and the major side peak becomes half roughly, compared to the case of T_d = 0us. This matches the measurement results shown in Fig. 10 DUT C case. However, the second side peak cannot be observed in measurement. This could be due to the limited circuit bandwidth [7].

IV. Conclusions

In this work, a 3T test cell array (1300x800) and a readout circuit are developed to investigate SF-channel RTN and reset transistor GIDL RTN in 40 nm low-power technology. The designed readout circuits can support both CDS and MS operations. Under the default bias with timing diagram 1, we found that GIDL RTN is much worse than SF-channel RTN, and most of DUTs in RN long tail of ICDF plot are GIDL-RTN case. Reset gate GIDL-RTN can be improved dramatically by decreasing source to gate voltage of the reset transistor.

From the results with MS operation, we found that MS has no effect on GIDL RTN because leakage voltage (ΔV_{SN}) at sense node has a linear dependence on time. On the other hand, for the SF-channel RTN, the RTN amplitude between the main peak and the major side peak becomes half due to MS operation. From the measurement result, the SF-channel RTN can be reduced by MS operation.

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