

Back Side Illuminated, Fully Depleted, Pinned Trench Photo MOS for Imaging Applications

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Abstract - This paper describes a new BSI image sensor pixel using an advanced Photo-MOS structure designed with capacitive deep trench pixel-to-pixel isolation. This Photo-MOS technology is a smart alternative to the conventional implanted pinned photodiode and providing an image quality gain. Indeed the photo-gate device fabrication takes benefit from the full-depth front process MOS trench etched through a fully optimized silicon epitaxial layer and dedicated to photon absorption, signal charges collection and storage zone avoiding any implanted doping species. On top of the photo Gate device, a planar read-out transistors and a vertical transfer gate is proposed.

I. INTRODUCTION

In this work, a new deep vertical fully depleted pinned Photo Gate device instead of fully depleted pinned photodiode for active pixel image sensor application is presented. Introduced for CCD application [1] and nowadays largely used in CMOS image sensor [2], conventional Back Side Illuminated (BSI) pinned photodiode process is limited by ion high-energy process capabilities and suffers from crystal damage and metal contamination that come along with desired implanted species [3],[4],[5].

The main advantage of the proposed vertical Photo-Gate device using epitaxial silicon as active layer lies in the realization without any implantation and collateral damaging. This architecture takes benefit from Capacitive Deep Trench Isolation (CDTI), formerly introduced for dark current reduction [6] and more recently for fully depleted memories for global shutter application [7],[8]. The proposed Photo MOS works in the charge domain taking advantages from vertical MOS capacitance to manage electrostatic potential to store positive charges (h^+) in fully depleted silicon

epitaxial layer. High full well, high Quantum Efficiency (QE) and low dark current with no lag has been demonstrated on tested devices. This architecture is compatible with Correlated Double Sampling (CDS) readout mode and likely could, for some applications, challenge the well-established fully depleted photodiode.

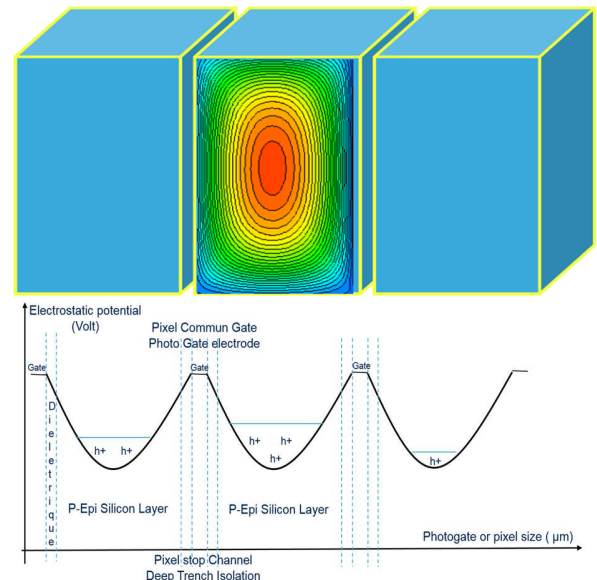


Fig.1. Device schematic and electrostatic potential diagram of the proposed architecture

II. VERTICAL PINNED PHOTO GATE

Figure 1 shows the vertical photogate principle where the epitaxial silicon starting material is fully enclosed by trench Si-Poly gate MOS. The photogate electrode, laterally positioned and shared by two pixels, works as pixel-to-pixel isolation to overcome the electrical and optical crosstalk and is, as well, used for electrostatic potential control. The gate electrode voltage is advantageously set to force the Si-SiO₂ interface in inversion mode for interface dark current cancellation [6], [9] at a specific standby voltage required by the pinning principle.

To complete the pixel, front side vertical Shallow Trench Transfer Gate and Planar Read Out transistor are implemented on top of the Photo MOS device. The N well region, provided by the transistor realization, works as top Photogate pinning layer supplying pinning voltage and carrier source for lateral and bottom surface inversion layer creation. On the backside and after wafer silicon thinning, the silicon surface passivation layer is deposited. This passivation stack is optimized for backside interface dark current cancellation and pixel sensitivity maximization. Figure 2 shows the SEM cross section of the 2 μ m pixel pitch prototype fabricated.

III. PIXEL WORKING PRINCIPLE AND OPERATING CONDITIONS

The P type choice for the starting material implies the signal charge to be holes carriers and pixel readout transistor will be PMOS device. Conventional 2T5 pixel schematic is proposed with operating power supply [0V; 3V3] range. The electrostatic bucket potential shape is determined by silicon net doping concentration. For this reason the P epitaxial layer doping has to be carefully considered to obtain the proper electrostatic fully depletion voltage targeting high charge

storage capability without any lag due to incomplete transfer.

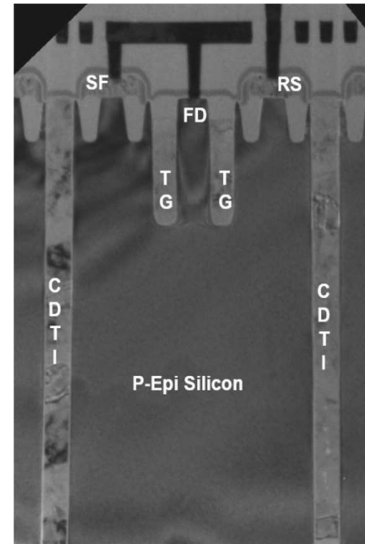


Fig. 2. Pixel SEM cross-section including deep trench (CDTI), Transfer Gate (TG) trench and planar MOS read transistor

The pixel electrostatic 2D simulated potential when the Transfer Gate is turn Off and On is respectively shown in figure 3.

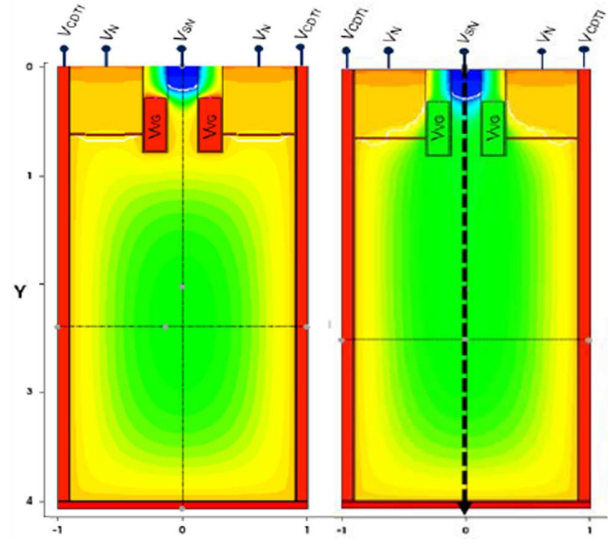


Fig.3. Electrostatic potential diagram, TG Off (left), TG On (right)

As shown in figure 4, when the transfer gate is turned On the electrostatic barrier is

removed and charge are transferred from in depth charge collection zone to the P+ surface Sensing Node (SN) zone.

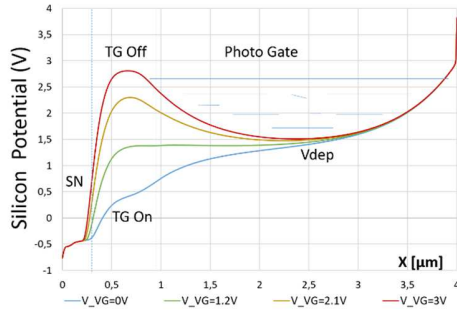


Fig.4. Electrostatic potential cutline: TG switching Off to On state

IV. RESULTS AND DISCUSSION

A summary of the 2.0 μm pitch, 2T5 rolling shutter architecture pixel array performances is presented in Table I.

TABLE I
PIXEL PERFORMANCES

Characteristics	
Pixel pitch	2.0 μm , 2T5, RS
CVF	90 $\mu\text{V}/\text{h}^+$
Saturation charge	13 000 h^+
QE @ 550 nm	80 %
PRNU	0.5 %
Dark current @60°C	5 h^+/s
Lag	no lag
Temporal noise floor	2 h^+
Dynamic range	75 dB

The active pixel readout conversion factor is $90\mu\text{V}/\text{h}^+$. As shown in figure 5, the pixel charge storage capability is totally driven by the epitaxial layer doping level and final thickness after wafer back side thinning. As

expected, the full well goes up linearly with the epitaxial layer thickness. In addition, the amount of charge goes up with the epitaxial doping level going up. Charge capability up to 13000 h^+ with no lag has been demonstrated for 1.5 Volt pinning voltage and 4.8 μm full silicon thickness.

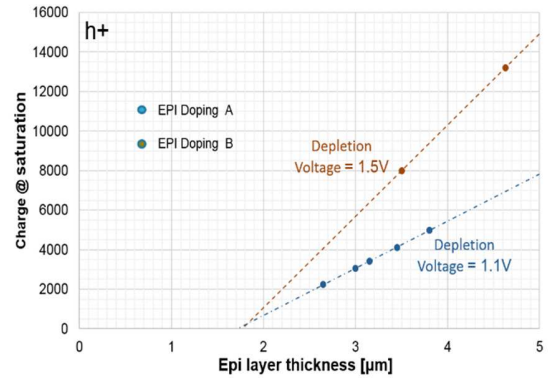


Fig. 5. Full well capability versus P-/Psub starting material

On this graph, one can observe a 1.7 μm equivalent zone without any charge storage. This zone comes from vertical TG foot print and top and bottom space charge extension (see fig3).

The Quantum Efficiency (QE), shown in figure 6, takes also advantage of the epitaxial layer thickness increase with a maximum QE of 80% at 550nm (no color filter, no micro lens).

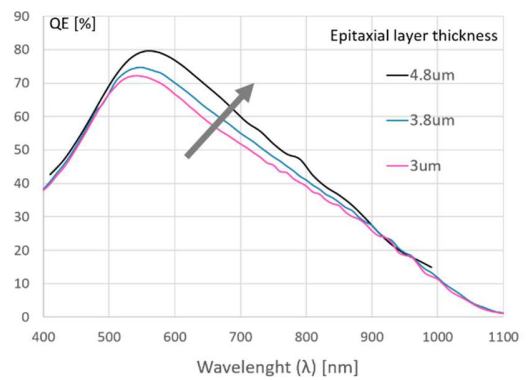


Fig. 6. Quantum Efficiency versus starting material

Dark current, monitored by pixel sidewall field effect passivation mechanism, reaches 5 h+/s with a standard deviation of 15 h+/s at 60°C (see figure 7) and is thus largely reduced compared to a BSI process, CDTI pixel isolation, planar N-type pinned diode experimental samples.

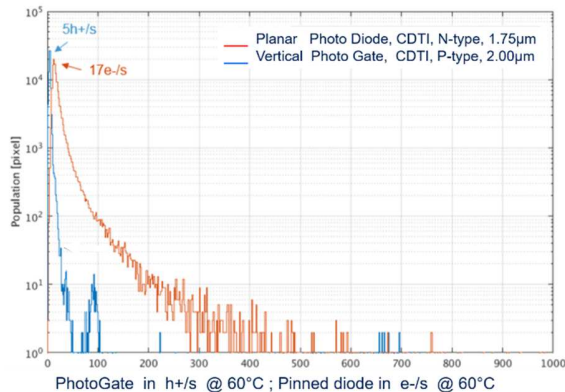


Fig. 7. Pixel dark current population @ 60°C

According to the implantation free photoactive collection and storage region, the tail of the distribution is pretty much eradicated.

Thanks to high full well capability and low noise floor figure, 75dB dynamic range has been demonstrated.

V. CONCLUSION

In this contribution, the results of a new 2T5 rolling shutter Active Pixel Sensor integrating vertical Photo MOS for imaging application are presented. The pixel works according to the fully depleted pinned MOS capacitance principle. The merge of the capacitive deep trench isolation and MOS gate electrode has been successfully introduced with process simplification. High QE, high full well, managed by the starting material, have been demonstrated and easily tuned by adjusting trench depth and epitaxial layer thickness.

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References:

- [1] N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, "No image lag photodiode structure in the interline CCD image sensor" in *Electron Devices Meeting, 1982 International*, vol. 28. IEEE, 1982, pp. 324–327
- [2] P.Lee, R.Gee, R.Guidash, T.Lee and E.Fossum, "An Active Pixel Sensor Fabricated Using CMOS/CCD Process Technology" in *Proc. IISW*, Jun. 1995
- [3] G. Fuse and M. Sugitani, "Fundamental Ion Implantation Technologies for Image Sensor Devices" *Proc Int. Image Sensors Workshop (IISW)*, pp.17-20, Snowbird, USA, June 2013.
- [4] N.Teranishi, G.Fuse and M. Sugitani "A Review of the Ion Implantation Technology for Image Sensors" in *Sensors* **2018**, 18, 2358; doi:10.3390/s18072358
- [5] J.Michelot, F.Roy, J.Prima, C.Augier, F.Barbier, S.Ricq, P.Boulenc, Z.Essa, L.Pinelli, H.Leininger, M.Gatefait and J-E.Broquin., "Back illuminated vertically pinned photodiode with in depth charge storage", in *Proc. IISW*, Jun. 2011.
- [6] N. Ahmed, F. Roy, G.-N. Lu, B. Mamdy, J.-P. Carrere, A. Tournier, N. Virollet, C. Perrot, M. Rivoire, A. Seignard, D. Pellissier-Tanon, F.Leverd, B.Orlando, "Mos capacitor deep trench isolation for cmos image sensors," in *Electron Devices Meeting (IEDM), 2014 IEEE International*. IEEE, 2014.
- [7] A. Tournier, F. Roy, Y. Cazaux, F. Lalanne, P. Malinge, M. McDonald, G. Monnot, N. Roux, "A HDR 98dB 3.2µm Charge Domain Global Shutter CMOS Image Sensor" in *Electron Devices Meeting (IEDM), 2018 IEEE International*. IEEE, 2018.
- [8] F.Roy, Y.Cazaux P.Waltz, P.Malinge, N.Billon Pierron, "Low Noise Global Shutter Image Sensor Working in the Charge Domain", in *IEEE Trans Letters*, 2019.
- [9] J. Janesick, "Multi-pinned phase charge-coupled device" in *NASA Tech Brief*, August 1990, vol. 14, no. 8, p. 22.