Electrical characterization of the backside interface on BSI global shutter pixels with Tungsten-shield test structures on CDTI process.

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***Abstract*-A new methodology is presented using well known electrical characterization techniques on dedicated single devices in order to investigate backside interface contribution to the measured pixel dark current in BSI CMOS image sensors technologies. Density of interface states and charges within the oxide extractions are achieved. The results show that in our case, the density of state is not directly the source of dark current excursions. The quality of the passivation of the backside interface appears to be the root cause. Thanks to the presented new test structures, it has been demonstrated that backside interface contribution to dark current can be investigated separately from other contributions.**

I.INTRODUCTION

Backside illuminated (BSI) technologies have evolved to incorporate new backside interface passivation techniques (i.e. high-K negatively charged dielectric stack to easily accumulate holes and therefore passivate the interface [1]) and tungsten (W) layer for shielding requirement of BSI Global Shutter pixels. Interface states and/or the quality of the passivation can be key for dark current. Therefore it is crucial to develop this interface characterization. Figure 1 shows the median distributions of dark current (Idark) measured on a pixel array at wafer level for three wafers processed with a BSI CDTI technology, the dielectric stack being a Ta2O5/Al2O3 with process condition variants. Atypical behaviors can be seen on wafers 2 and 3. For both wafers, there is a higher and non-uniform dark current. In the following work, the different measurements have been performed on the same dies as for the Idark measurement (Figure 2). To study the potential correlation between Idark, density of interface states (Dit) and quality of passivation (negative charges within the oxide Neff), two test structures have been developed in a BSI global shutter pixel technology (with CDTI [2]) using the W-shield as a gate: a backside MOS capacitor (Figure 3) ($L = 500\ \mu m, W = 31.6\ \mu m$) and a backside W-shield gate pseudo-MOS transistor (Figure 4) ($L = 10\ \mu m, W = 27\ \mu m$). In the last structure, CDTI are biased in a way that there is always an inversion layer at their interface in order to connect surface source and drain to the bottom interface of interest (channel of the W-shield gate transistor). Figure 5 shows the conventional operation of the transistor test structure. In the next sections, first Dit is investigated with a tentative correlation with Idark. Then the passivation quality is studied. Finally, a charging phenomenon present on both structures is presented.

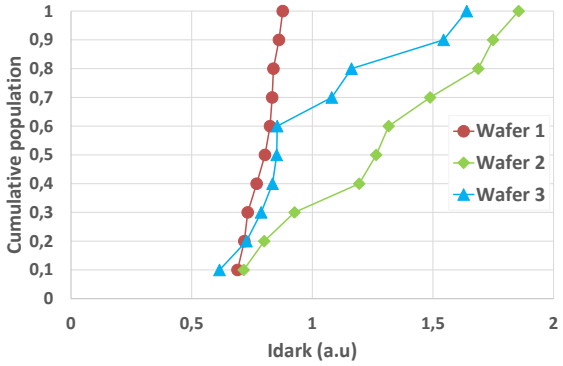

Figure 1 : Cumulative population of the pixel dark current measured on testchips on several dies of 3 wafers showing distinct behaviors depending on the wafer.

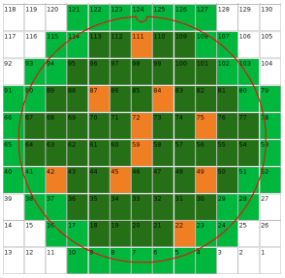

Figure 2 : Sampling map of the measured dies (in orange) for all the measurements.

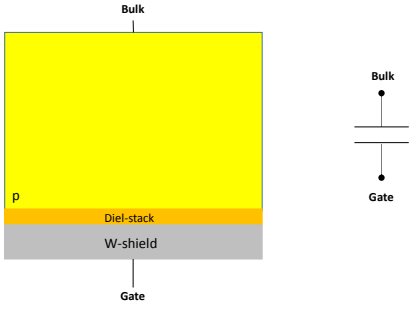

Figure 3 : Illustration of the capacitive test structure used to extract N_{eff}.

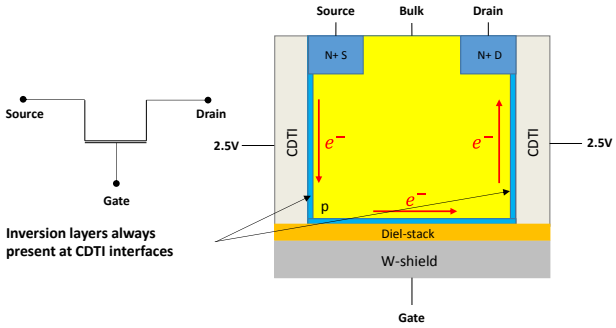

Figure 4: Illustration of the transistor test structure used to extract D_{it} (an isolation is present between the source and drain to prevent punchthrough).

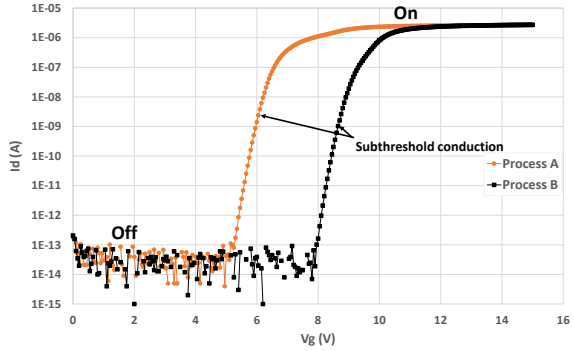

Figure 5 : Id(Vg) curves showing the conventional operation of the atypical transistor with clear ON/OFF behaviors.

II. INTERFACE STATES CHARACTERIZATION

The dark current generated by an interface may be dominated by interface states if their density is high. In order to extract the interface states density (Dit) for each die, the charge pumping method [3] [4] [5] is applied on the W-shield transistor test structure (Figure 4). The method is illustrated by Figure 6. The CDTI are biased at 2.5V in order to have an inversion layer at their interface. The drain and the source are grounded. A square pulse with the following characteristics is applied to the W-shield gate: $V_{gpulsebase}$ is swept from 2V to 12V, $\Delta V_{gpulse} = 6$V, minimum frequency of the signal $f = 50$ kHz and rise and fall time $T_{r,f} = 1$µs. The pumped current is measured through the bulk contact. The choice of the minimum frequency was made in order to avoid the measurement of traps in the High-K dielectric volume [6]. Using the method described in [7], no geometric effect was detected in the measurements. The maximum measured pumped current is proportional to the mean Dit (cm^{-2}):

$$I_{pump_{max}} = D_{it} q S f \qquad (1)$$

Here, $I_{pump_{max}}$ represents the maximum pumped current, q is the elementary charge, S the gate area. Figure 7 shows the maximum pumped current as a function of the

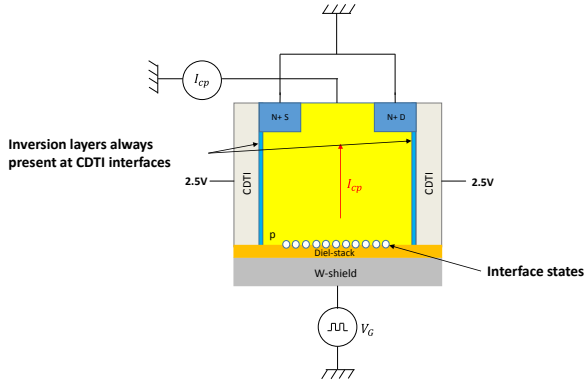

Figure 6: Charge pumping method applied to W-shield transistor test structure.

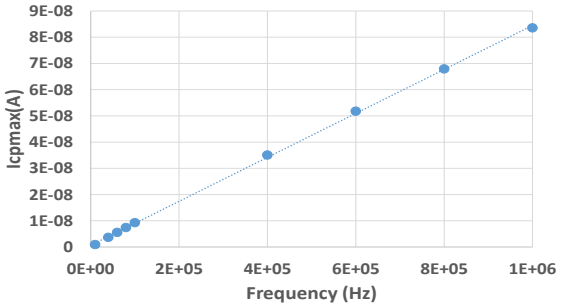

Figure 7: Icpmax(f) curves with the transistor test structure.

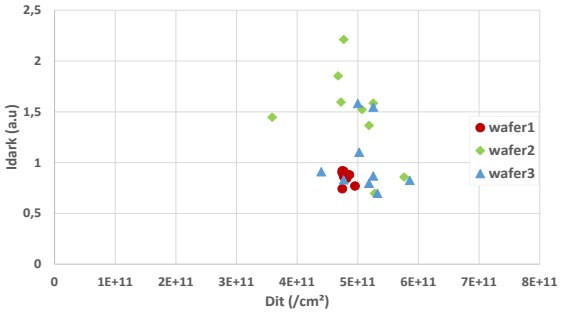

Figure 8 : Idark(Dit) scatter plot. All the wafers show a same level of Dit.

frequency. It can be seen that the maximum measured pumped current is linear with f which is in agreement with equation (1). The slope extraction gives Dit. Measurements are performed on the 3 wafers using the sampling map of Figure 2. Figure 8 presents the Idark vs Dit scatter plot. It does not show any clear tendency. Dit looks not to be correlated to Idark in this case. So the measured dark current differences between the 3 wafers do not seem to be explained by a difference of Dit, it can be seen that all the wafers have an equivalent level of interface states ($\sim 5 \times 10^{11}/cm^2$).

III. QUALITY OF THE PASSIVATION CHARACTERIZATION

As interface states do not seem to be the response for Idark excursions, the quality of the passivation

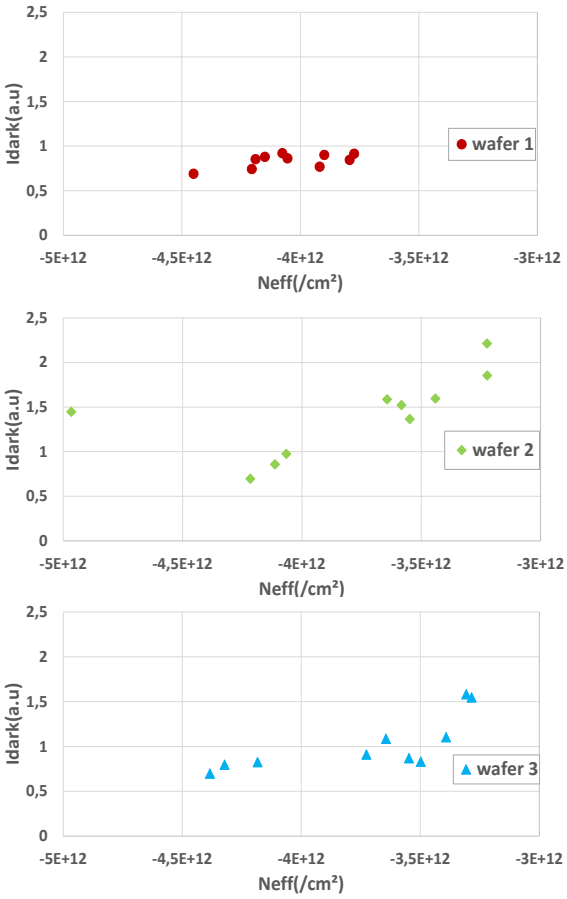

Figure 9 : Idark(Neff) scatter plot for the 3 wafers.

might be another root cause of the Idark response seen in Figure 1. Indeed, with very similar Dit on the measured wafers, the field effect passivation, that is, having an electric field at the interface to accumulate charges in order to passivate the interface, can have a key contribution. The electric field is induced by negative charges within the oxide (Neff). On the following analysis the Maserjian's function is used on C-V measurements to estimate the effective charge density within the oxide on the capacitive structure (Figure 3) [8] [9]:

$$Y(V_g) = \left(\frac{1}{C}\right)^3 \frac{dC}{dV_g} \qquad (2)$$

Thanks to this function, the substrate doping concentration (N_a) and the flat band voltage (V_{FB}) can be extracted:

$$Y_{min} = -\frac{1}{q\varepsilon_{Si}N_a} \qquad (3)$$

$$Y(V_{FB}) = -\frac{Y_{min}}{3} \qquad (4)$$

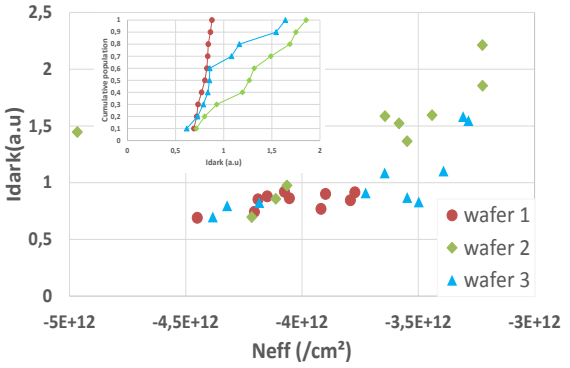

Figure 10 : Idark(Neff) scatter plots for wafers 1, 2 and 3. Contrary to the Dit study, a correlation is visible between Neff and the measured dark current.

Where Y_{min} is the minimum reached by the Maserjian's function and ε_{Si} the silicon permittivity. Then it is possible to calculate Neff:

$$N_{EFF} = \frac{-(V_{FB}-W_{MS})C_{ox}}{q} \qquad (5)$$

Where N_{EFF} is the effective number of charges within the oxide, W_{MS} the metal semiconductor work function and C_{ox} the oxide capacitance. For the measurements, the following characteristics are applied: V_g is swept from 2V to 12V, the signal frequency applied is $f = 50$ kHz, and the modulation of the signal is 0.02V. Figure 9 presents the scatter plots of Idark vs extracted Neff for the 3 wafers. On wafer 1, it is hard to extract an eventual correlation probably because the Idark distribution is very narrow (Figure 1). However, on wafers 2 and 3, a clear correlation can be identified between Neff and Idark. In order to observe if there is a more general tendency, a global scatter plot with the 3 wafers together is shown in Figure 10. On this figure, two parts of the scatter plot can be distinguished: a first one where the dark current increase according to Neff is weak (almost a plateau) and a second one where the dark current increase according to the Neff decrease (in absolute value) is clearly visible. According to [1], the plateau is explained by the fact that when a certain number of charges within the oxide is reached, the interface is fully passivated and the Idark from the backside interface becomes negligible and the measured dark current comes from another part of the pixel (DTI, frontside interface, silicon volume etc.). On the contrary, when Neff decrease (in absolute value) as on some wafer 2 and 3 dies, the passivation is not efficient enough and a significant Idark appears coming from the BS interface.

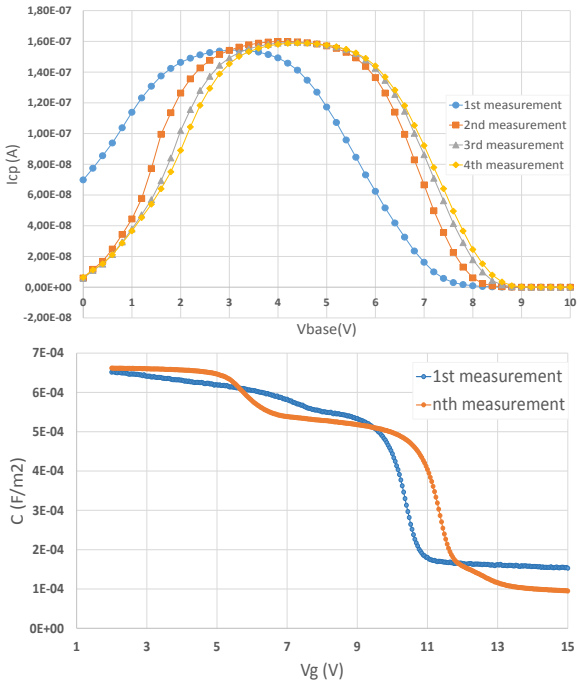

Figure 11 : Charging effect measured on both MOS and W-shield transistor structures.

IV. CHARGING EFFECT ON BOTH STRUCTURE

After a first measurement up to relatively high voltage on both structure, a charging effect occurs when the structures are measured a second time and again. This effect can be seen on Figure 11. In both cases, the curve shift seems to be related to a V_{FB}/V_t shift. In the case of the charge pumping, between the first measurement and the other ones, the maximum pumped current slightly increases which is the result of an increase of Dit according to equation (1). In the case of the C-V measurement, it can be seen that a more pronounced bump is present after a certain number of measurements. A bump in C-V measurements can be the result of Dit centered within the gap [10]. Concerning the curves shift, one possible explanation is that during the measurements V_g reaches high voltage (here 12V) that can induce a negative charge injection which results in higher V_{FB}/V_t voltage. A hysteresis effect may be seen (and may be correlated with the charging effect) on both structures (Figure 12). In this case, V_g is swept from 0V to 12V and then from 12V to 0V and finally from 0V to 12V again. An effect of charging/discharging can be seen. To be more precise, more investigations would be needed and at least cautions have to be taken. The different extractions presented earlier in this paper were made during the first measurement when structures are not already stressed. After waiting a certain time, the structures come back at their initial state. It should

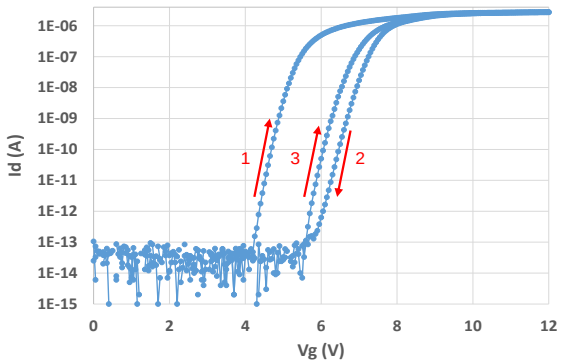

Figure 12: Hysteresis effect on the transistor structure, the same effect can be seen on the capacitance structure.

be noted that for the product utilization, such conditions are not applied and such effect should not happened.

V. CONCLUSION

With these structures, it is possible to electrically characterize the backside interface of a BSI technology using tungsten shield. By means of two known characterization methods, it is possible to extract Dit and Neff (which are the two important parameters for dark current). So it is possible to determine if the dark current mainly comes from the backside interface, and to discriminate the origin of the BS dark current. A drawback of this method is the presence of a charging effect which have to be studied more precisely. In addition to these Idark contribution studies, these dedicated devices with associated characterizations can be helpful for process monitoring, TCAD calibration and reliability works.

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