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Crystalline Selenium-Based Stacked CMOS Image Sensor with in-Pixel Pulse-Generating Operation Suitable for Single-Photon Counting

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Abstract

We propose the concept of a high-efficiency, avalanche-type, crystalline selenium (c-Se)-based CMOS image sensor with in-pixel pulse-generating operation, which provides high sensitivity, high speed, and low noise, making it suitable for single-photon counting. In this study, the first integration of c-Se-based stacked sensors with in-pixel ADCs was demonstrated in a non-photon counting mode. We confirmed the proportionality of the intensity of the output signal to the intensity of the optical input. Furthermore, the first images of 128 × 96 pixels were successfully captured.

Introduction

Photon counting is a superior imaging technology, especially under low-illumination conditions where photons reach the detector discretely. Previously, many studies have focused on the implementation of photon count imaging. Among them, single-photon avalanche diodes (SPADs) have recently attracted much attention because of their high photon detection efficiency by using Geiger-mode operation in APDs [1]. Despite some progress toward achieving compact SPAD imagers [2], there are still challenges in implementing high-spatial-resolution SPAD sensors because of their large circuit architectures.

We herein propose c-Se-based stacked CMOS image sensors with in-pixel pulse-generating operation. A single photo-generated carrier can be multiplied in high-efficiency c-Se-based APDs [3,4], and in-pixel ADCs can count the number of photons [5,6]. Combining these technologies improves the signal-to-noise ratio, leading to the realization of single-photon counting, which has advantages in the pixel size reduction and high-speed operation.

Device Design and Fabrication

Fig. 1 shows a schematic diagram of photon count imaging. An incident single photon absorbed in the photoconversion layer stacked on the CMOS circuit can be multiplied by avalanche multiplication. In contrast to conventional CMOS image sensors, the intensity of the signal can be obtained by counting the number of incident photons digitally.

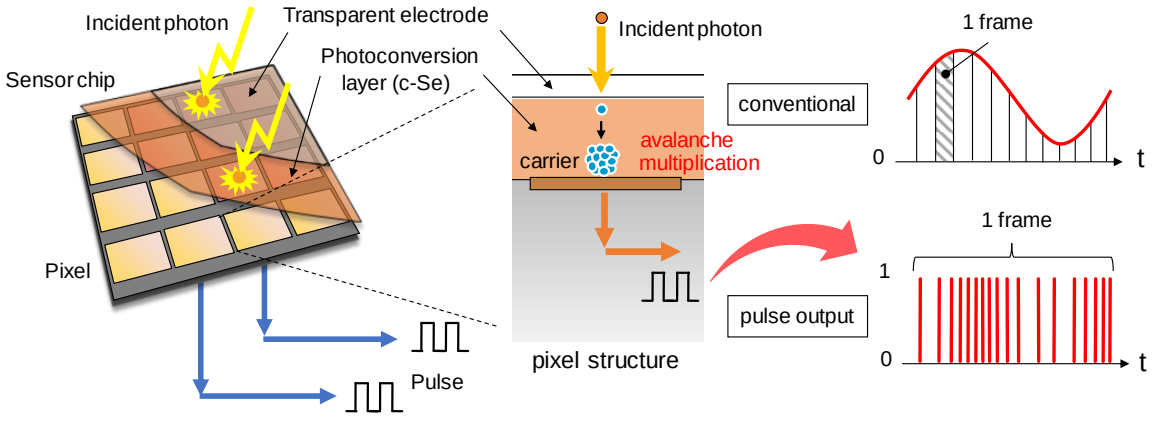

Fig. 1: Schematic diagram of photon count imaging. The incident photon absorbed in the c-Se photoconversion layer can be multiplied by avalanche multiplication. In contrast to the conventional CMOS image sensors, which detect the amount of accumulated charge as an analog quantity, the intensity of the signal can be obtained by counting the number of incident photons digitally.

Herein, we deposited highly absorptive c-Se-based photodiodes (Fig. 2(a) [7]) directly onto the CMOS circuits connected with Au pixel electrodes as shown in Fig. 2(b). Owing to the extremely high absorbance, we can reduce the thickness of the c-Se layer to 300 nm. We deposited a 20-nm-thick n-type wide-bandgap (Eg = 4.9 eV) amorphous gallium oxide (Ga_2O_3) layer to provide hole blocking from the pixel electrodes. Next, we deposited a tellurium (Te) nucleation layer and a 300-nm-thick amorphous selenium (a-Se) layer continuously at room temperature, followed by annealing to convert a-Se layer into a p-type c-Se layer [8]. Finally, a 30-nm-thick ITO layer was deposited to serve as a transparent electrode. In addition, owing to the low crystallization temperature of Se, the entire fabrication process was implemented below 200°C, enabling the direct fabrication of photoconversion layer onto CMOS circuits. A cross-sectional SEM image of the fabricated sensor is shown in Fig. 2(c). As can be seen from the figure, the smooth 300-nm-thick c-Se film clearly covers the entire pixel.

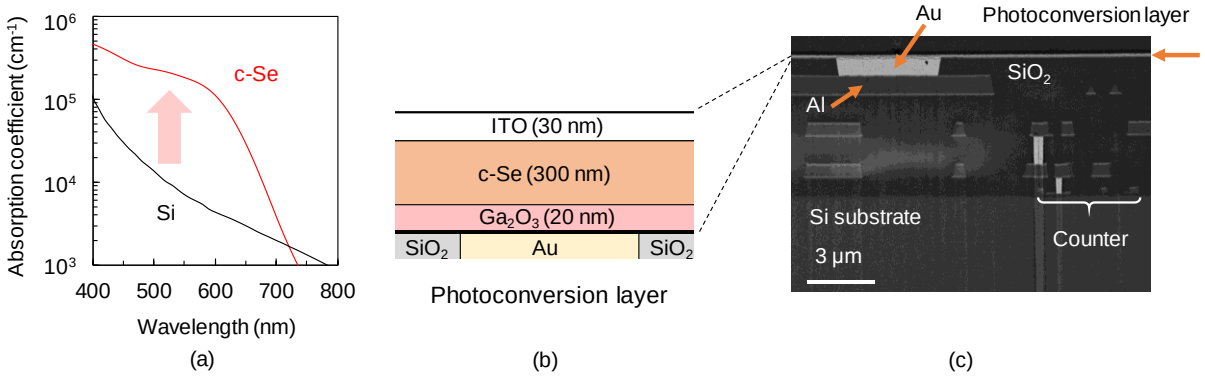

Fig. 2: (a) Absorption coefficient as a function of wavelength for c-Se and Si. (b) A cross-sectional image of the stacked CMOS image sensor. The c-Se-based photodiodes are directly deposited onto the CMOS circuits. (c) A cross-sectional SEM image of fabricated CMOS image sensor.

Fig. 3 shows the circuit diagram of the pixel. The pixel consists of a comparator, CMOS inverters, a reset transistor, and a counter. Whenever the voltage of floating diffusion (V_{FD}) reaches the threshold voltage of the comparator (V_{TH}) through photo-generated carriers, a pulse signal is created. The number of pulse signals created in a frame period is stored by an in-pixel counter. This type of ADC has advantages in terms of noise resistance and high-speed detection.

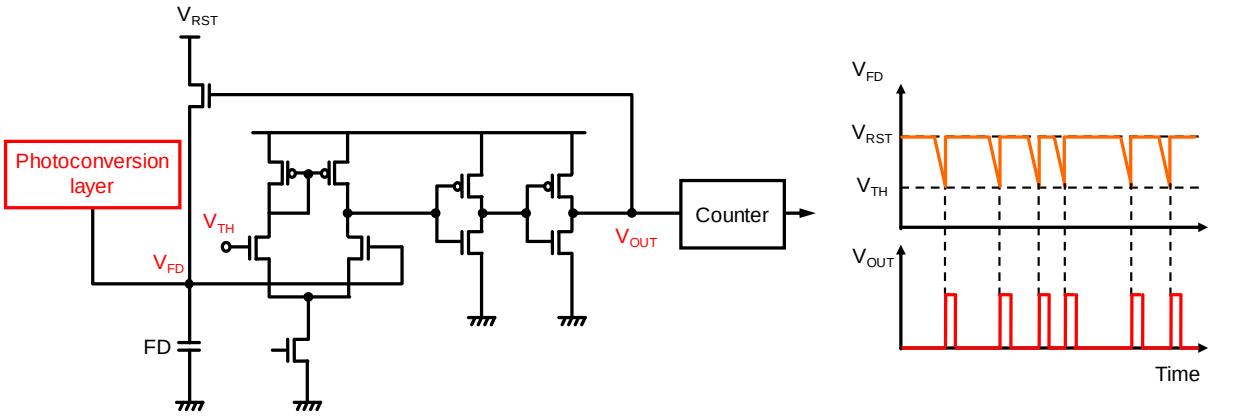

Fig. 3: The circuit diagram of the pixel. Pulse generator including a comparator and CMOS inverters converts photo-generated carriers in a photoconversion layer into pulse signals, whose number is stored by in-pixel counter.

Fig. 4(a) shows a chip photograph of the stacked image sensor. The sensor has 128 × 96 pixels, with each pixel being 61 × 61 μm^2; every pixel has a Au pixel electrode of 5-μm diameter. An enlarged pixel view and the pixel layout are shown in Figs. 4(b) and 4(c), respectively.

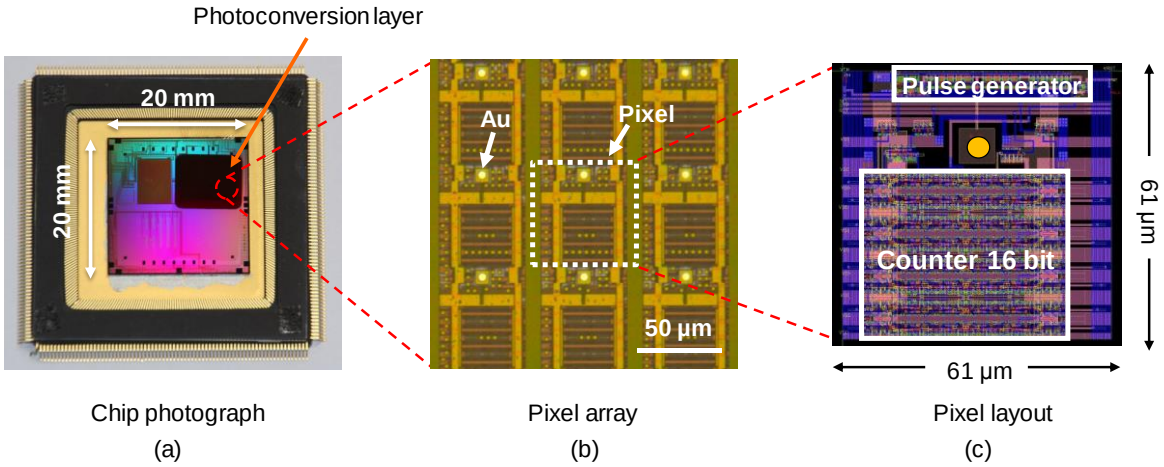

Fig. 4: (a) A chip photograph of the fabricated CMOS image sensor, which has 128 × 96 pixels, with each pixel being 61 × 61 μm^2. (b) The enlarged pixel view. (c) The pixel layout. Each pixel comprises a pulse generator and a 16-bit counter.

Measurement Results

Fig. 5(a) shows the pulse output frequency as a function of the supply voltage to the c-Se/Ga_2O_3 photodiode in the non-avalanche mode. Measurements were conducted with a reverse bias applied to the photodiodes. As shown in Fig. 5(a), the output signal intensity increases with the supply voltage. Fig. 5(b) shows the input-output characteristic of the stacked image sensor with a supply voltage of 2 V, indicating excellent linearity from 1 to 10^5 lux.

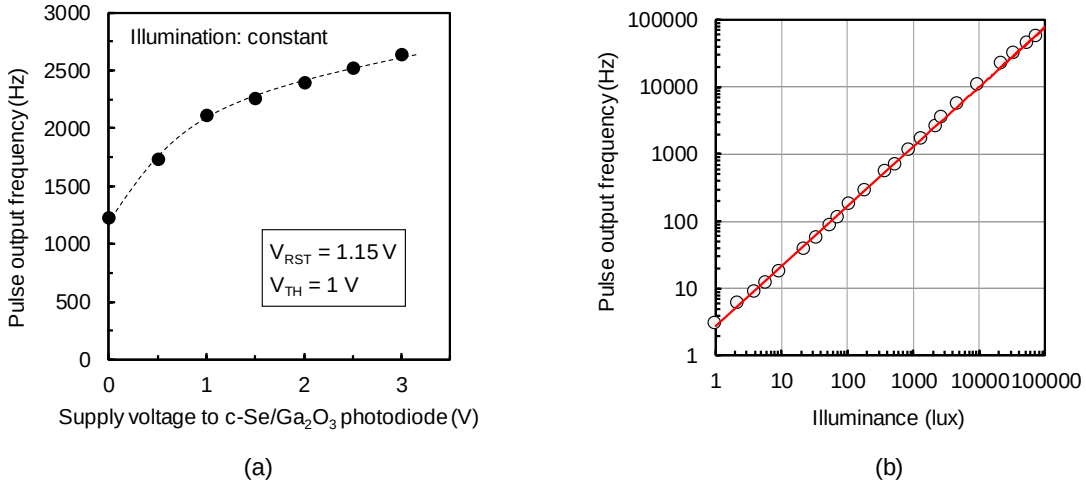

Fig. 5: (a) The pulse output frequency as a function of supply voltage to c-Se/Ga_2O_3 photodiode in non-avalanche mode. Measurements are implemented with a reset voltage of 1.15 V and a threshold voltage of 1 V. The output signal increases as the supply voltage increases. (b) The input-output characteristic of in-pixel ADC with a supply voltage of 2 V, indicating the excellent linearity from 1 to 10^5 lux.

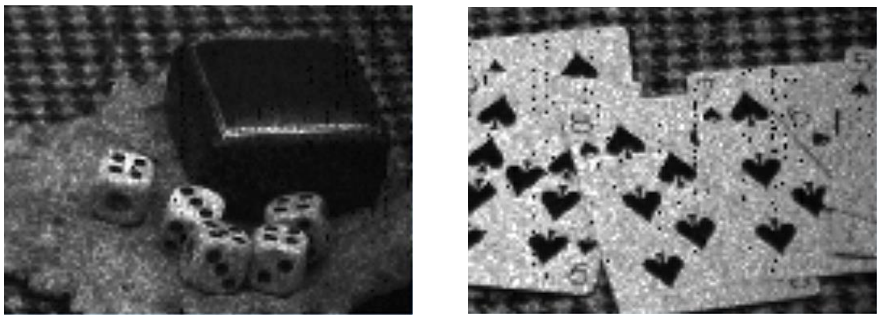

Fig. 6: The first captured images of 128 × 96 pixels in non-photon counting mode with a supply voltage of 2 V. (V_{RST} = 1.15 V)

We successfully obtained the first video images of the developed image sensor with 128 × 96 pixels in the non-photon counting mode with a supply voltage of 2 V (Fig. 6).

Conclusion

We proposed c-Se-based stacked CMOS image sensors with in-pixel pulse-generating operation. The results indicated the linear output response of in-pixel ADCs from 1 to 10^5 lux. In addition, we successfully obtained the first video images of the developed image sensors with 128 × 96 pixels in the non-photon counting mode. In the future, we will realize photon count imaging using the combined stacked CMOS image sensor.

References

[1] S. Koyama et al., "A 220 m-range direct time-of-flight 688× 384 CMOS image sensor with sub-photon signal extraction (SPSE) pixels using vertical avalanche photo-diodes and 6 kHz light pulse counters," in Proc. Symp. VLSI Circuits, Jun. 2018. pp. 71–72.

[2] A. Ximenes et al., "A 256× 256 45/65nm 3D-stacked SPAD-based direct TOF image sensor for LiDAR applications with optical polar modulation for up to 18.6 dB interference suppression," in Proc. ISSCC Dig. Tech. Papers, Feb. 2018. pp. 96-98.

[3] S. Imura et al., "Low-voltage-operation avalanche photodiode based on n-gallium oxide/p-crystalline selenium heterojunction," Appl. Phys. Lett., vol. 104, no. 24, pp. 242101–242101–4, 2014.

[4] S. Imura et al., "High sensitivity image sensor overlaid with thin-film crystalline-selenium-based heterojunction photodiode," in IEDM Tech. Dig., Dec. 2014, pp. 4.3.1–4.3.4.

[5] M. Goto et al., "Three-dimensional integrated CMOS image sensors with pixel-parallel A/D converters fabricated by direct bonding of SOI layers," in IEDM Tech. Dig., Dec. 2014, pp. 4.2.1–4.2.4.

[6] M. Goto et al., "A three-dimensional integration technology with embedded Au electrodes for stacked CMOS image sensors," in Proc. IISW, 2015, pp. 48–50.

[7] S. Imura et al., "High-sensitivity image sensors overlaid with thin-film gallium oxide/crystalline selenium heterojunction photodiodes," IEEE Trans. Electron Devices, vol. 63, no. 1, pp. 86–91, 2016.

[8] T. Nakada et al., "Efficient ITO/Se heterojunction solar cells," Jpn. J. Appl. Phys., vol. 23, no. 8, pp. L587–L589, 1984.