R30

A High Optical Performance 2.8μm BSI LOFIC Pixel with 120ke$^-$ FWC and 160μV/e$^-$ Conversion Gain

Ken Miyauchi[†], Shunsuke Okura[†], Kazuya Mori[†], Isao Takayanagi[†], Junichi Nakamura[†] and Shigetoshi Sugawa[‡]

[†]Brillnics Japan Inc., 6-21-12 Minami-Oi, Shinagawa-ku, Tokyo, 140-0013 Japan

[‡]Graduate School of Engineering, Tohoku University, 6-6-11-811, Aza-Aoba, Aramaki, Aoba-ku, Sendai, Miyagi, 980-8579 Japan

Contact: Ken Miyauchi: phone:+81-3-6404-8066, fax:+81-3-5767-5568, email: miyauchi.ken@brillnics.com

ABSTRACT

In this paper, we report about a prototype CMOS image sensor with a 2.8μm back side illuminated (BSI) pixel that employs the lateral overflow integration capacitor (LOFIC)[5]-[8] to further expand dynamic range of our reported sensors[1]-[4]. Full well capacity of 120ke$^-$ and conversion gain of 160μV/e$^-$ have been achieved. For high optical performance with the BSI structure, an n-layer of the deep photodiode under LOFIC is formed. Owing to this structure, 70% peak quantum efficiency and 91% angular response at ±20° have been achieved without blooming.

INTRODUCTION

Achieving both high sensitivity and high dynamic range (DR) is required for many imaging applications, especially for security/surveillance applications.

Recently, over 85dB single exposure high dynamic range (SEHDR) CMOS image sensors (CIS) with high full well capacity (FWC) photodiode (PD)[1]-[4] were reported. However, it is difficult to drastically increase the PD FWC further. Thus, one of solutions for over 90dB SEHDR is LOFIC technology[5]-[8]. In the LOFIC CIS, the floating diffusion (FD) capacitor (C_{FD}) and the LOFIC can be designed independently by only adding the LOFIC and a switch between FD and LOFIC. As a result, high sensitivity by minimized C_{FD} and high FWC by maximized LOFIC have been achieved at the same time. This advantageous characteristic resolves the trade-off between high FWC and high sensitivity that surely exists in the conventional CISs.

However, the conventional LOFIC pixel still has a disadvantage that is low optical performance compared to the typical 4Tr. pixel because the optical fill factor of the PD is lower due to the area occupation by the LOFIC.

In this paper, a prototype chip of a new LOFIC pixel built in BSI process technology to improve optical performance is presented.

CONCEPT AND OPERATION

Fig. 1 (a), (b) and (c) show a circuit schematic, a timing diagram and potential diagram of the LOFIC pixel, respectively. Compared with conventional 4Tr. pixels, there are an additional switch (SG) and the LOFIC (CS). To achieve high FWC, the LOFIC pixel accumulates all the overflow photoelectrons from PD during exposure in CS until signal is read out. At the first stage of readout, the reset and signal levels are read out in a high gain mode (HCG). Then, the photoelectrons in the PD and FD/CS are mixed and the mixed signal is read out in a low gain/high FWC mode (LCG). By using the HCG signals for low illuminance conditions and the LCG signals for high illuminance, expanding DR is realized.

Fig. 2 (a) shows a cross sectional view of a conventional front side illuminated (FSI) LOFIC pixel. Increasing PD fill factor is limited by the large CS in a pixel. On the other hand, in our proposed structure using the BSI technology (Fig. 2 (b)), there is a deep n-layer under the CS for the following three purposes;

(i)To increase fill factor for high optical performance,

(ii)To expand the PD area for high FWC in HCG,

(iii)To reduce the neutral region under the CS for crosstalk suppression.

Also, the deep n-layer is laid out in a square shape to obtain optical symmetry.

To collect all the photoelectrons generated in the BSI side, we designed the dopant concentration of the deep n-layer lower than that of the n-layer of the FSI side and formed concentration gradient in the deep n-layer to generate electric field towards FSI side. In addition, an n-layer under the transfer gate (TG) and the SG gate is formed to obtain the overflow path from PD to CS and to prevent blooming. The potential barrier at the overflow path is designed lower than that of the pixel-to-pixel isolation.

Also, to remove leakage currents that are generated at

shallow trench isolation (STI) and the gate oxide surface, PN junction isolation around FD instead of STI, and buried overflow path under the TG and the SG are introduced.

EVALUATION RESULTS

Fig. 3 shows photoelectric conversion characteristics of this prototype chip. Two curves exhibit good linearity. We obtained 160μV/e^- conversion gain (C.G.) and 7ke^- FWC in HCG, and 120ke^- FWC in LCG. Compared to our previous devices, we have achieved to increase LCG FWC without reduction of HCG C.G.. Because signal electrons at the conjunction point of HCG and LCG signals are 6ke^-, which is near the HCG saturation, we have achieved 38dB signal to noise ratio at that point.

Fig. 4 and Fig. 5 show the measured results of quantum efficiency (Q.E.) and angular response (AR), respectively. Although the microlens structure of this prototype chip is not fully optimized, 70% peak Q.E. and 91% AR at ±20° have been achieved. These values are comparable to those of our previous sensors[1]-[4]. In addition, Q.E. in LCG matches that of HCG, which suggests that all the overflow photoelectrons from PD are transferred to FD and CS without blooming due to the overflow path.

Fig. 6 (a) and (b) show the measured results of Gr/Gb ratio. Under the blue light condition, less than 2% deviation has been achieved and this suggests that more than 98% photoelectrons generated in the BSI side under the CS are collected in the FD without crosstalk.

Fig. 7 shows HDR sample images captured by this prototype chip. We captured some color objects which are illuminated by the halogen light or miniature light. Even for the scene of 100dB differences in brightness and darkness, this prototype chip captured all the color objects without halation.

CONCLUSION

A prototype chip with a BSI LOFIC pixel has been demonstrated.

Fig. 8 and Table 1 show a chip micrograph and a performance comparison, respectively. We have achieved 120ke^- FWC and 160μV/e^- C.G. with the smallest non-shared LOFIC pixel. Through optimization of microlens structure, we expect over 70% peak Q.E. and over 91% AR at ±20° without blooming will be achieved. Also, assuming the same column signal chain of our previous sensors[1]-[4], read noise of less than 1e^- and over 100dB DR will be obtained. These techniques are readily available for new SEHDR CIS's for security and IoT cameras.

ACKNOWLEGMENT

The authors gratefully acknowledge the support by Yutaka Sato in acquiring HDR images.

REFERENCES

[1] I. Takayanagi, et al., "An 87dB single exposure dynamic range CMOS image sensor with a 3.0μm triple conversion gain pixel," Proc. IISW, pp.274-277, 2017

[2] I. Takayanagi, et al., "An over 90 dB intra-scene single-exposure dynamic range CMOS image sensor using a 3.0 μm triple-gain pixel fabricated in a standard BSI process," Sensors, 18, 203, 2018

[3] K. Mori, et al., "Back side illuminated high dynamic range 3.0μm pixel featuring vertical p-n junction capacitance in a deep pinned photodiode," Proc. IISW, pp.169-172, 2017

[4] S. Tanaka, et al., "Single exposure type wide dynamic range CMOS image sensor with enhanced NIR sensitivity," ITE Transactions on Media Technology and Applications, pp.195-201, 2018

[5] S. Sugawa, et al., "A 100dB dynamic range CMOS image sensor using a lateral overflow integration capacitor," Proc. ISSCC, pp.352-353, 2005

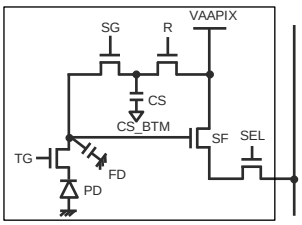
[6] S. Sakai, et al., "Pixel scaling in complementary metal oxide silicon image sensor with lateral overflow integration capacitor," Japanese Journal of Applied Physics, vol. 49, 04DE03, 2010

[7] H. Sugo, et al., "A deadtime free global shutter CMOS image sensor with in-pixel LOFIC and ADC using pixel-wise connections," Symposium on VLSI Technology, pp.224-225, 2016

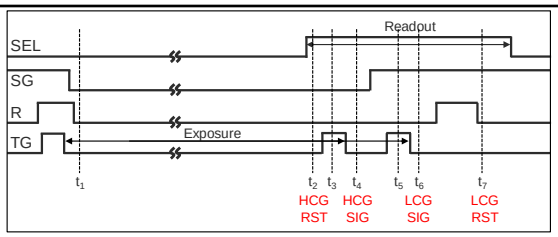
[8] Y. Sakano, et al., "224-ke saturation signal global shutter CMOS image sensor with In-pixel pinned storage and lateral overflow integration capacitor," Symposium on VLSI Technology, pp.C250-C251, 2017

[9] S. Iida, et al., "A 0.68e-rms random-noise 121dB dynamic-range sub-pixel architecture CMOS image sensor with LED flicker mitigation," Proc. IEDM, pp.10.2.1-10.2.4, 2018

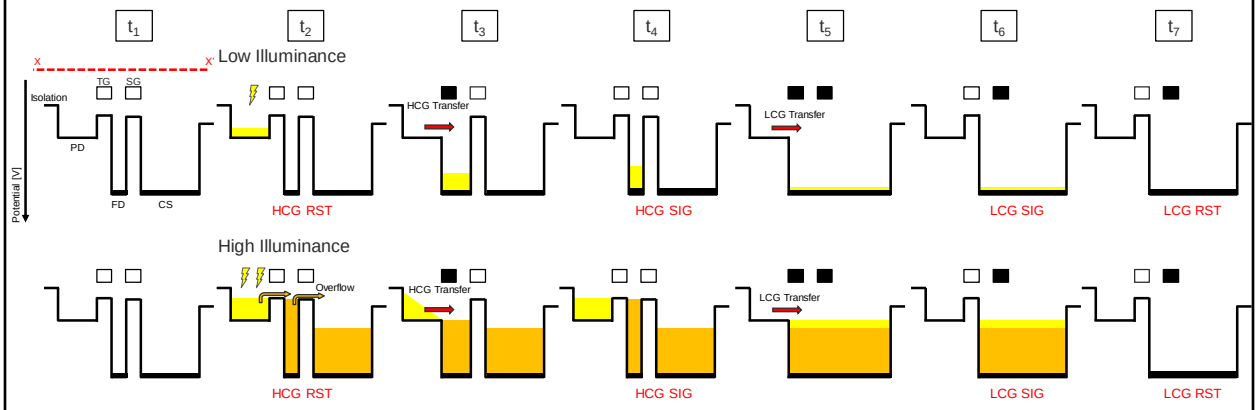
[10] V. C. Venezia, et al., "1.5μm dual conversion gain, backside illuminated image sensor using stacked pixel level connections with 13ke- full-well capacitance and 0.8e- noise," Proc. IEDM, pp.10.1.1-10.1.4, 2018



(a) Pixel circuit schematic

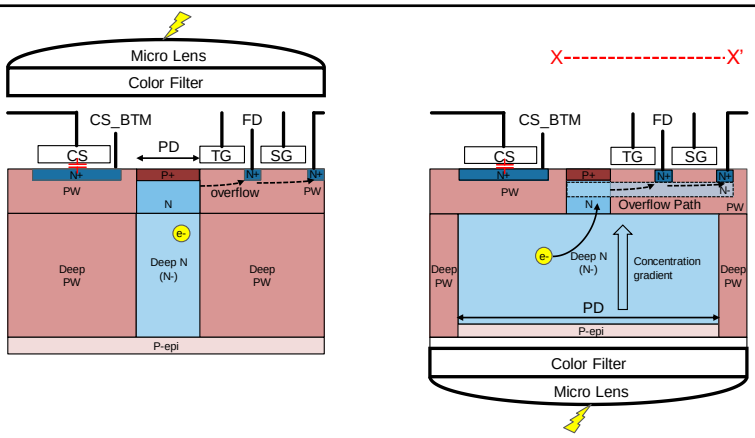


(b) Timing diagram



(c) Potential diagram

Fig. 1 Pixel circuit and timing diagram



(a) Conventional FSI LOFIC (b) This work : BSI LOFIC

Fig. 2 Cross sectional view of pixel

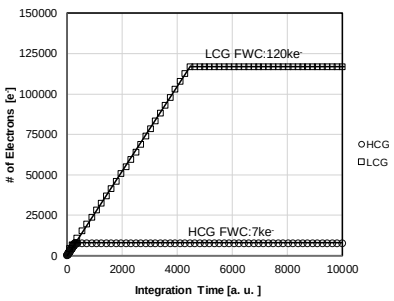


Fig. 3 Photoelectric conversion characteristics

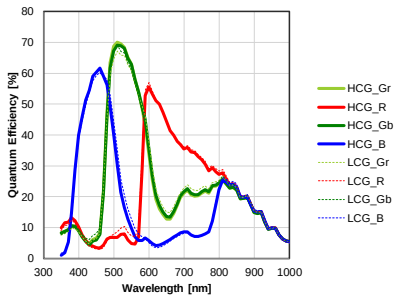


Fig. 4 Quantum efficiency

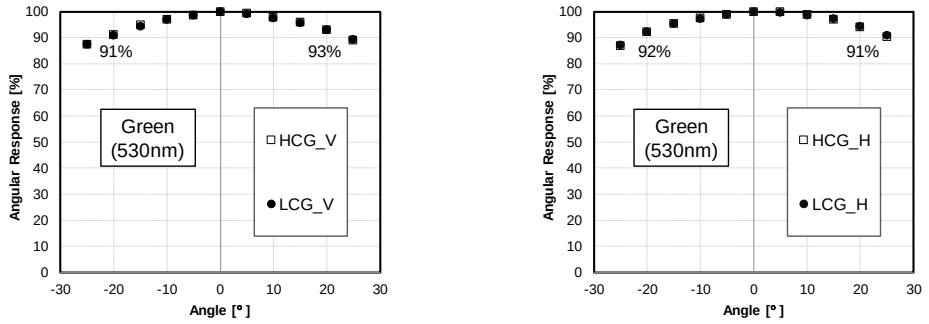
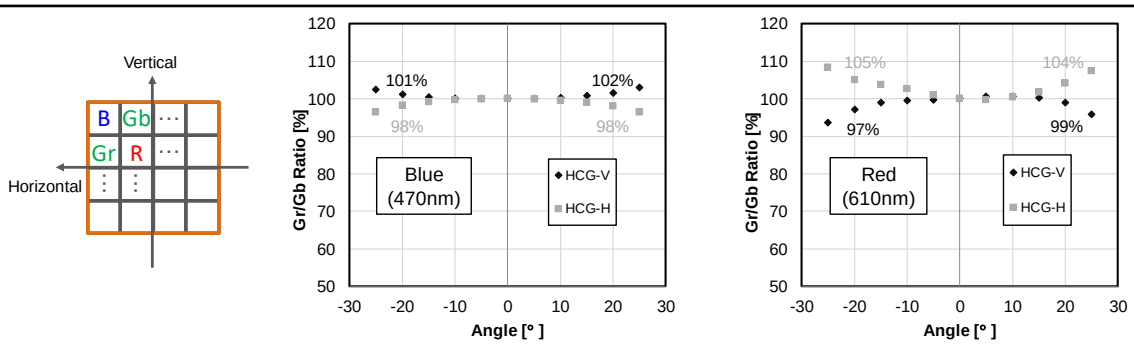
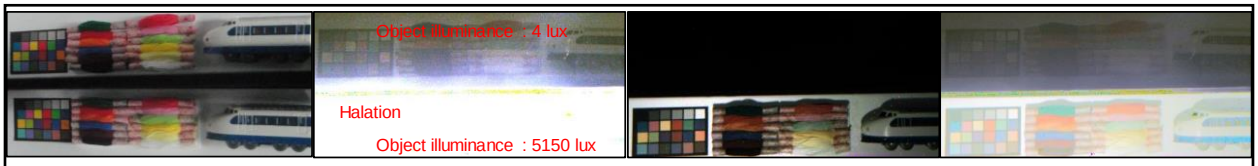


Fig. 5 Angular response



(a) Blue light **(b) Red light**

Fig.6 Angular dependence of Gr/Gb ratio



(a) Color Objects **(b) HCG image** **(c) LCG image** **(d) HDR image**

Fig. 7 Sample images : 100dB illuminated objects

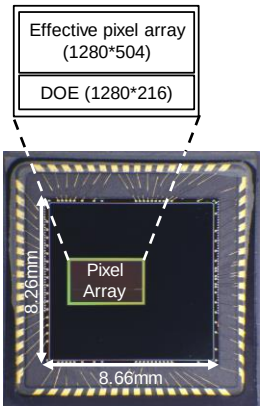


Fig. 8 Chip micrograph

Table 1 Performance comparison

	This Work	[9] @IEDM2018	[8] @VLSI2017	[7] @VLSI2016	[6] @JJAP	[10] @IEDM2018 NOT LOFIC	[1]-[4] @IISW2017 NOT LOFIC
Process	BSI (65nm 1P4M)	90nm 4Cu1AL	FSI (180nm FEOL/90nmBEOL)	Stack (SOC:45nm 1P4M/ASIC:65nm 1P5M)	FSI (180nm 2poly-3metal)	Stack	BSI (65nm 1P4M)
VAAPIX	2.8V	2.9V	3.3V	3.3V	N/A	N/A	2.8V
Pixel Size	2.8μm	3.0μm	3.875μm	6.6μm (1.65μm sub-pixel $*4^{H}*4^{V}$)	3.0μm	1.5μm	3.0μm
# of Pixels	1280*504	1920*1200	1.3M	640*476	1280*960	8M	1928*1088
FD/SF Shared	1PD/FD	1PD/FD	1PD/FD	16PD/FD	2PD/FD	2PD/FD	2PD/FD
HCG FWC	7ke$^-$	10ke$^-$	5ke$^-$	N/A	N/A	4.5ke$^-$	N/A
LCG FWC	120ke$^-$	78.5ke$^-$	224ke$^-$	220ke$^-$	69ke$^-$	13ke$^-$ (PD Saturation)	45ke$^-$ (PD Saturation)
FWC (/1μm^2)	15306	8722	14918	5051	7667	5778	5000
HCG-C.G.	160μV/e$^-$	N/A	N/A	N/A	84μV/e$^-$	200μV/e$^-$	152μV/e$^-$
LCG-C.G.	10μV/e$^-$	N/A	N/A	N/A	N/A	20μV/e$^-$	21μV/e$^-$
AR @±20°	91%	N/A	N/A	N/A	N/A	N/A	90.4%
Q.E.	70%@Peak	N/A	N/A	N/A	N/A	80% @Peak	78.8% @Peak