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A scalable 12b-16b charge-domain multi-slope column ADC for HDR imagers with 86dB DR at 1 µs conversion time

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Introduction

New and upcoming video standards require ADCs with high conversion rates to support high frame rate, and high bit-depth to achieve high dynamic range (HDR). The single-slope architecture is used extensively in image sensors thanks to its low complexity and small footprint of the column circuitry. However, each additional bit halves the obtainable frame-rate due to limitation of the counter frequency. Multi-slope architectures have been introduced to improve this. In [1] an architecture is presented with 8 parallel ramps, while [2] uses a variable ramp to exploit the pixel shot-noise property. To further improve on these, this paper proposes an architecture that overcomes the speed/resolution trade-off by using three ranges in a sub-ranging charge-based ADC.

Architecture

An overview of the ADC is shown in Fig. 1. It consists of two sample blocks, an OTA, comparator CMP, digital control and three charge pumps with different stepsizes.

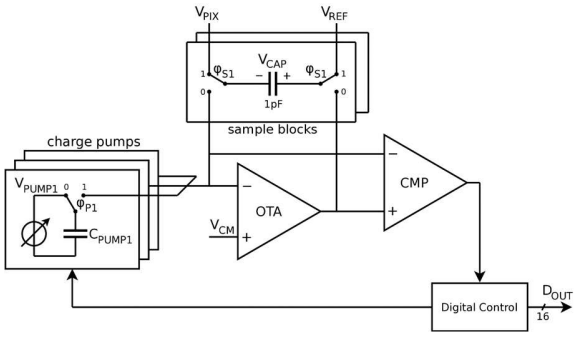

Fig. 1: Overview of the charge-based sub-ranging multi-slope architecture.

The corresponding signals are shown in Fig. 2. First, the pixel voltage V_{PIX} is sampled with respect to the reference voltage V_{REF} on capacitor V_{CAP} in the sample block (φ_{S1}=1). Next, the capacitor is connected to the OTA (φ_{S1}=0) and the AD conversion starts. Based on the comparator output, charge pump 1 is activated (φ_{P1}: 0→1→0) causing big voltage steps (V_{STEP1}) down on V_{CAP}, until V_{CAP} < 0. Next, charge pump 2 is used for moderate steps (V_{STEP2}) up until V_{CAP} > 0, and finally small steps (V_{STEP3}) down are made using charge pump 3. Based on the number of steps in each range, the output code is calculated.

By using two sample blocks, column sampling and conversion happen in parallel, improving the frame rate. In this scalable design there are (a maximum of) 64 steps in ranges 1 and 2 (6b + 6b) and 16 steps (4b) in range 3. In 16b mode the conversion time is 1 µs, while in 12b mode (4b + 4b + 4b) the conversion time is 0.5 µs.

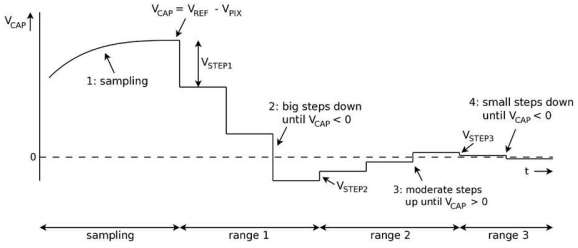

Fig. 2: Signal sampling and AD conversion in three ranges.

Calibration

To obtain good DNL, the ratio between the different voltage steps must be accurate: In 16b mode, V_{STEP2} = V_{STEP1}/64 and V_{STEP3} = V_{STEP2}/16. However, due to PVT variation and limited matching of the small pump capacitors, the voltage steps deviate. To make the step ratios accurate, an on-chip calibration mechanism is implemented, see Fig. 3. V_{PUMP1} is a digitally adjustable global voltage determining V_{STEP1} and the full-scale range V_{FS} of the ADC, which can be set between 0.1V and 3V. The calibration procedure for V_{STEP2} is as follows: φ_{RESET} is pulsed (briefly activated) to make V_{CAP}=0, φ_{P1} is pulsed to make one range 1 step down and φ_{P2} is pulsed 64 times to make 64 range 2 steps up. After this, ideally V_{CAP}=0. To achieve this, the calibration charge-pump ($\varphi_{CALPUMP}$) is used to either increase or decrease V_{CAL} (=V_{PUMP2}) based on the comparator output. After several iterations of this procedure, V_{STEP2} is matched to V_{STEP1} with the desired ratio. Next, V_{STEP3} is calibrated to match V_{STEP2}/16 in the same way. The actual values of the (pump) capacitors, charge injection of the pump switches, buffer offset and the value of V_{CM} are all within the loop and compensated for by the calibration. A calibration step takes about the same time as a regular conversion and it is performed in the vertical blanking interval after a frame conversion to compensate for VT variation and leakage of C_{CAL}. After power-up (V_{CAL}=0), initial calibration is completed within 10ms.

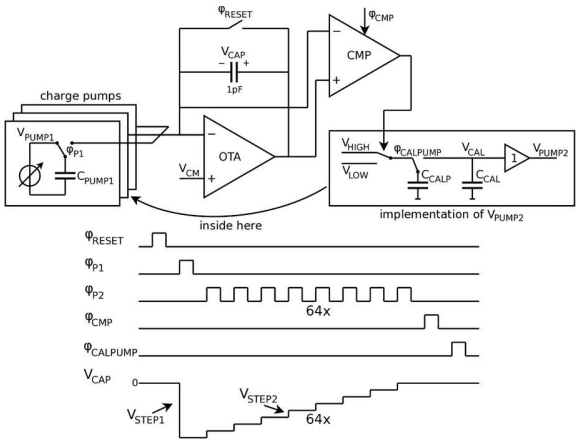

Fig. 3: Calibration circuitry and operation to match 64 V_{STEP2} to V_{STEP1}.

Reduced conversion time

To reduce the conversion time, both 6b ranges are extended with an offset circuit, see Fig. 4. At conversion start, the offset circuit is activated and introduces an offset of ~4.5 steps. After each comparison, 4 steps are now made instead of 1, until V_{CAP} < 0. After turning off the offset, a maximum of 5 conversions with single steps is required to reach V_{CAP} < 0 again. The additional 5th step creates ±½ step over-range and relaxes the requirement of the offset circuit to ±10%. This implementation reduces the number of comparisons in ranges 1 and 2 from 63 to 15+5, saving conversion time and power.

Noise

The ADC has 4 dominant noise sources: sample noise, pump noise, comparator noise and crosstalk. By using a unity gain buffer instead of the OTA, sample noise is close to kT/C = 64 µV. Each pump action adds a small amount of kT/C noise to V_{CAP} proportional to $\sqrt{C_{PUMP}}$. The pump capacitors are therefore minimized to 34 fF for range 1 and 4 fF for ranges 2 and 3. Smaller values

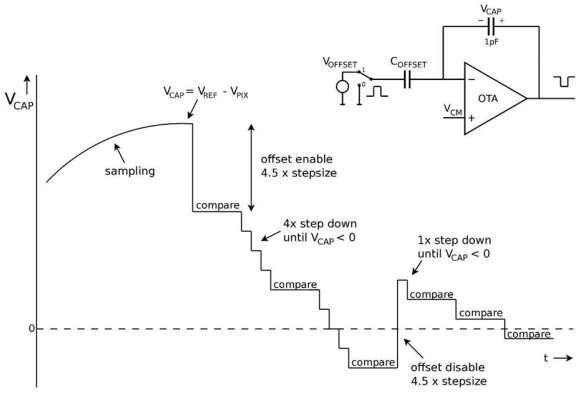

Fig. 4: Offset circuit and corresponding wavevorms of a 6b conversion of ranges 1 and 2.

would make V_{PUMP1} too large or cause accuracy issues in ranges 2/3. This yields 17 µV noise for each range 1 step and 6 µV for each range 2/3 step, resulting in maximal 64 µV pump noise for low-light signals (< 1/16 V_{FS}), and 146 µV for full-scale signals. This fits nicely with the pixel shot-noise characteristic.

To limit the contribution of comparator noise, digital averaging is used, reducing the effective comparator noise. Crosstalk from supply and other lines also impacts the overall noise performance and is hard to mitigate due to the large aspect ratio of stacked column parallel ADC (20 µm x 1250 µm). Thanks to the large feedback factor, OTA noise is largely common for the comparator and therefore it has little impact.

Implementation

The column ADC is applied in a 4224 x 2248 prototype image sensor with 2.5 µm 2x2 shared pixels in 0.18 µm 4M1P CMOS technology, see Fig. 7. Both above and below the pixel array, there are 1056 column ADCs. The double-sided pitch of the column ADCs is 5 µm, so there is 1 ADC per (shared pixel) column.

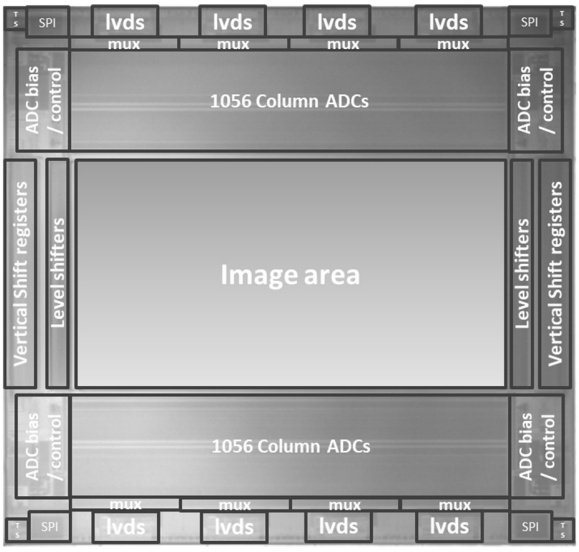

Fig. 7: Chip photo, measuring 14.5mm x 13.6mm, top part identical to bottom.

Digital Double Sampling (DDS) [2] / digital CDS is used to cancel reset noise, FPN, VT variations and 1/f noise of both pixel and ADC. It requires two AD conversions with associated noise and conversion time; however, it avoids noise and time involved in analog CDS.

Measurements

Fig. 8 shows a 16b video still with an ADC conversion time of 1 µs, and Fig. 9 shows an artefact-free shot-noise curve. The ADC noise is 180 µV measured using an internal reference generator with V_{FS} = 3V and all 2112 ADCs operational. Subtracting the simulated noise of the reference generator (100 µV) yields an estimated ADC noise of 150 µV, resulting in a dynamic range of 86dB.

Fig. 8: A 4224 x 2248 video still with 1 µs ADC conversion time.

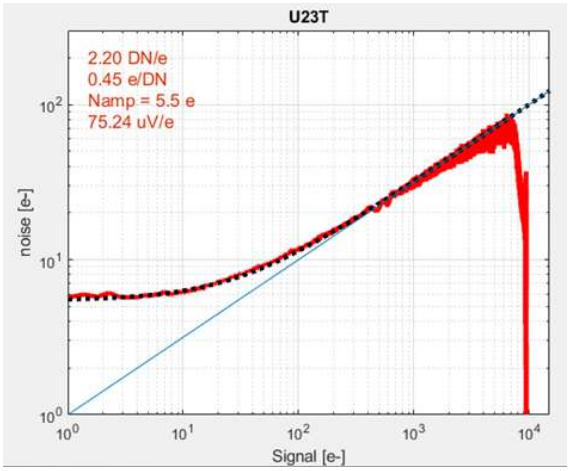

Fig. 9: Artefact-free shotnoise curve.

The ADCs consume 3.2W in 16b mode (1.5 mW per ADC) from 1.8V/2.5V/3.3V including reference, bias and buffering.

Fig. 10 shows a transfer curve indicating good INL; the bend is due to non-ideal large signal behavior of pixel and column. The global shape of the sub-sampled histogram (bottom) is caused by the scene, while the limited local variation in counts shows no significant DNL artefacts. This is in line with the shotnoise curve.

Fig. 11 shows a comparison with state-of-the-art. This ADC has the highest bit-depth, input range and DR, making it attractive for HDR video, while its short conversion time in a slower technology demonstrate the high-speed potential of this architecture.

Conclusion

This paper introduces a new ADC architecture, capable of both high dynamic range (86dB at 1 µs conversion time) and high-speed imaging with conversion times down to 0.5 µs.

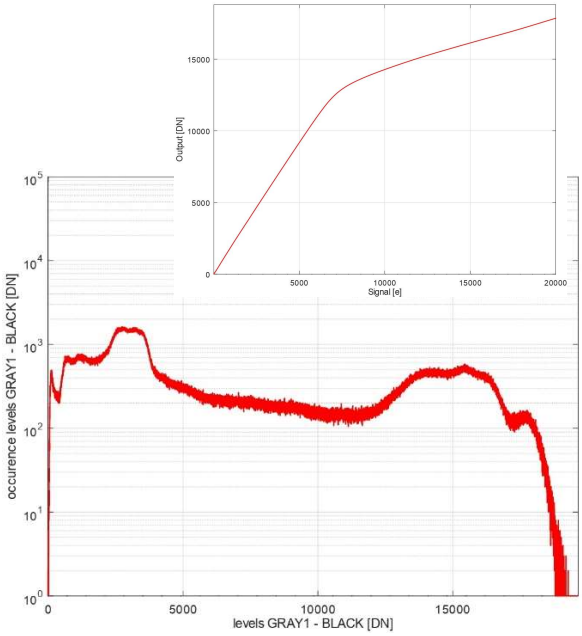

Fig. 10: transfer curve (top) and ADC histogram (bottom).

	unit	This work	[3]	[4]	[5]
Process	nm	180	90	90	45/65
Number of bits	-	**16**	14	12	12
Pixels (H)	-	4224	3840	**8192**	7728
Pixels (V)	-	2160	2160	2160	**4368**
Frame rate	fps	120	**480**	120	240
Total power	W	3.2	5.2	3.0	3.0
Power per ADC (incl misc)	mW	1.5	1.36	**0.73**	0.78
Conversion time	µs	1.0	3.5	6.9	**0.95**
Analog gain	-	1.0	1 / 4	1.0	1/0
Noise	e^-	5.5	4.6	**4.4**	4.5
Noise ADC	μV_{RMS}	150	**140**	250	414
Full-scale range	mV	**3000**	923	1197	524
Dynamic range	dB	**86.0**	76.3	74.4	62.1

Fig. 11: Comparison table with state-of-the-art.

References

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