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Image Sensor with Panel Readout and Serialization using Multiple PLLs

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I. INTRODUCTION

Until recently, the world's highest frame rate continuously running image sensors were CMOS sensors with multi-tap Analog outputs. This development was fully custom so no much knowledge other than private talks and the final camera specs exists about these sensors. The fastest of the analog sensors have the data rate of about 25Gpix/s and the number of outputs of over 256. It is time now for Digital sensors to emerge and beat the Analog sensors in the data rate. Until recently, the limitations in developing of the ultra-high speed digital sensors were size, power, and, simply, the absence of the suitable digital platform. Our prediction is that the digital sensors have matured enough and will soon dominate the high speed camera market. In this paper, we will propose one capable digital architecture, give some implementation details and present the status of the work.

II. AN ULTRA- HIGH SPEED DIGITAL ARCHITECTURE

The path to higher frame rates, say 10,000 Fps and more, in continuous timing digital CMOS image sensors has rather been straightforward [1-3]:

- Use column parallel ADCs with multiple ADCs per pixel pitch
- Use multiple column read lines enabling several rows of the imager being read at once

With growing number of vertical read lines and growing number of ADCs, less sways are required to read the entire image down; the higher is the frame rate. Less obvious would be the architecture of the sensor memory and of the output interface.

A hypothetical multi-tap Analog sensor having 250 outputs at 100 MHz delivers the data amounting to, say 250 Gbit/s, so the equivalent Digital sensor should approximately have 250 digital outputs operating at 1 GHz each.

So, in the end, one would need a massive array of serializers operating between the sensor memory and the output ports, say, SLVS ports, where each serializer is a 1GHz circuit.

Multiple ADCs per pixel, say, 8 or 16, dictate large pixel size. The large pixel is in line with the requirement of high sensitivity of the pixel used for ultra-high speed imaging. But the large pixel results in the large sensor size.

So imagine the sensor of a 20-30 mm size having hundreds of serializers spread over the sensor periphery and operating at the 1GHz rate. This monstrous architecture requires an efficient clocking and synchronization scheme to align the data all over the chip.

We developed a sensor (The concept [4] is drawn in Fig.1.) which resolves the above difficulty in the following way:

- Memory keeping data from ADCs is split into the number of memory blocks
- Each memory serves a vertical block of pixels (panels) in the image sensor
- Each memory-block has a built-in controller

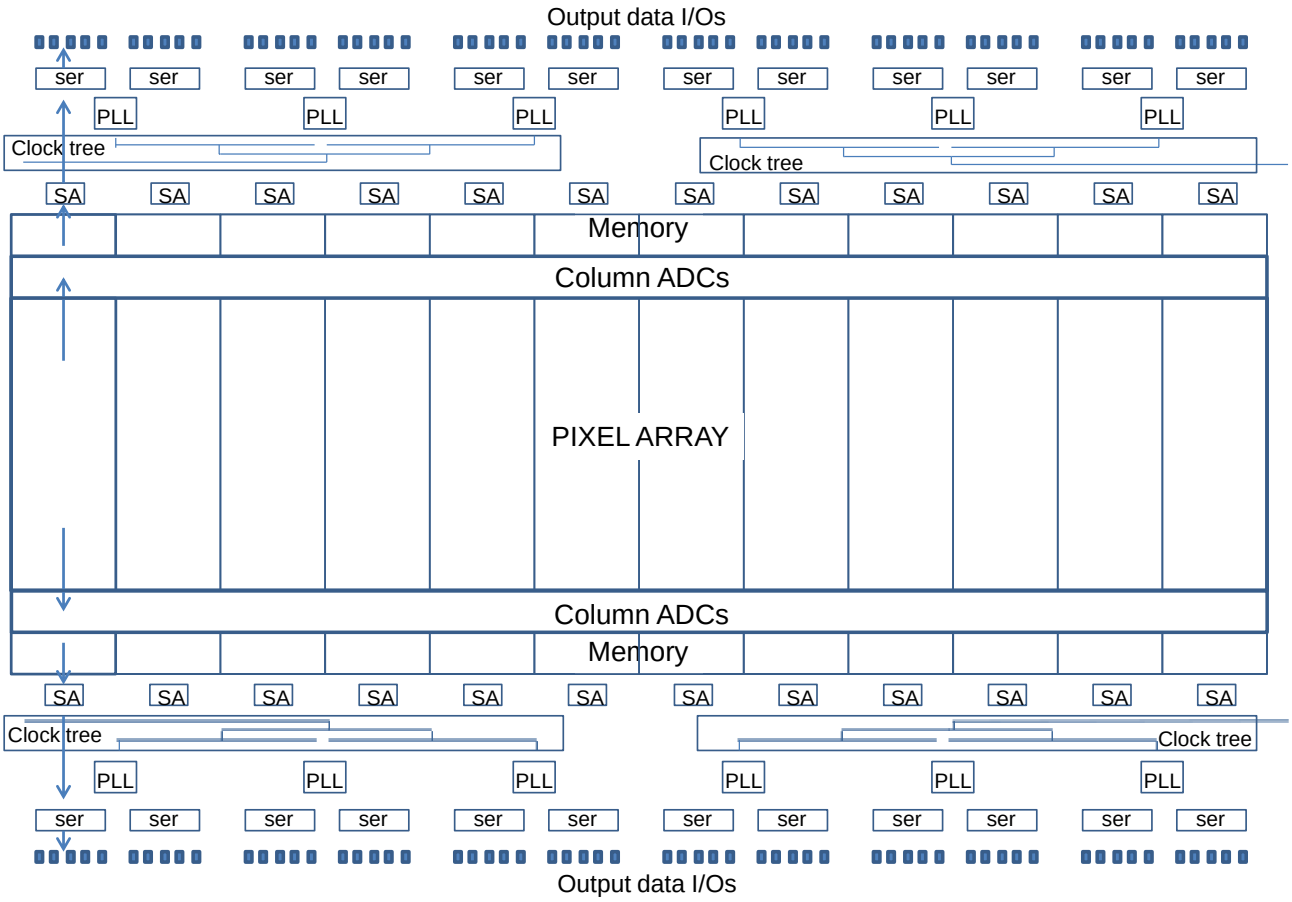

Fig.1. Architecture of the Ultra-High Speed Sensor where pixels are read up-down in panels. Here, "SA"-memory sens-amp block, "ser"- serializer block.

- Each memory block sends data to its serializer
- Each memory block has its own PLL generating waveforms for the serializers
- Data from the serializers goes to SLVS drivers
- The only signals which are distributed over the sensor through a carefully designed Clock Tree are a) Low frequency Master Clock and b) initialization signal for memory controllers.

So, the GHz signals and controls are distributed only locally, between the PLL, the serializer and the related output I/O drivers.

A single Master clock (in this chip coming from 4 corners, assures all PLLs are locked to the same time reference.

III IMPLEMENTATION

The architecture with multiple ADCs per column of the pixels gives the opportunity to have a family of sensors with various resolution by shrinking the pixel size in half.

We first designed a 1.2Mpix sensor with a 15.6um pixel and 8 ADCs per column. Then we replaced the pixel with the 7.8um one. It fit into the same readout with 4 ADCs per its column. Thus we got a 5MPix

sensor. We can expand this family further by developing a 3.9um pixel and having a 20Mpix sensor. The principle is clearly seen from the drawing in Fig.2.

In these designs we used the Floating Gate global shutter pixel Fig.3. we reported earlier [5-6].

The column ADC circuit has also been re-used from the previous designs [6-7], with a tighter new pitch. We did not change the process, and still used an older 0.18um CMOS sensor process.

The details of the memory, PLL, serializers and output drivers are not discussed in this paper. Some more details could be found in [4].

Table below shows expected specifications from 2 sensors.

	Sensor 1	Sensor2
Process	UMC CIS18	
Resolution	1.2MP, 1280x960	5MP, 2560x1920
Pixel	15.6um 7T GS	7.8um 7T GS
Conversion gain	60 uV/e-	80uV/e-
Noise	10e-	10e-
Shutter efficiency	99.9%	99.9%
Frame Rate, max	12,000 Fps	3,000 Fps
ADC	3.9um, 10b	
Output	120 SLVS ports	
Data Rate	1.6 GHz	
Clock, max/min	200/100MHz	
Package	478-pin uPGA	

IV RESULTS

At this time, both sensors were manufactured, with 1.2Mpix sensor having gone through the 2nd revision, but both have not been characterized yet.

The big obstacle in this sort of a sensor development is not the sensor per se, but the characterization camera. The development of the camera to read from such a sensor may take several years. We've got a simple camera (Fig.4.) which runs up to the sensor ½ of the maximum speed, and one of the customers has recently developed a demo board which could run the sensor at the maximum speed of 200 MHz (1.6 GHz data).

The 1.2Mpix sensor showed a good performance at the maximum data rate. The 5Mpix sensor, which did not undergo the modification, operates at ¾ of the maximum data rate.

Fig.5. shows the images taken from the 1.2Mpix sensor at 12,000 Fps in the customer's board. We will soon get the new revision of the 5Mpix sensor which should run at the rate of 3,000 Fps

V CONCLUSION

High speed CMOS sensor architecture based on multiple column ADCs per pixel pitch is capable to grow the frame rate by employing more and more ADCs per column. This is not fantastic in view of finer 65nm and 90nm processes becoming available to CMOS sensor designers.

With the output data rate exceeding 1 GHz, and using more and more digital outpits from the sensor, we found an elegant solution which allows to keep the Giga-Hertz signals within the close range between the local memory, local PLL, serializers and local output pads.

The pixel array is read in blocks of vertical stripes (panels) where each panel has its own autonomous readout with ADCs, memory, PLL, a controller, serializers and the output SLVS drivers.

VI REFERENCES

[1] A Krymski US Patent 7,876,362
[2] A. Krymski US Patent 7,659,925
[3] A.Krymski, "A High Speed 1 MPix Sensor with Floating Storage Gate Pixel", 2015 IISW, Vaals, The Netherlands.
[4] A.Krymski. US Patent 10,057,523
[5] A. Krymski. US Patent 8,698,061
[6] A. Krymski "A High Speed 4 Megapixel Digital CMOS Sensor" 2007 IISW, Ogunquit, pp.78-81.
[7] A. Krymski US Patent 7,336,214

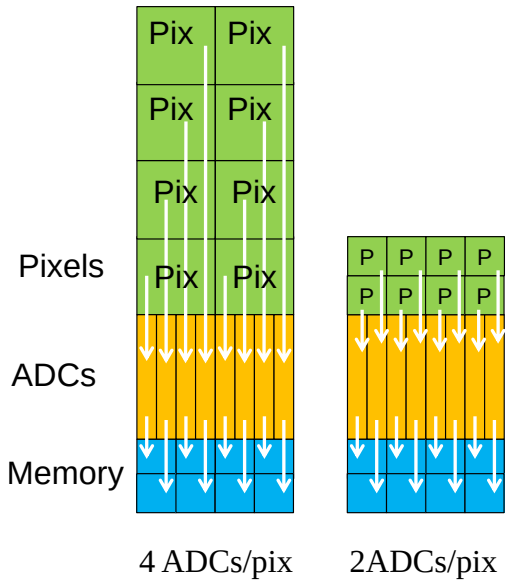

Fig.2. By shrinking the pixel 2 times, the same multi-ADC per column architecture could be re-used to make a new sensor.

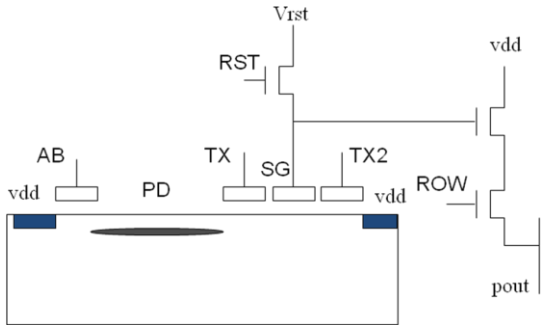

Fig.3. 7T Global shutter pixel with the floating storage gate

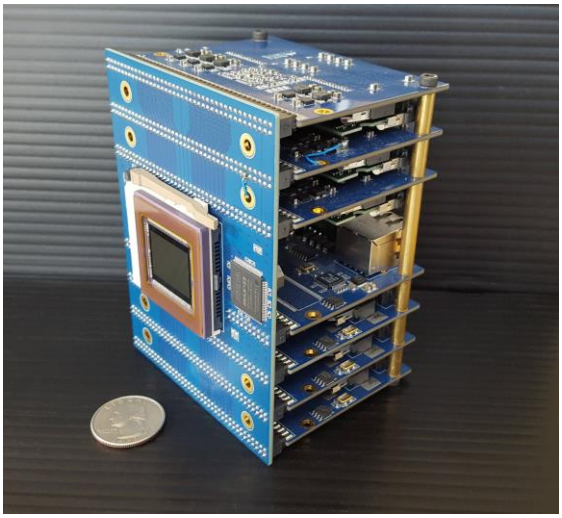

Fig.4. Camera used in the sensor testing. Supports both 1.2MPix and 5MPix sensors

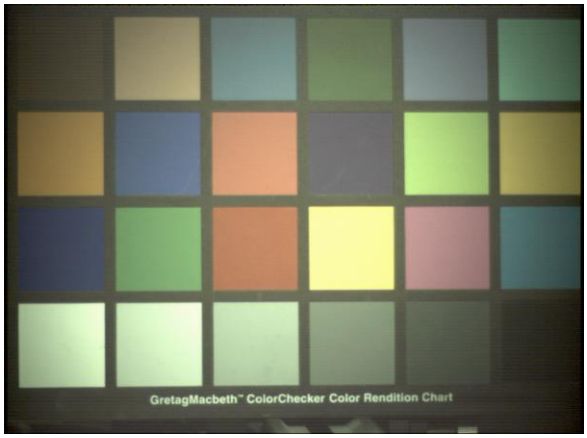

Fig.5. A picture of the Macbeth chart taken by 1.2Mpix sensor at 12,000 kFps.