Multi-spectral High-Speed Backside Illuminated TDI CCD-in-CMOS Imager

Pierre Boulenc[1], Steven Thijs[1], David San Segundo Bello[1, 2], Jonas Bentell[1], Vasyl Motsnyi[1], Linkun Wu[1], Marco Müller[3], Pilar Gonzalez[1], Klaas Tack[1], Celso Cavaco[1], Maarten Rosmeulen[1], Stefano Guerrieri[1] and Piet De Moor[1]

[1] imec, Kapeldreef 75, B-3001 Leuven, Belgium
[2] now at Pyxalis, 170 Rue de Chatagnon, 38430 Moirans, France
[3] ETH Zurich, Rämistrasse 101, 8092 Zürich, Switzerland

Tel : +32 16 28 15 44, E-mail : pierre.boulenc@imec.be

Introduction

Monolithic CCD-in-CMOS integration has become the chosen approach to combine noiseless charge transfer of CCD with the efficiency of CMOS high-speed drivers and readout for Time Delay Integration (TDI) [1-5].
This work presents the recent improvements of Imec's Backside Illuminated (BSI) CCD-in-CMOS technology for high-speed multi-spectral line-scan applications.

Technology test vehicles

Imec's CCD-in-CMOS technology is continuously being tuned to reach high pixel performance. Analog-out test vehicles have been designed and manufactured to carry out such investigations and improvements. Several variations of pixels and readout stages have been characterized and compared to select the best combination of design and process conditions, depending on target applications. Two major pixel families have been developed and tested.
Firstly, 5 µm pitch pixels devices have been designed to aim for high line rate TDI imaging [2]. Conversion Gain has been doubled to fully match signal and external Analog-to-Digital Converters (ADC) ranges. This results in a lower noise-floor in electrons compared to [2] as shown in Figure 1.

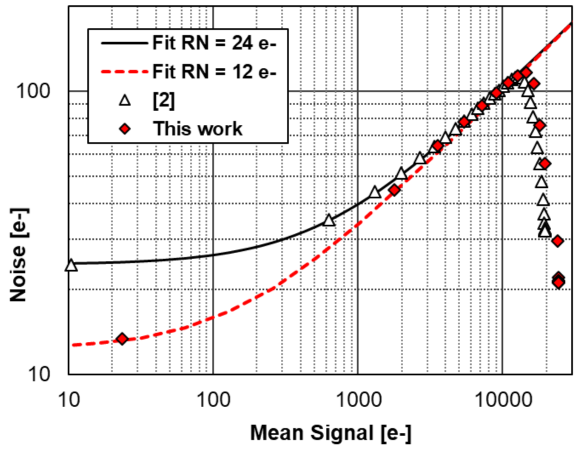

Figure 1: Photon Transfer Curves for new vs. previous generation [2] of 5 µm pitch pixels; readout at 20 kHz.

Row drivers for the CCD gates have been updated to ensure a wider range of operating voltages with a finer control of slew rate for both pixel gates and output stage gates. As can be observed in Figure 2, Charge Transfer Inefficiency has been drastically improved vs. [2] at higher line rates, allowing the almost perfect charge transport up till 1 MHz.

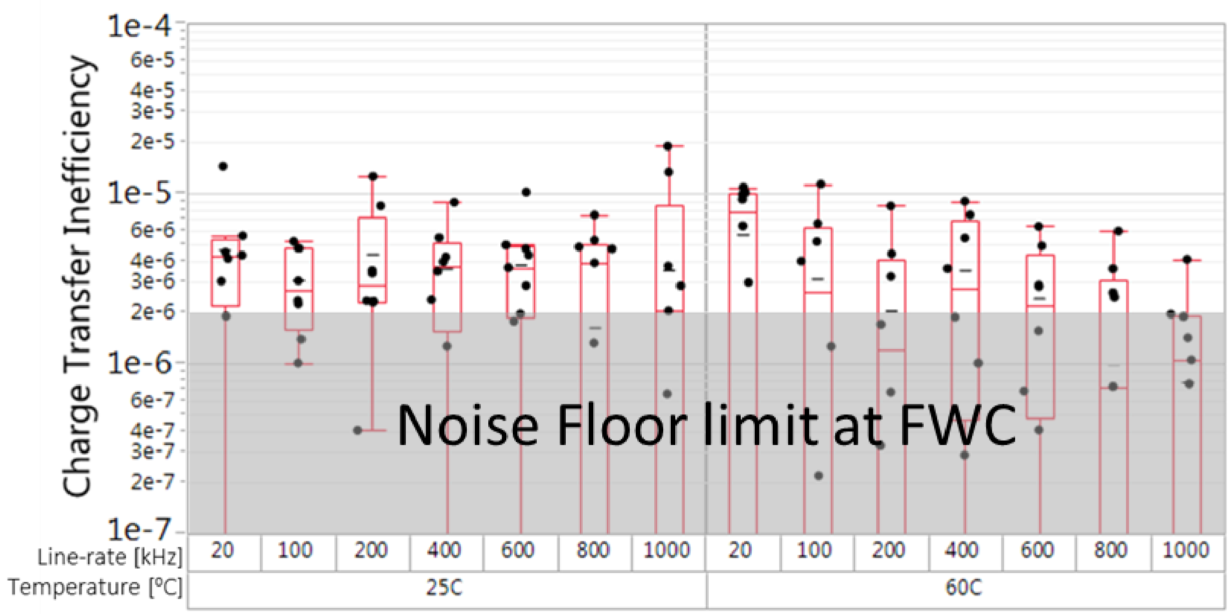

Figure 2: Charge Transfer Inefficiency at various line rates and temperatures for signal levels up till linear Full-Well-Capacity measured on CCD in CMOS test vehicle with 5 µm pitch pixels.

Secondly, a 15 µm pitch pixels sensor has been derived from the architecture described in [2], using the same updated blocks as the 5 µm pitch pixels device mentioned previously. Since pixels are much larger, such a device is expected to be operated at a lower line rate. As extracted from Figure 3, blooming (resp. saturation) Full-Well-Capacity (FWC) of 150.000 (resp. 200.000) electrons is reported at room temperature. Together with a dark current of 800 pA/cm^2, this makes this device an interesting alternative to classical TDI CCDs for space applications. However, with a 99.97 % measured Charge Transfer Efficiency at 8 kHz, this device still requires design improvements.

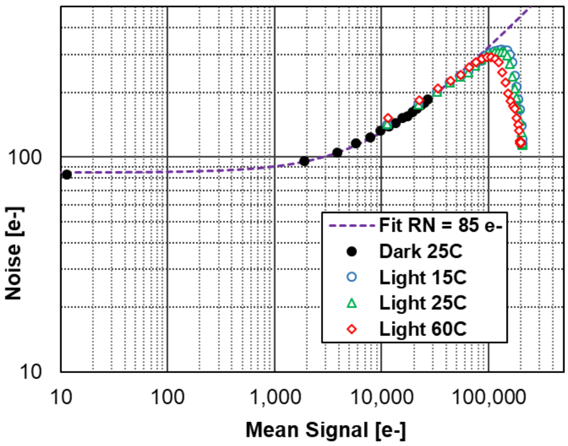

Figure 3: Photon Transfer Curves for 15 µm pitch pixels device; readout performed at 8 kHz line rate.

TDI System-on-Chip

As previously reported [3], Imec has also developed a Digital-Out CCD-in-CMOS TDI imager. This device features 7 bands, with individual stage selection among the available 256 CCD rows (Figure 6). Bi-directional readout is possible thanks to top and bottom dedicated charge to voltage conversion stages.

As observed in Figure 4, blooming (resp. saturation) Full-Well-Capacity is found to be of 20.000 (resp. 23.000) electrons with a noise floor of 15 electrons at room temperature (with uncontrolled package temperature).

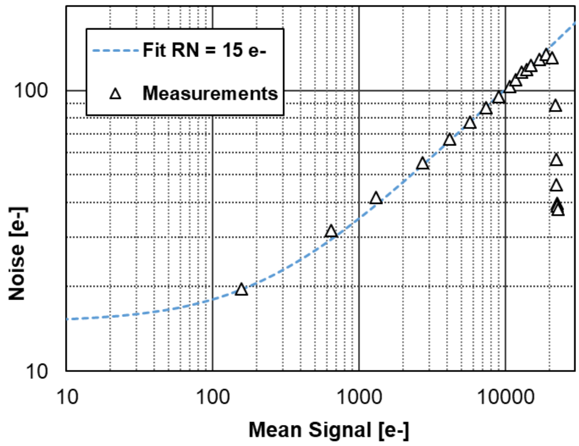

Figure 4: Dark Signal Transfer Curve measured at 115 kHz line rate on a single CCD band.

Backside processing and Anti-Reflective Coating (ARC) have been optimized to enhance Quantum Efficiency (QE) for either the Red-Green-Blue (RGB) spectrum with 96 % peak QE at 510 nm wavelength, either the ultra-violet spectrum with 93 % peak QE at 310 nm wavelength on a 5.8 µm thick substrate, as shown in Figure 5.

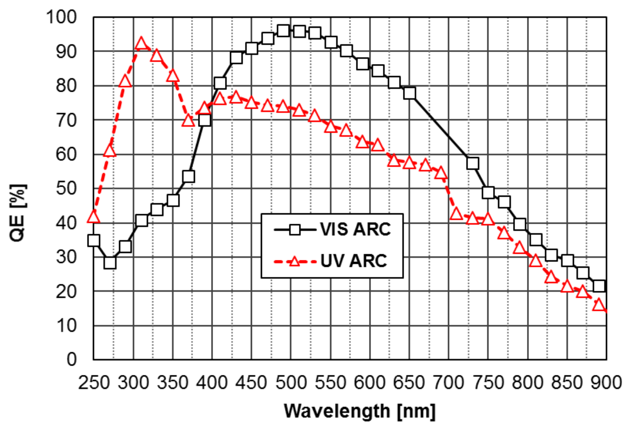

Figure 5: Quantum Efficiency vs. wavelength for BSI samples with 5.8 µm thick substrate and different Anti-Reflective Coatings (ARC).

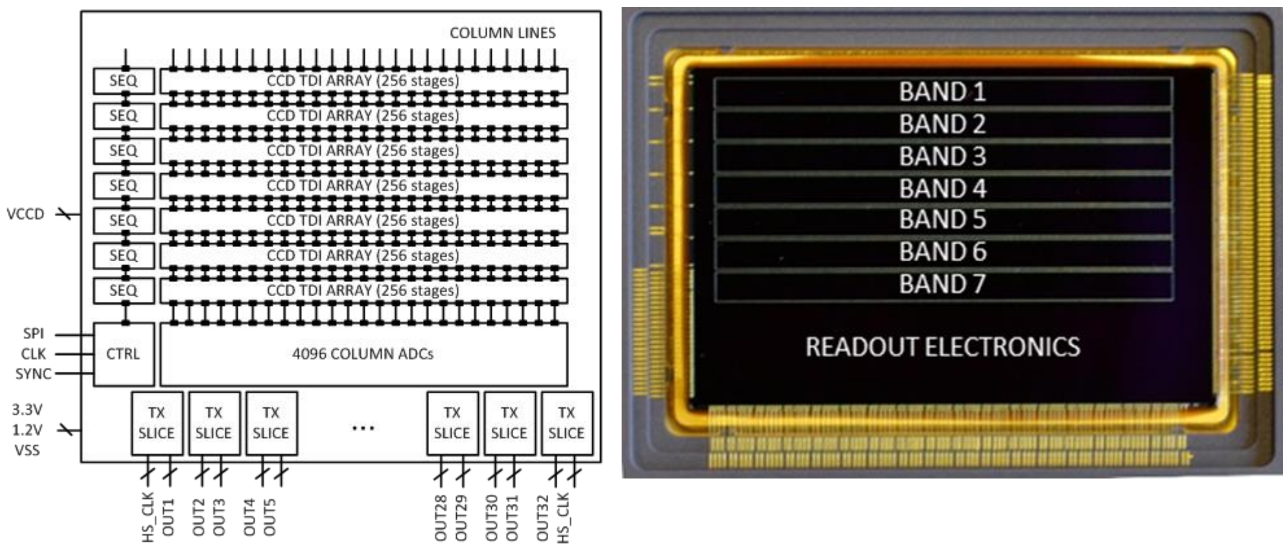

Figure 6: 7-band CCD-in-CMOS TDI schematic diagram (left) and a Back-Side-Illuminated sample (right).

Multi-spectral TDI imager

Process and design optimizations from test vehicles have been successfully ported to the 7-band CCD-in-CMOS TDI full System-on-Chip imager [3] allowing to realize sharp TDI imaging at the highest reported 4K line rate of 275 kHz (Figure 7 top). In order to demonstrate the multi-spectral principle, Red, Green and Blue glass filters have been attached on top of the imager lid and sharp 4K 58 kHz RGB color frames have been obtained (Figure 7 bottom) by selecting 3 simultaneously operated CCD bands.

Figure 7: Close-up of frames taken with 1 band at 275 kHz line rate (top) and with 3 bands + RGB glass filters at 58 kHz line rate (bottom).

In order to realize multi-spectral TDI, one can consider various approaches like wafer-level hyperspectral filters deposition [6]. However, the spectral width of these filters is very narrow and would require many CCD bands, slowing down the whole imager line rate.

A recent development gears this multi-band imager towards more multi-spectral capabilities by directly integrating the glass color filters onto the imager backside surface. Glass filters with 7 different optical bands, each covering approximately 100 nm spectral width, have been glued together with black epoxy to shield the chip area outside the CCD bands and integrated with controlled alignment on a demo sensor (Figure 8).

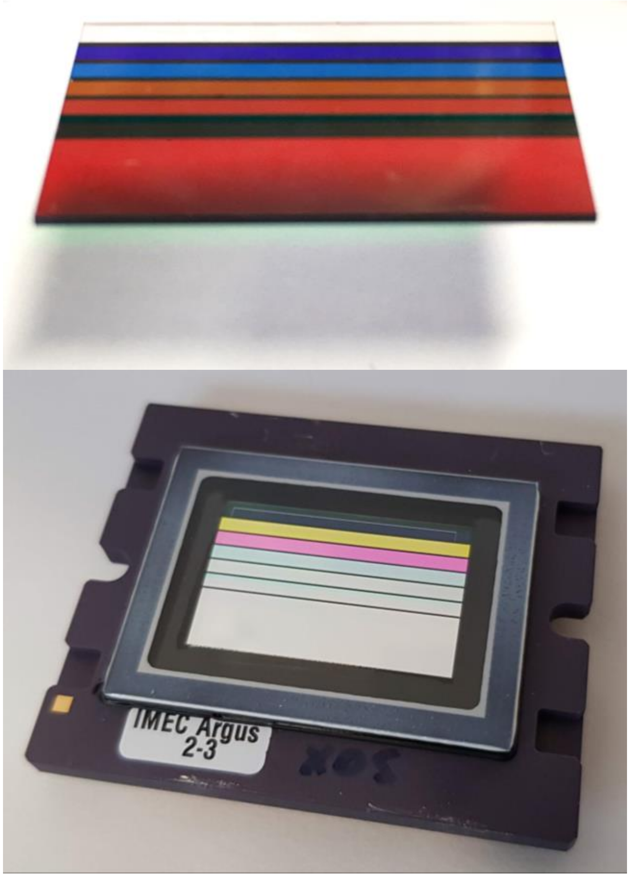

Figure 8: 7-band assembled glass filters before (top) and after (bottom) direct integration onto the multi-band CCD-in-CMOS TDI imager.

A first 7-band TDI frame taken at 31 kHz line rate is presented (Figure 9), exemplifying the multi-spectral capability of the CCD-in-CMOS imager.

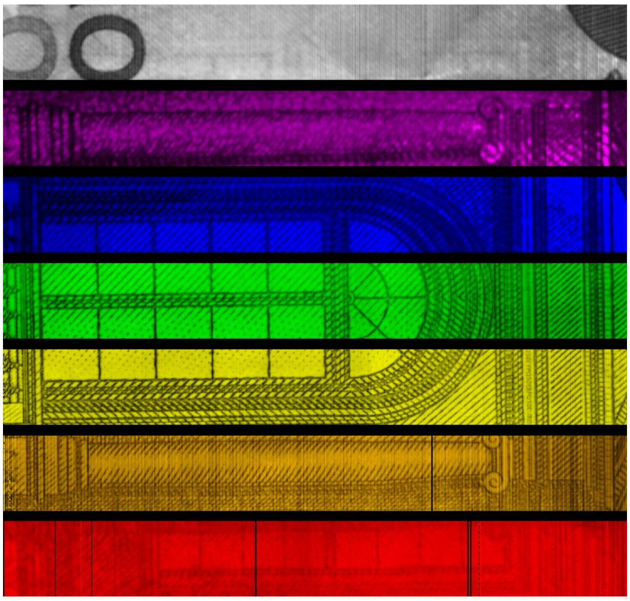

Figure 9: Close-up of a frame taken with the 7 filters assembly and 7 CCD bands at 31 kHz line rate.

Conclusions

These results strengthen the state of the art low-light and high-speed capabilities of Imec's CCD-in-CMOS technology (Table 1). Imec's TDI imager combines on the same chip highly complex CMOS circuits, fast and efficient charge transfer CCD pixels and directly integrated 7-band glass color filters. Such device is the fastest multi-spectral charge-domain CMOS TDI imager ever reported that allows simultaneous 7 color line-scan imaging.

Acknowledgements

This project has received funding from the Electronic Component Systems for European Leadership Joint Undertaking under grant agreement No 662222. This Joint Undertaking receives support from the European Union's Horizon 2020 research and innovation program and Belgium, Netherlands, Greece, France.

The filter integration is part of the ESA AO/1 9315/18/NL/AR contract MICROM-HIDE: Technologies For Microsatellites Multispectral High Definition Imager.

	This work	[2, 3]	[4]	[5]
Technology	130 nm	130 nm	180 nm	150 nm
Number of columns	4096	4096	4096	8192 / 4096
Number of rows	256	256	256	192 / 96
Pixel size	5.4 µm	5.4 µm	5 µm	3.5 µm / 7 µm
Full well	**23 ke-**	30 ke-	30 ke-	30 ke- / 185 ke-
Poly CCD gap	110 nm	110 nm	250 nm	NA
Conversion gain	**40 µV/e-**	28 µV/e-	NA	NA
Noise floor at RT	**15 e-**	20 e-	12 e-	20 e- / 105 e-
Dark Current at RT	**2.5 nA/cm²**	3.5 nA/cm²	3.7 nA/cm²	11.0 nA/cm²
Full-Frame line rate	**275 kHz**	43 kHz	270 kHz	58 kHz / 29 kHz
Max line rate	**1000 kHz**	800 kHz	NA	NA
CTI **line rate**	**$< 10^{-5}$** **from 20 to 1000 kHz**	$< 5.10^{-5}$ from 2 to 800 kHz	$< 10^{-5}$ 270 kHz	5.10^{-4} / 9.10^{-4} 58 / 29 kHz
Peak QE **wavelength**	**96 % (VIS) / 93 % (UV)** **510 / 310 nm**	89 s% 530 nm	49 % 630 nm	42 % 630 nm
MTF at Nyquist **wavelength**	0.44 525 nm	0.44 525 nm	NA	NA
Supply voltage Max	3.3 V	3.3 V	NA	NA
Integrated drivers	YES	YES	YES	NO
Stage Selection	individual	individual	per 64	individual
TDI bands	7	7	1	5

Table 1: Comparison with published state of the art CCD-in-CMOS technologies.

References

[1] P. De Moor et al., "Enhanced time delay integration imaging using embedded CCD in CMOS technology", IEEE International Electron Devices Meeting, pp. 4.6.1-4.6.4, December 2014.

[2] P. Boulenc et al., "High Speed Backside Illuminated TDI CCD-in-CMOS Sensor", International Image Sensor Workshop, 2017.

[3] D. San Segundo Bello et al., "A 7-band CCD-in-CMOS Multispectral TDI Imager", International Image Sensor Workshop, 2017.

[4] H. J. Lee et al., "Charge-Coupled CMOS TDI Imager", International Image Sensor Workshop, 2017.

[5] C. Ma et al, "Design and Characterization of a 3.5um pitch, 8192 resolution, 5 Spectrum CMOS TDI image sensor", International Image Sensor Workshop, 2017.

[6] N. Tack et al. "A compact, high-speed, and low-cost hyperspectral imager", Proc. SPIE 8266, Silicon Photonics VII 8266(0), 8266Q, 2012.