Partially Pinned Photodiode Performances for Emerging Space and Nuclear Applications

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INTRODUCTION

JUPITER'S moon exploration missions as well as nuclear and high energy physics applications require CMOS Image Sensors (CIS) with good performances in terms of dark current and with a high fill factor in order to mitigate the dark current increase after Total Ionizing Dose (TID) exposure. In this contest, the use of photodiodes that can provide high performance on a wide range of TID is mandatory.

On the other hand, when exposed to TID, CISs suffer from severe degradations due to the generation of different defect species (i.e. positive trapped charges and interface states) in the oxides that are present in the pixel structure. Several studies in the past decades have dealt with TID effects in CISs mainly focusing on 3T conventional photodiodes (PD) and 4T pinned photodiodes (PPD) [1], [2]. It has been shown that in 3T-PD the Si/SiO_2 interfaces are in contact with the depleted zone thus leading to a dark current increase due to the TID induced defects in these regions. For PPD, the depleted region is no more in contact with the oxides, and then the dark current after TID is less important than in 3T PD. However, this pixel suffers from severe degradation mostly linked to the charge transfer degradation from the PPD to the floating diffusion. This makes the PPD not suitable for radiation environments where the TID is higher than 10-100 krad. Nevertheless it has been demonstrated in [3] that 3T PD can be radiation hardened by using radiation hardened by design (RHBD) techniques. This shows that the radiation hardness of CIS is a tricky issue and that the existing technologies have to be mixed to obtain good response overall investigated dose range.

The partially PPD (p-PPD) consists of a 3T photodiode with a pinned region and an un-pinned one (e.g. N+ doped region which serves to reset the photodiode) [4], [5]. Since an appreciable portion of the photo-sensitive region has a pinned surface potential, this pixel retains some advantages of the PPD, e.g. low dark current and tunable conversion gain. In addition, P+ doping protects the p-PPD thus making it a good candidate for the use in radiation environments. Despite this, there is no clear radiation hardness evaluation of this photodiode technology in the literature.

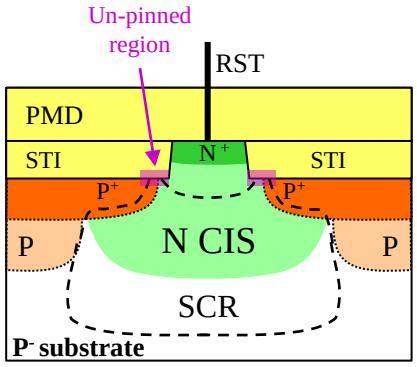


Fig. 1 Cross section views of 3T Partially Pinned Photodiode pixel. SCR = Space Charge Region. RST = Reset MOSFET.

In this study, the p-PPD is evaluated at TID up to 1Mrad(SiO_2). The response of three different pixels design is investigated in order to estimate the radiation hardness and possible ways of RHBD mitigation techniques.

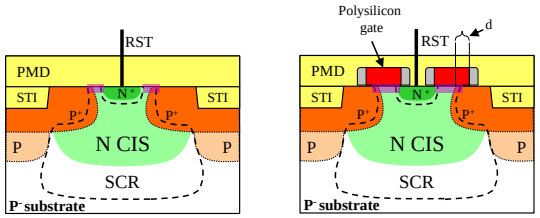
I. THE PARTIALLY PINNED PHOTODIODE

Fig. 1 reports the cross sectional view of the 3T-standard p-PPD [6] [4], never investigated under irradiation to the best of our knowledge.

It is composed of a photo sensitive region, the N-doped photodiode, and three transistors to reset the signal (RST), amplify it (source follower transistor, SF) and to select the row (row select transistor, RS) to the column readout chain [7]. In this particular photodiode, the top of the N doped region is covered with a P^+ implant to prevent the contact between the depletion region and the oxides. As shown in Fig. 1, the photodiode depth is reduced in order to fully deplete the photodiode during the operation [4]. In order to connect the photodiode to

RST MOSFET, the P+ pinning layer has to be opened somewhere to let the N region reach the surface. Therefore, in partially pinned photodiodes the depletion region is in contact with oxide interfaces, in the vicinity of the RST contacts. Since the total area of the depleted oxide interface is smaller than in a standard 3T-pixel the dark current is lower in these photodiodes than in a standard 3T pixel.

To carry out this study, two variants of the standard p-PPD have been evaluated. In the first, displayed in In Fig. 2 (a), the STI have been recessed away from N-doped region. In Fig. 2 (b) a gate surrounded p-PPD is represented; for this design, the radiation hardness technique used for conventional photodiode is employed in order to study if possible improvements against radiation are possible for partially pinned photodiode.



(a) Partially Pinned Photodiode with recessed STI

(b) Partially Pinned Photodiode with polysilicon gate

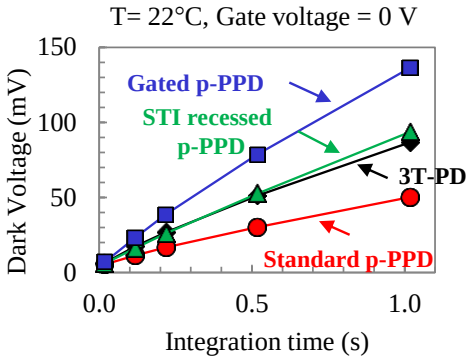
Fig. 2 Cross sectional views of (a) the STI have been recessed away from the N-doped region. In (b) the radiation hardness technique used for conventional photodiode is applied to the p-PPD to improve its radiation hardness. SCR = Space Charge Region. RST = Reset MOSFET. PMD = Pre Metal Dielectric. STI = Shallow Trench Isolation.

II. EXPERIMENTAL DETAILS

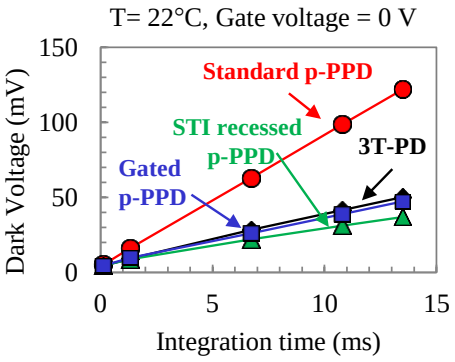
Investigated CIS was manufactured using 180 nm CIS process with dedicated and optimized in-pixel devices. The integrated image sensors are composed of a pixel array (128×256 pixels) with three transistors per pixel. The analog readout circuits are designed using 1.8 V MOSFETs. All the transistors of the readout chain have been radiation hardened by ISAE-SUPAERO using Enclosed Layout Transistors (ELT) [8] to mitigate the Radiation Induced Narrow Channel Effects (RINCE) and sidewall leakage [9].

Pixel arrays have been divided into different regions to investigate the radiation hardness of the four-pixel designs and RHBD solutions. For the study presented in this work only four regions (of about 32x64 pixels) are investigated in order to study the radiation hardness the various p-PPDs design and to compare it with 3T conventional PD.

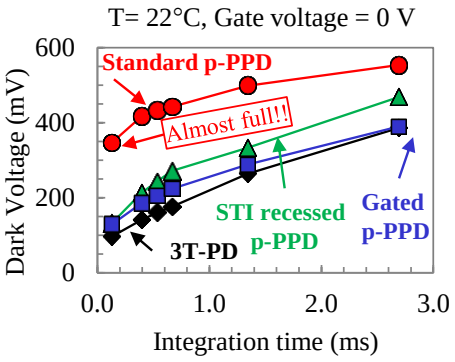
Room temperature 10 keV X-ray irradiations were performed at the CEA, DAM, DIF with Aracor facility (Arpajon, France). The circuits were exposed up to TID levels of 1krad, 50krad and 1 Mrad(SiO_2). The devices have been characterized within the month after the end of the X-rays irradiation.



(a) Non-irradiated



(b) 50 krad(SiO_2)

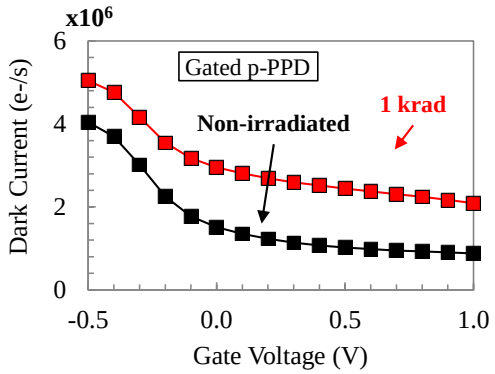


(c) 1Mrad(SiO_2)

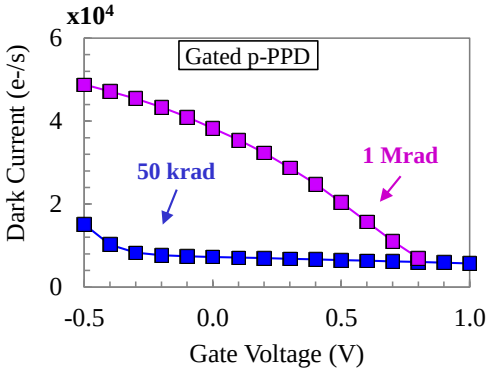
Fig. 3 Dark voltage as a function of the integration time for (a) non-irradiated photodiodes and after exposure to TID of 50 krad (b) and 1 Mrad (c).

III. P-PPD DARK CURRENT INCREASE

The evolution of the dark signal as a function of the integration time is reported in Fig. 3 for p-PPDs and standard 3T PD. Before irradiation the standard p-PPD has a lower dark current with respect to the 3T PD current values comparable to or even higher than the 3T one. After TID exposure, the standard p-PPD dark current increases much more than the other diodes because of the radiation-induced positive trapped charge in the STI that leads to the depletion of the P+ pinning layer.



(a) Dark Current vs. Gate Voltage (0 rad and 1 krad)



(b) Dark Current vs. Gate Voltage (50 krad and 1 Mrad)

Fig. 4 The influence of the gate voltage applied on the polysilicon gate is reported thanks to dark current evolution as a function of the gate voltage for (a) non-irradiated and 1 krad irradiated gated partially pinned photodiode and (b) 50 krad and 1 Mrad irradiated gated partially pinned.

On the contrary, STI recessed and gated partially pinned photodiodes exhibit reasonable dark current levels comparable to the 3T conventional photodiode at 50 krad thus meaning that the doping concentration of the P+ layer at the PMD interface is high enough to prevent the PMD depletion.

At 1 Mrad the performances of the partially pinned photodiodes reach the level of the conventional 3T one. It is worth noting that at 10 Mrad both 3T standard PD and p-PPDs are not functional anymore as already reported in [10].

Fig. 4 reports the evolution of the dark current as a function of the gate voltage for the gated p-PPD. It is possible to note that for doses below 1 Mrad (see Fig. 4 (a) and Fig. 4 (b)) the influence of the gate voltage starts to be evident for negative values being the dark current increase higher than for positive gate voltages. At 1 Mrad, on the other hand, the dark current decrease with the increasing of the gate voltages. In any case, it is possible to conclude that the lowest dark current is obtained for positive gate voltages.

In order to explain the increase of the dark current at gate voltages < 0V, Fig. 5 shows an illustration of the degradation mechanism.

It is possible to see that when the gate is negative biased a gate induced drain leakage (GIDL) is responsible for the augmentation of the dark current. Moreover, since the depleted region is in contact with the spacer, the dark current level increase with the increasing of the TID due to the radiation induced defects in the gate oxide and in the spacer.

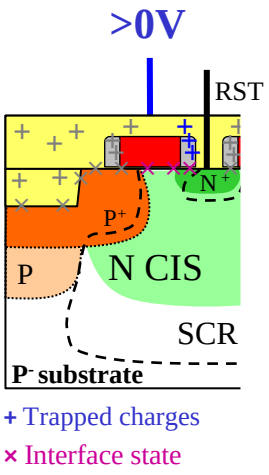


Fig. 5 Illustration of the dark current increase mechanism for gated p-PPD at negative gate voltages.

IV. TID INDUCED DEGRADATIONS

Dark current evolution with the TID, reported in Fig. 6, shows that the gated p-PPD gives the best performances thanks to the fact that the gate voltage can be adjusted to ensure that the depleted region is in contact, even at high TID, only with the gate oxide, which is a much high purity oxide compared with STI and PMD.

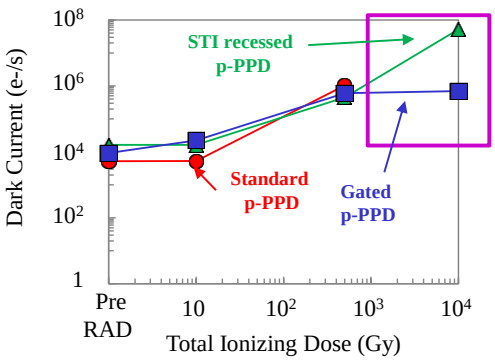
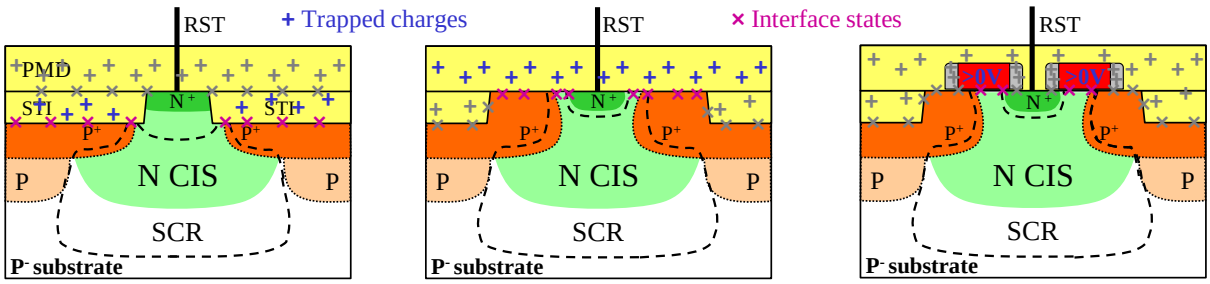


Fig. 6 Dark current evolution as a function of the TID. Dark current values are calculated at the optimum gate voltage (e.g. 0 V for standard and STI recessed partially pinned photodiode and 0.8 V for gated partially pinned one).



(a) Standard Partially Pinned Photodiode

(b) Partially Pinned Photodiode with recessed STI

(c) Partially Pinned Photodiode with polysilicon gate

Fig. 7 Pixel degradation mechanism illustration in (a) a standard, (b) STI recessed and (c) gated p-PPD at TID>1krad(SiO_2).

To clarify the TID induced degradations in the different pixels Fig. 7 reports the illustration of the induced defects. In the standard p-PPD displayed in Fig. 7 (a), the dark current increase is due to the positive trapped charges and interface states induced in STI by the radiation. In the other two variants these defects do not contribute to dark current increase (see Fig. 7 (b) and Fig. 7 (c)). However, the depleted region in the STI recessed photodiode is in contact with the PMD near the N+ node, as can be seen in Fig. 7 (b), thus enhancing the dark current at 50 krad. At 1 Mrad the interface states in the PMD contribute to the reduction of the P+ layer even at the PMD interface.

Consequently, the Si/SiO_2 depleted interface becomes wider thus leading to a further dark current increase. In the case of the gated p-PPD (Fig. 7 (c)), for positive gate voltage the depleted region is in contact with the gate oxide with a lower interface state density than the PMD. Then, the dark current augmentation is lower in this photodiode with respect to the non-gated one (if the right gate biasing condition is used).

V. Conclusions

The main conclusion of this study is that, contrary to what is generally thought, the standard p-PPD is less radiation tolerant than the conventional 3T-photodiode (unhardened) because of the complete removal of the P+ pinning layer at low dose.

However, the results show also that protecting the N+ contact by a polysilicon gate allows keeping good performances at 1Mrad making this photodiode an interesting candidate for the targeted TID range.

VI. References

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