R50

Back Side Illuminated High Dynamic Range 4.0µm Voltage Domain Global Shutter Pixel with Multiple Gain Readout

K. Mori, T. Otaka, T. Isozaki, N. Yasuda, T. Akutsu, K. Miyauchi, A. Tsai†, Y. Sawai, S. Tanaka
I. Takayanagi and J. Nakamura

Brillnics Japan Inc., 6-21-12 Minami-Oi, Shinagawa-ku, Tokyo, 140-0013 Japan
†Brillnics Inc., Guangming 6th Rd., Zhubei City, Hsinchu County 302, Taiwan

Contact: Kazuya Mori: tel: +81-3-6404-8801, fax: +81-3-5767-5568, email: mori.kazuya@brillnics.com

Introduction

Backside illuminated image sensors with a 4.0µm global shutter (GS) pixel have been fabricated in a 45nm/65nm stacked CMOS process as a proof-of-concept vehicle. The pixel components for photon-to-voltage conversion are formed on the top substrate (the 1st layer). Each photo converted signal from the 1st layer pixel is stored in sample-and-hold (S/H) capacitors on the bottom substrate (the 2nd layer) via micro hybrid-bump (HB) interconnection to achieve a voltage domain GS function. The 2 sets of voltage domain storage capacitor per pixel enable a multiple gain readout to realize single exposure high dynamic range (SEHDR) [1] in the GS operation.

Pixel structure and operation timing

Fig. 1 shows a schematic view of the stacked pixel structure. The storage memory region is formed on the fully light-shielded bottom stacked layer. Thus, the photodiode can be extended as large as possible on the top layer. This configuration offers extremely small parasitic light sensitivity (PLS), high saturation signal and high optical performance compared to the charge domain GS pixels where in-pixel memory is located inside a pixel.

Fig. 2 shows a schematic diagram of the prototype sensor and an off-chip signal processing block. The stacked pixel configuration with two sets of different conversion gain signal storage realizes the GS operation with the single and multiple exposure HDR function [1,2,3]. Also, additional switches enable the rolling shutter (RS) operation. The analog-to-digital conversion is carried out via off chip AFE with CDS.

The shutter pointer and readout timings for RS (a) and GS in the single (b) and multiple exposure HDR (MEHDR) function (c) are shown in Fig. 3. Fig. 4 shows a timing sequence of shutter release (Global Shutter), the global HDR readout (Read1) and data readout from the pixel S/H capacitors (Read2) in the single exposure.

Characterization

A photo-electron conversion plot in the single and multiple exposure is shown in Fig. 6. Full well capacity of 40ke$^-$ is obtained with a high charge density photodiode [2]. Angular response of a green pixel in the Bayer configuration and QE (quantum efficiency) plot are shown in Fig. 5(a) and 5(b), respectively. Angular responses for both horizontal and vertical directions exhibit no significant difference.

Pixel performance improvements

DR enhancement is attempted with a multiple exposure scheme [6,9]. In the GS readout sequence in Fig. 3 (b), low and high conversion readouts are carried out for short and long exposure readout, respectively, to perform HDR operation where longer exposure with high gain covers low light portions while shorter exposure with low gain covers high light portions of the scene. As shown in Fig. 6, maximum linear light response range is boosted 160 times with a 1:20 exposure ratio than that of the HCG single exposure case, which results in DR of 102dB.

Noise floor of 4e$^-$ has been obtained with a very higher CG (>190µV/e$^-$) in pixel option. Further noise reduction is feasible by in-pixel CDS gain and enlarged S/H capacitor [4]. Sample images of a rotating body are shown in Fig. 7 that demonstrate no image distortion in the GS mode, while distortion is seen in the RS mode. Fig.8. demonstrates 100dB MEHDR in the GS operation with an object having 100dB brightness ratio.

Conclusion

A back side illuminated high dynamic range 4.0μm global shutter pixel has been developed. Table 1 summarizes the pixel performance characteristics. Table 2 compares global shutter pixel performance in single exposure systems. In the proposed pixel architecture, the 40ke⁻ FWC, -140dB PLS, over 70% peak green QE and 90% angular response at ±20° have been obtained, which significantly exceeds performance of charge domain GS pixels[5-8]. Smaller noise floor and higher FWC than those of the conventional voltage domain pixels [3,4,9] have been obtained. Two sets of in-pixel multiple memory enable further DR extension up to 100dB with a multiple readout operation, while single exposure HDR operation achieves 78 dB DR. Obtained key sensor performance can be improved further, especially in SNR and DR, and pixel size can be shrunk by minor design modifications.

ACKNOWLEGMENT

The authors gratefully acknowledge the support by Yutaka Sato in acquiring sample images.

Reference

1) I. Takayanagi, et al., *"An over 90 dB intra-scene single-exposure dynamic range CMOS image sensor using a 3.0 μm triple-gain pixel fabricated in a standard BSI process,"* Sensors, 18, 203, 2018

2) K.Mori, et al., "*Back side illuminated high dynamic range 3.0μm pixel featuring vertical p-n junction capacitance in a deep pinned photodiode*", in Proc, 2017 International Image Sensor Workshop, Hiroshima, Japan May30-June2, 2017

3) G. Meynants, "*Backside illuminated CMOS active pixel sensor with global shutter and 84 dB dynamic range*", Scientific Detector Workshop – Firenze – 8 October 2013

4) T. Kondo, et al, "*A 3D stacked 16Mpixel global-shutter CMOS image sensor using 4 million interconnections*", ITE Trans. on MTA Vol. 4, No. 2, pp. 129-135 (2016)

5) T. Yokoyama, "*High performance 2.5um global shutter pixel with new designed light-pipe structure*", In proc of IEDM 2018 233-236(10.5) Sanfransisico,CA, USA Dec 01-05, 2018

6) M. Kobayashi, "*A 1.8e- rms temporal noise over 110dB dynamic range 3.4μm pixel pitch global shutter CMOS image sensor with dual-gain amplifiers, SS-ADC and multiple-accumulation shutter*", ISSCC2017 4.5 ED, Vol. 63, No. 1,pp.10-15, January 2016

7) A. Tournier, et al, "*A HDR 98dB 3.2μm charge domain global shutter CMOS image sensor*", In proc of IEDM 2018 229-232(10.5) Sanfransisico,CA, USA Dec 01-05, 2018

8) Y. Kumagai, "*Back-illuminated-pixel-pitch global shutter CMOS image sensor with charge-domain memory achieving 10k e- saturation signal*", In proc of IEDM 2018 237-240(10.6) Sanfransisico,CA, USA Dec 01-05, 2018

9) L. Stark, "*Back-illuminated voltage-domain global shutter CMOS image sensor with 3.75μm pixels and dual in-pixel storage nodes*", In proc of 2016 Symposium on VLSI Technology Digest of Technical Papers June 14-17, 2016

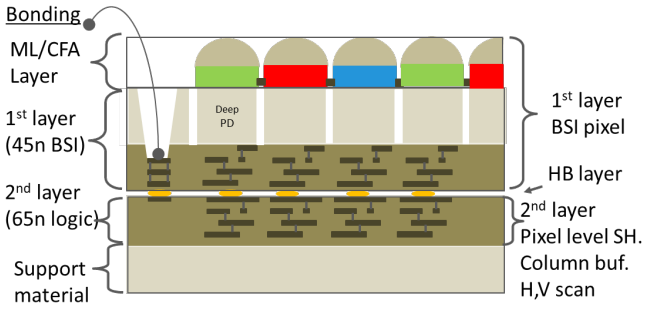

Fig. 1 Schematic view of the stacked pixel structure

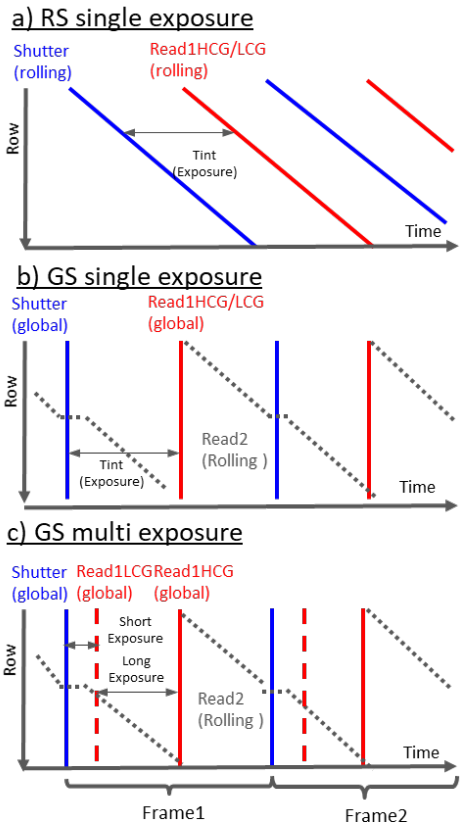

Fig.3 Shutter pointer and readout operation timing in various HDR modes

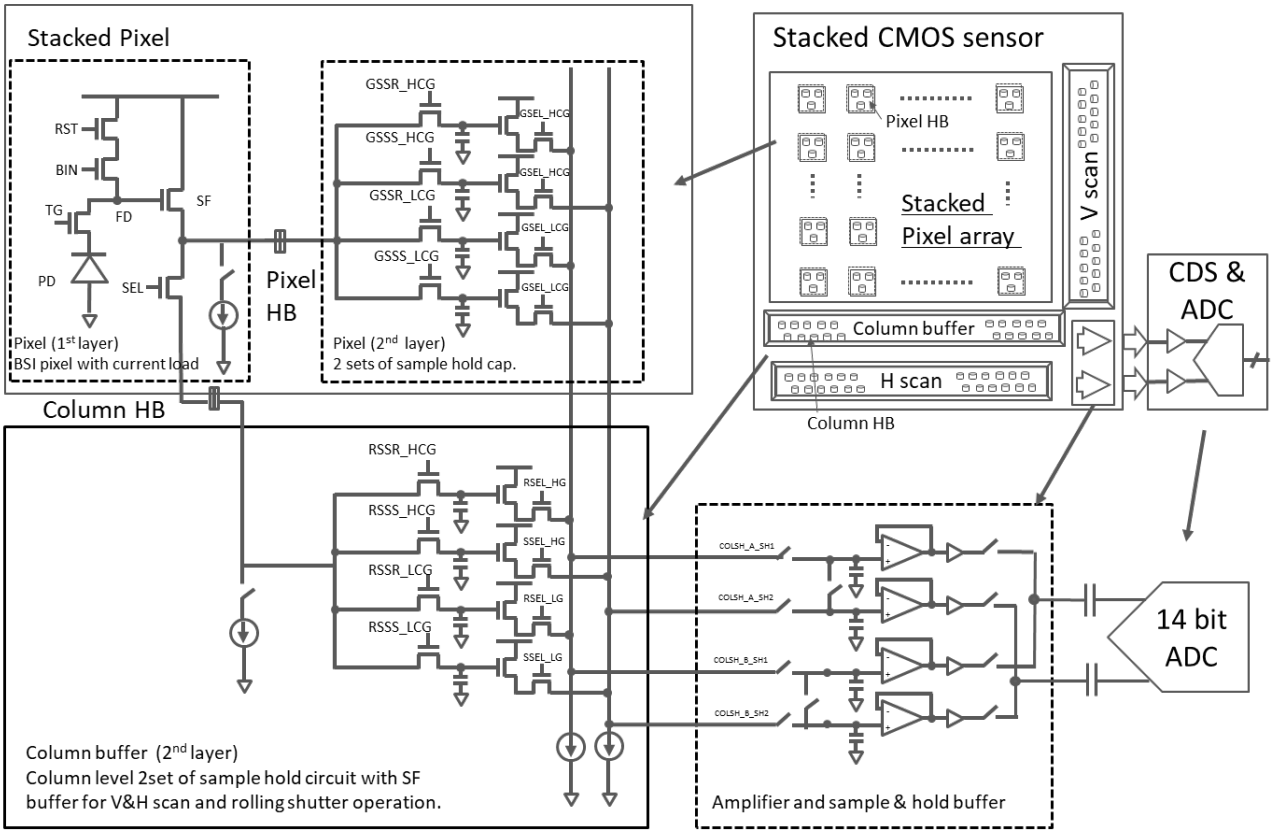

Fig.2 Block diagram and pixel circuit schematic in pixel, column and amp & ADC block

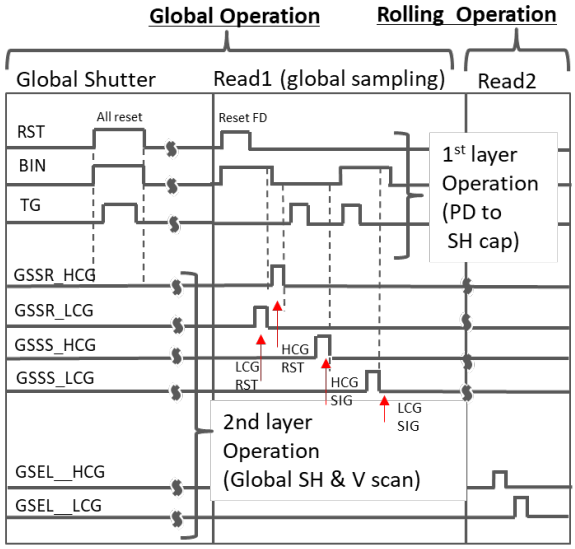

Fig.4 A timing sequence to realize multiple pixel gain readout
Global : Shutter, charge integration, global sampling(Read1)
Rolling : readout from SH cap(Read2), V & H scan

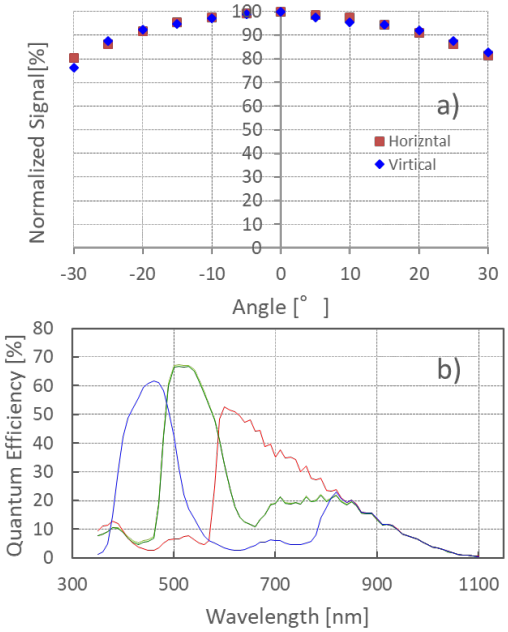

Fig.5 Angular response of green pixels (a:top) in Bayer configuration at 530nm and QE(b:bottom) w/ glass lid.

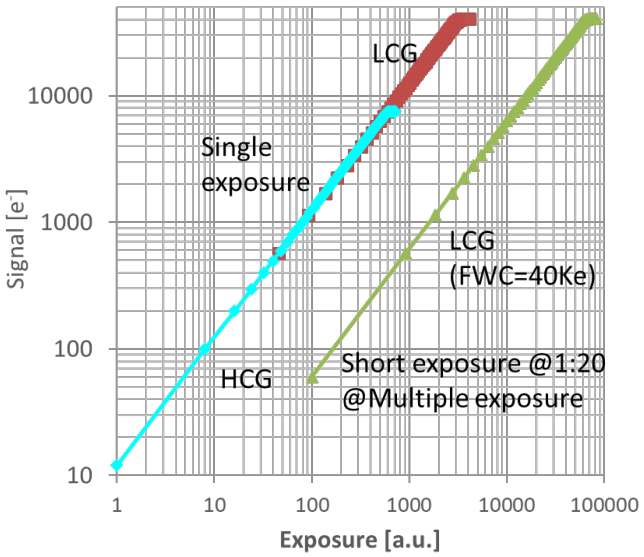

Fig.6 Photo conversion characteristics of multiple gain readout operation in single and multiple exposure.

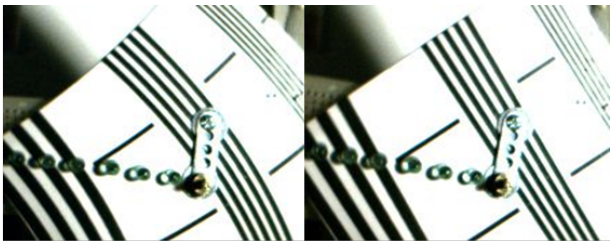

Fig.7 GS and RS images in single exposure (left : RS , right :GS)

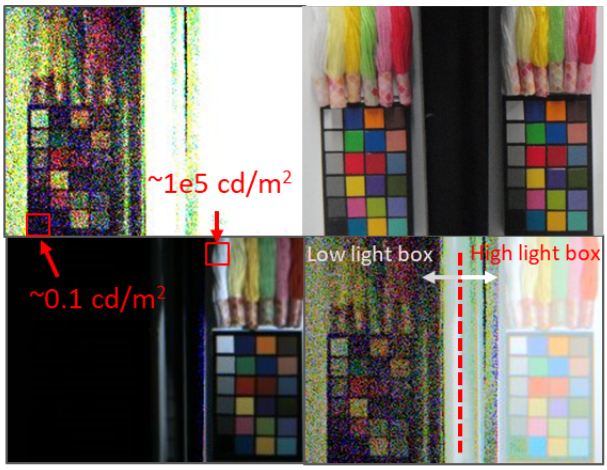

Fig.8 100dB HDR image in multiple exposure of 6 and 0.6msec.
(top,right : An object,
top,left : HCG / long exp,
bottom,left : LCG / short exp,
bottom,right : 8bit HDR image)

Table 1 . 4.0µm stacked pixel characteristic in global shutter operation Tint = 300usec/ RT (rolling operation)

Specification		Specification	Low gain GS (RS)	High gain GS (RS)
Pixel size [µm]	4.0	Dynamic range [dB]	77 (85) [102@1:20 of multi exposure]	
Pixel operation voltage [V]	2.5	Conversion Gain [µV/e-]	21	170
Responsivity [ke-/lx-s] (5100k,CM500)	37	Linear full well [ke-]	35	6
QE (G) max [%]	74	FWC [ke-]	40	7
Angular response [%] @±20° (H & V)	>90	Noise floor [e-]	30(13)	5(2.1)
Parasitic light sensitivity [-dB]	< 140	Dark pixel FPN [e-]	16(3)	4.2(1.2)
PRNU[%] at 50% of FWC	0.5	Image lag [e-]	<1.0	

Table 2 . Comparison of recent global shutter pixel performance in single exposure systems

Specification	This work	IEDM2018 Kumagai et.al. [8]	IEDM2018 A.Tournier et.al. [7]	IEDM2018 T.Yokoyama et.al. [5]	ISSCC2017 M.Kobayashi et.al. [6]	VLSI2016 L.Stark et.al [9]	ITE. 2016 T.Kondo et.al. [4]	IISW2017 K.Mori et.al[2]
Storage memory	Voltage domain	Charge domain	Charge domain	Charge domain	Charge domain	Voltage domain	Voltage domain	Not GS
Pixel size [µm]	**4.0**	2.74	3.2	2.5	3.4	3.75	3.8	3.0
Pixel operation voltage[V]	**2.5**	3.3	2.5	NA	3.3	NA	3.3	2.8
QE (G) max [%]	**74**	NA	72.9	67	NA	NA	NA	77
Angular Resp. [%]@±20°	**>90**	NA	NA	50	40	NA	NA	>90
PLS [-dB]	**<140**	80	NA	81.6	89	80	180	NA
Dynamic range [dB]	**78**	74	68	NA	79	59	60.5	91
Noise floor [e- rms]	**5**	1.85	2	2	1.8	8.5	33	1.1
Full well capacity [ke-] (e-/µm2)	**40 (2500)**	10 (1331)	16.6 (1620)	6.3 @LFWC	16.2 (1400)	8.1 (700)	35 (2423)	45 (5000)