A High Performance 2.5um Charge Domain Global Shutter Pixel

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***Abstract*—**We developed a new 2.5um Global Shutter (GS) pixel using 65nm process with an advanced Light-Pipe (LP) structure. This is the world's smallest charge domain GS pixel reported so far. The pixel shows excellent optical performances even with F#2.8 lens and extremely low dark current. This new developed pixel plat form is key enabler for ultra-high resolution sensors, industrial cameras with wide aperture lenses and low form factors optical modules for mobile applications. We will discuss the key design guidelines for such a small pitch GS pixel.

INTRODUCTION

In recent years, there is a strong market demand for small pitch and high performance GS sensors which can take images without distortion for fast moving objects. This function is highly desirable for machine vision and automotive applications. Moreover it can realize facial recognition for mobile use.

In practical use of GS sensor, it is important to achieve high signal-to-noise ratio. Since GS pixel has additional components - memory node (MN), compared to rolling shutter pixel; suppressing dark current generated in the MN is one of the key factors of GS pixel development. Also suppressing parasitic light sensitivity (PLS) is very important even in oblique incident light, particularly for these applications. For machine vision, large optical format sensors are usually used for high resolution. For mobile use, module height must be low, therefore small F# lenses are necessary.

In order to meet such requirements, we have developed small pitch GS pixel. We already showed a low noise and high QE 2.8um GS pixel with 110nm technology [1, 2]. In this paper we report a 2.5um GS pixel which features extremely low dark current MN and advanced LP structure, using a 65nm process node [3].

DEVICE STRUCTURE

Figure 1 and Figure 2 show the circuit schematic and the cross section schematic of the developed pixel respectively [4]. In order to maximize active area, there is no row select transistor and floating diffusion is shared by two pixels diagonally. We adopted a full pinned Memory Node (MN) to realize low dark current [2]. The MN is covered with tungsten (W) shield to protect from incident light [5]. The ultra-thin backend process reduced the optical height from the Si surface to the micro-lens which contributed to the immunity against oblique light and realized the LP structure using a high refractive index material [6, 7].

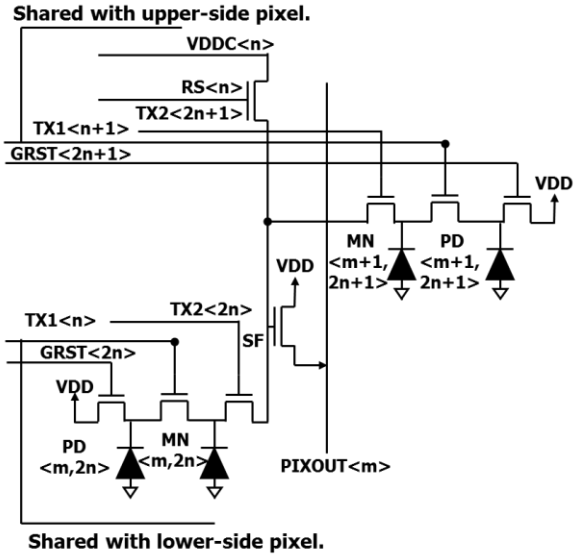


Figure 1: Pixel circuit schematic of GS pixel.

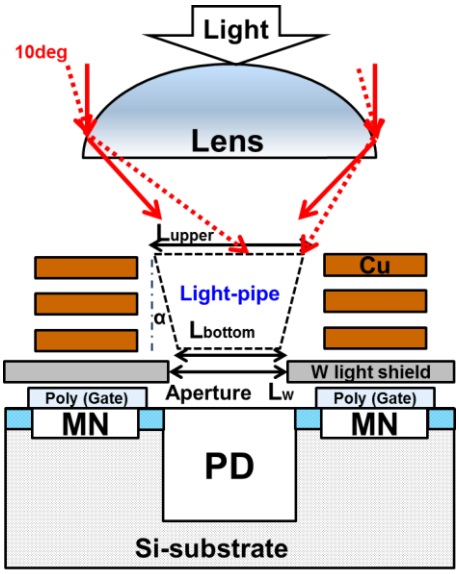


Figure 2: Cross-section schematic of GS pixel

DESIGN CONCEPT FOR CHARGE DOMAIN

The placement of Photo Diode (PD) and MN should be determined taking the tradeoff with each performance into account. Table 1 shows the figure of merit for PD and MN as the GS pixel's charge domain. Light sensitivity of the PD needs to be larger and that of the MN needs to be lower. On the other hand, Full Well Capacity (FWC) of the MN should be larger than that of the PD in order to store the electrons transferred from the PD without loss. Our deliberate study led us to choose a narrower MN and a wider PD, namely maximizing the fill factor which helps to maximize the QE with good angular response. Therefore, the challenges of this work are described as follows: (1) narrow full pinned MN design to achieve large FWC and low dark current with good charge transfer from MN to floating diffusion (FD), (2) LP design to keep sensitivity of MN low even with oblique light.

Table 1: Figure of merit for charge domain.

	Photo Diode (PD)	Memory Node (MN)
Light Sensitivity	Lager-is-better (QE)	Smaller-is-better (PLS)
Angular Response of Sensitivity	Keeping Larger	Keeping Smaller
Full Well Capacity	Lager-is-better	Larger than PD
DC, DSNU	Smaller-is-better	
Lag	Smaller-is-better	

MEMORY NODE DESIGN

In order to suppress the dark current, we adopted the full pinned MN structure [2]. Figure 3 shows the cross section schematics of (a) conventional MN and (b) full pinned MN. The adopted MN has p-type implants, both under the poly-Si gates, and under the gap between TX1 and TX2, in order to accumulate holes at the surface with negative gate biasing. The surface p-type implant makes the MN's threshold voltage higher and increases hole accumulation with the negative gate biasing. Due to the lower effectiveness of negative gate biasing in the region under the gap, a high concentration p-type implant to the gap is required in order to accumulate holes under the gap. However the higher p-type concentration under the gap can make a potential barrier under the gap, and can make it difficult for electrons to transfer from MN to FD. Therefore the dosage of the p-type implant to the gap should be determined considering FWC and image lag of the MN.

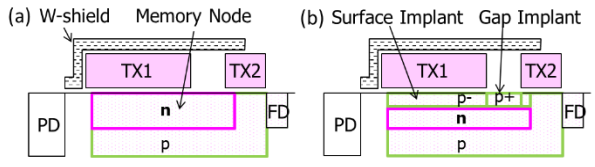


Figure 3: Cross section schematics of (a) conventional MN and (b) full pinned MN.

In order to obtain large FWC even with narrow MN, the MN potential should be kept larger for the entire MN. On the other hand, in order to suppress image lag, electrical field for transfer from MN to FD should be kept larger. To meet both requirements, we successfully designed implant layouts and conditions for MN so that the potential has continuous gentle slope from one edge to the other. Figure 4 shows one-dimensional potential profile of the non-optimized MN and the well-designed MN in this work when TX2 is turned on.

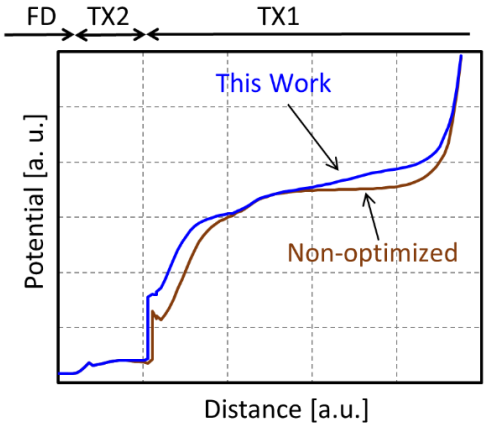
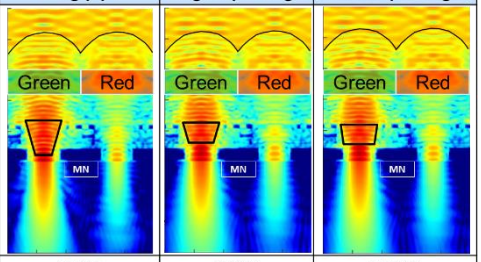


Figure 4: One-dimensional potential profile of the non-optimized MN and the well-designed MN.

OPTICAL DESIGN

Optical design, especially LP, is one of the most important factors to achieve high performances. In order to collect oblique incident light, the upper surface of the LP (L_{upper}) should be maximized. On the other hand, the bottom of the LP (L_{bottom}) must be smaller than the W aperture ($L_{bottom} < L_W$) in order to allow the light to enter into the W aperture without loss. Therefore the LP structure should be tapered. Three types of tapered LP structure were studied comparing 1/PLS at incident angle of 0 degrees and 10 degrees using the 3D-FDTD simulation as shown in Figure 5 (a) and (b) respectively. This is the important note that the simulated QE was comparable for each structure, however 1/PLS was greatly affected by LP structure. A long LP (Type A), had the worst 1/PLS at 0 degrees, because the 2nd reflection at the interface cannot achieve the total reflection due to its incident angle as shown in Figure 6. A large tapered LP (Type B), had the worst 1/PLS at 10 degrees because the larger taper angle makes the range of the incident angle that can be totally reflected narrower. A small tapered LP (Type C) showed the best optical performances. From this work, the new LP design guidelines are described as follows: (1) The height of LP should be designed so that single totally reflected light goes to Si surface through the bottom of LP; (2) The taper angle of the LP should be designed small considering incident angle.

(a) Angle 0 deg.	Type A Long pipe	Type B Large taper angle	Type C Small taper angle
Electric Field			
1/PLS	7700	9800	12500
QE	64.6 %	63.2 %	65.0 %

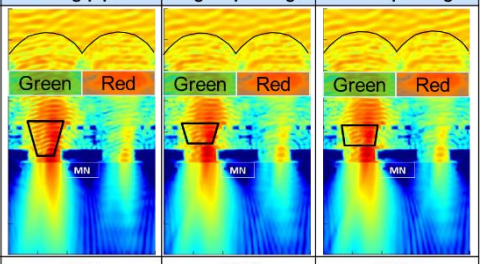
(b) Angle 10 deg.	Type A Long pipe	Type B Large taper angle	Type C Small taper angle
Electric Field			
1/PLS	5600	4500	6000
QE	55.5 %	54.8 %	55.3 %

Figure 5: Comparison of three types of light pipes at
(a) incident angle 0 degree.
(b) incident angle 10 degree.

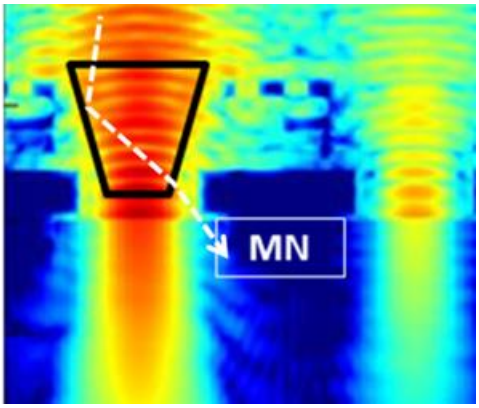


Figure 6: Enlaeged view of type A @ 0 degree.

EXPERIMENTAL RESULTS

The cross-section of newly designed, fabricated 2.5um GS pixel with the small tapered LP is shown in Figure 7. Key pixel performances with color are summarized in Table 2. Linear FWC at PD was 6300ele. FWC at MN was more than 9000ele, which is enough to store electrons transferred from PD. Image lag was well suppressed. Figure 8 shows the distribution of image lag at TX2 with the non-optimized MN and the well-designed MN. The MN in this work shows no outlier distribution of lag at TX2. Dark current and DSNU at MN were 13 ele/s and 24 ele/s at 60 degree C respectively.

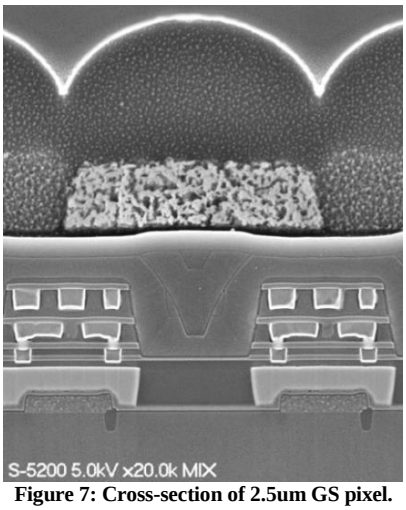


Figure 7: Cross-section of 2.5um GS pixel.

Table 2: Key pixel performances with color

Pixel Performance		Unit	2.5um
Conversion Gain @SF out		uV/ele	100
Linear FWC @PD (max SNR)		ele	6300
Saturated FWC @ MN		ele	>9000
Image Lag @ TX2		ele	None
Image Lag @ TX1		ele	None
Image Lag @ GRST		ele	None
Temporal Noise		ele rms	1.5
Dark Current	@ PD (60C)	ele/s	43
DSNU		ele/s	28
Dark Current	@ MN (60C)	ele/s	13
DSNU		ele/s	24
QE @ Green (λ=530nm)		%	68
AR of Sensitivity		degree	12.5
1/PLS @ F2.8		-	10400

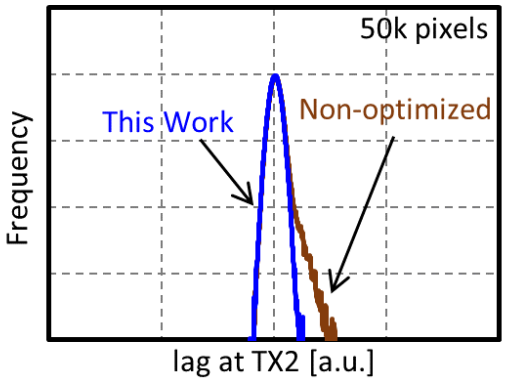


Figure 8: Image lag distribution at TX2.

Figure 9 shows the QE curves. The QE for Green pixel (530nm) was 68% and the peak QE of the monochrome was 78%. As shown in Figure 10, AR of QE maintaining 80% of its peak value was ±12.5 degrees. Figure 11

shows the AR of 1/PLS which was maintained at half value or more in the range of ± 10 degrees. Figure 12 shows the F# dependence of 1/PLS of the color. 1/PLS was very stable down to F # 2.8 and the value was 10400.

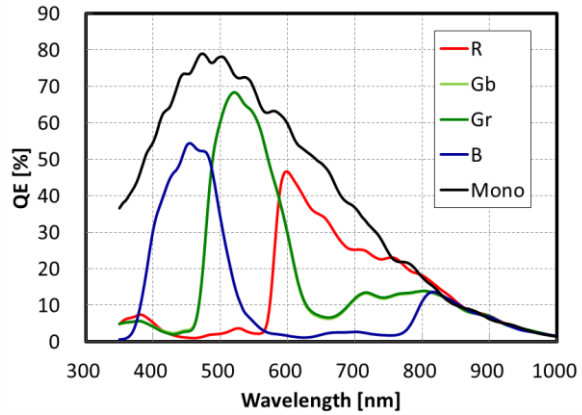


Figure 9: QE curves of 2.5 um GS pixel.

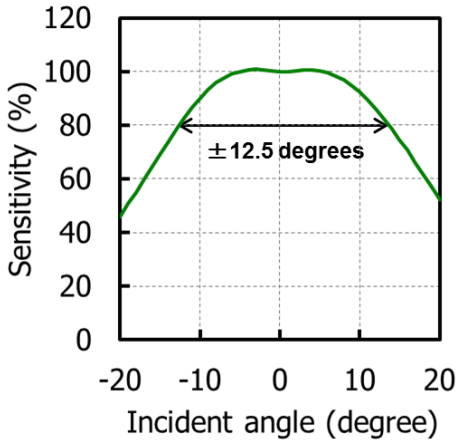


Figure 10: Angular response of QE.

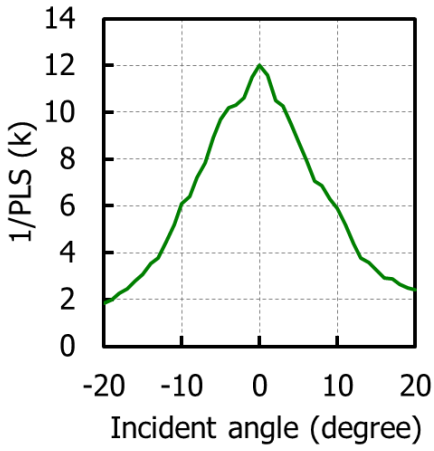


Figure 11: Angular response of 1/PLS with color.

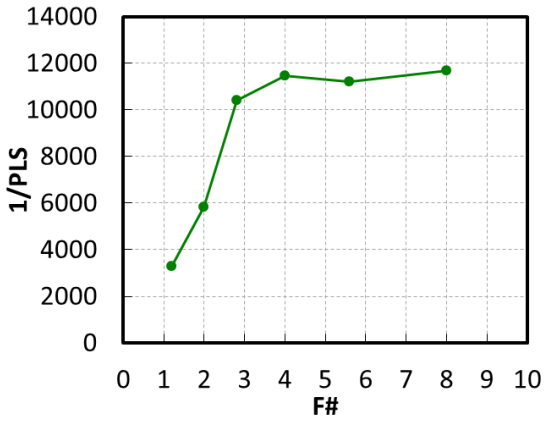


Figure 12: F# dependence of 1/PLS with color.

CONCLUSION

We developed the world's smallest 2.5um charge domain GS pixel with 65nm process. The pixel with color achieved 68% QE and ±12.5 degrees AR. 1/PLS was 10400 with the F#2.8 lens. Table 3 describes the comparison of the monochrome pixel with previous report [7]. Despite the smaller pixel size compared with past reports, the best in class performances were achieved.

Table 3: Comparison table with previous report.

	Unit	This work	[6]
Pixel Pitch	um	2.5	2.8
Linear FWC	ele	6300	6000
Dark Currentat at MN	ele/s	13	60
Peak QE (mono)	%	78	70
1/PLS (mono)	--	8100	2200

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