Impact of Kickback Noise of Comparator in Single Slope ADC on Photon Transfer Curve Characterization

Shang-Fu Yeh, Meng-Hsu Wu, Chih-Lin Lee, Chin Yin, Kuo-Yu Chou, Hon-Yih Tu, Calvin Yi-Ping Chao
Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, ROC
Tel: (886) 3-5636688 Ext 703-3478, email: sfyehe@tsmc.com

***Abstract*—The impact of kickback noises of the comparators in the single-slope column-parallel ADCs on the PTC measurement is studied. The kickback noise affects PTC characterization result, and the measured conversion factor becomes inaccurate. The kickback noise is caused by the coupling voltage from column-wise comparators to a global voltage source of the comparators. A simulation flow is proposed to simulate this effect with acceptable simulation time and accuracy. The simulation result matches the measurement data well. A special test condition is also used to verify the hypothesis. The test condition creates non-uniform images with column gradient to mitigate the kickback effect. The result shows that the measured PTC slope matches the ideal value well.**

Keywords—Kickback Noise, Photon shot noise, Photon transfer curve (PTC), Comparator, Single Slope ADC (SS-ADC)

I. INTRODUCTION

The demand of CMOS image sensor (CIS) in smart phones, wearable devices and automotive industry grew fast in past two decades. In order to obtain important sensor parameters, *e.g.*, digital output to electron conversion factor (e-/DN), photon transfer curve (PTC) [1] is widely used in CIS characterization since photon distribution is ruled by the Poisson process. The PTC method relies on the accurate photon shot noise measurement in a well-controlled light illumination condition where photon shot noise becomes the major noise source. However, in analog readout chain, the kickback (coupling) noise of analog circuit [2] could affect PTC measurement result severely because the measured random noise (RN) is modulated by kickback noise. Fig. 1(a) shows an example. In this case, the measured slope in noise-to-signal log-log plot is 0.42 (solid line). However, the theoretical slope should be 0.5 (dotted line). The noise value in ideal line is calculated from the measured signal value and an estimated conversion factor (3.2 e-/DN). Fig. 1(b) depicts the measured (solid line) and ideal (dotted line) RN histogram. The peak value of measured RN histogram is higher than ideal value, which affects the conversion factor calculation. The consequence is that the extracted conversion factor (e-/DN) becomes inaccurate. In this paper, the effect of kickback noise on PTC measurement is studied. We found that the kickback noise in comparator in column-parallel single-slope ADC (SS-ADC) was the root cause of the PTC slope deviation. Both the simulation and measurement data are presented to support the hypothesis.

II. KICKBACK NOISE IN THE COLUMN ADC

Fig. 2 shows the column ADC and comparator schematic diagram of the chip used in this work. An 8.3 Mpixel array (3296^H x 2512^V) is readout by 1648 column ADCs. The column ADC consists of a gain stage, a comparator and a high-speed counter. A global DAC is used to generate a ramp voltage (Vramp) with a huge filtering capacitor of 1 nF. A global

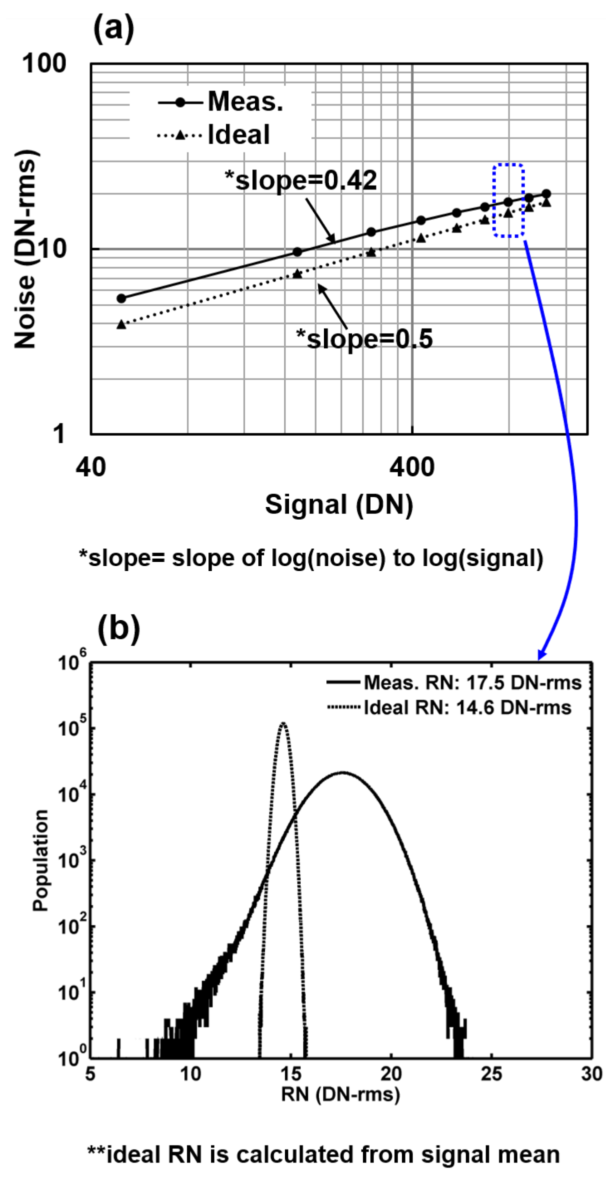

Fig.1(a) The measured noise-to-signal plot. (b) The measured and ideal random noise (RN) histogram.

voltage generator can provide two bias voltages (VBN, VBP) for all comparators. R_{par1}, R_{par2} and R_{par3} represent the parasitic resistance of metal connection between the comparator, the DAC, and the global voltage bias, respectively.

During readout, due to the parasitic coupling capacitance (Cc) in the comparator, the voltage of Vramp, VBN and VBP are coupled by comparator's output voltages (vo1 and vo2) and the voltage of comparator's internal nodes. Moreover, if many

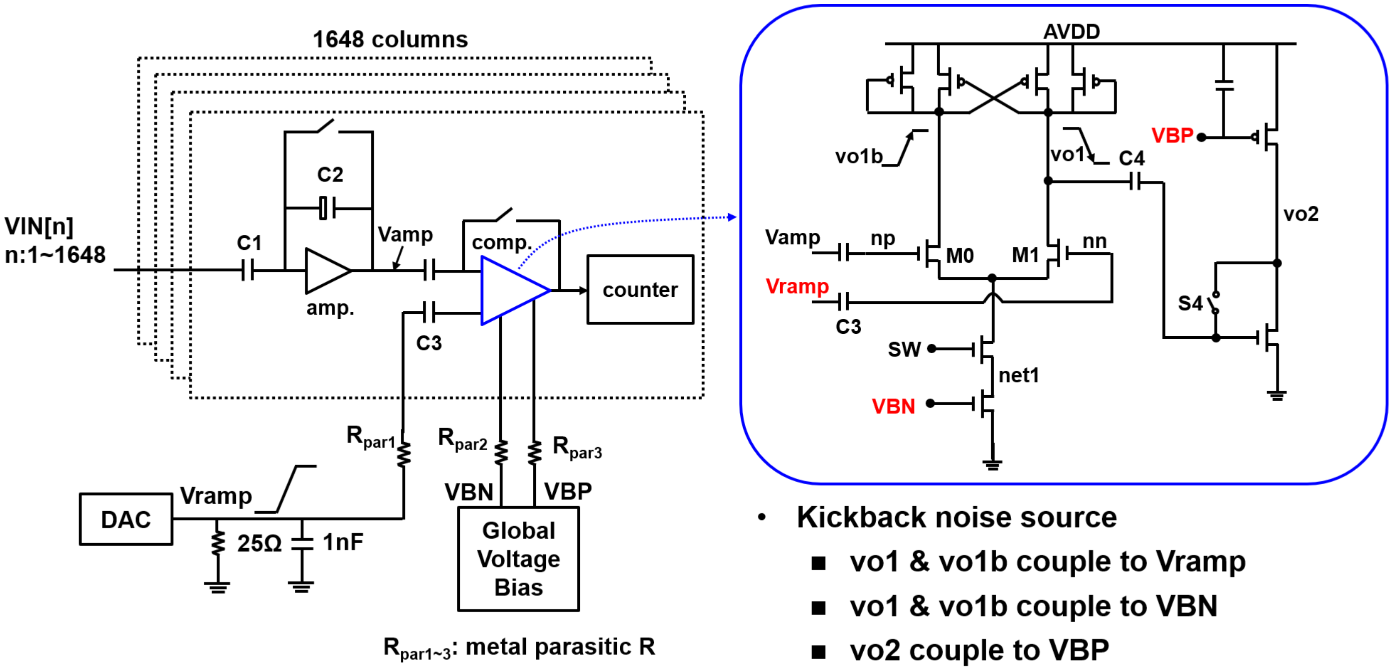

Fig. 2 Column ADC schematic diagram.

Table I

	Value
R_{par1}	30Ω
R_{par2}	618Ω
R_{par3}	923Ω

Table II

Device or nodes		CC [fF]
M0,M1,C_{gs}		46
M0,M1,C_{gd}		3.3
Vramp	vo1	11.3
nn	vo1	2.6
VBN	nn	3.5
VBN	vo1	3.35
VBN	net1	2.35
VBP	vo2	2.1

Table III

Target e_{sig} [e-]	Target shot noise $\sqrt{e_{sig}}$ [e-rms]	e_{sig} of N input signals [e-] (N=1648)	$\sqrt{e_{sig}}$ of N input signals [e-rms] (N=1648)	Signal $\sqrt{e_{sig}}$ / target $\sqrt{e_{sig}}$ (%)
1000	31.623	998.629	31.622	99.999%
1500	38.730	1499.547	38.729	99.999%
2000	44.721	1999.477	44.721	99.999%
2500	50	2502.174	50.001	100.001%
3000	54.772	3002.381	54.773	100.001%

comparators flip in a short period, the accumulated coupling voltage on Vramp, VBN and VBP become larger. The consequence is that early flipped comparators will inject kickback noise to Vramp, VBN and VBP, and then affect the later flipped comparators which are going to flip soon since the bias voltages are changed. This leads to an abnormal noise histogram as shown in Fig. 1(b). The scenario becomes worse when a uniform light source is applied in CIS characterization since most of comparators flip in a short period.

In order to address this issue, the global voltage bias should have strong driving (or high bandwidth) to quickly recover VBN & VBP to their original levels once they suffer from kickback noise. The trade-off is that the thermal noise of VBN & VBP become larger, which increases the noise floor of analog readout chain. Moreover, the value of R_{par1}, R_{par2} and R_{par3} should be as small as possible for shorter recovery time of Vramp, VBN and VBP. Table I shows the value of R_{par1}, R_{par2} and R_{par3}. Table II shows the extracted coupling capacitance in the comparator with a layout pitch of 1.6 um in N22 technology. The large values of R_{par2} and R_{par3} are due to long distance between the global voltage bias and column comparators (>1000 um). In the revised metal-ECO chip, the R_{par2} and R_{par3} are decreased to around 20 ohm and 45 ohm, respectively, by using top thick metal for the connection.

III. Simulation Flow

In order to verify the hypothesis, we propose a simulation flow to check the impact of kickback noise on the PTC characteristic. There are two challenges in the simulation. The first one is how to model photon shot noise with Poisson distribution in SPICE-like simulator. The second is how to simulate a complicated circuit, which includes 1648 column circuits, a global DAC and a bias circuit, with the shot noise model in an efficient way. Otherwise, the simulation time could be too long, and it is difficult to fine-tune (or debug) the column circuit.

Fig. 3 depicts the proposed simulation flow. First, a parasitic extracted netlist with N column circuit (N=1648 in this case) is prepared. A piecewise linear (PWL) current source is used to replace the real DAC circuit for netlist simplification. The PWL current source output connects to a 25-ohm resistor and 1-nF filtering capacitor to ground. The R_{par1}, R_{par2} and R_{par3} are included in the netlist as well. The next step is to create photon shot noise patterns for 1648 column circuits inputs. In order to mimic the real pixel output distribution among columns in PTC measurement, we use a software program to generate 1648 random numbers for 1648 column circuits inputs whose

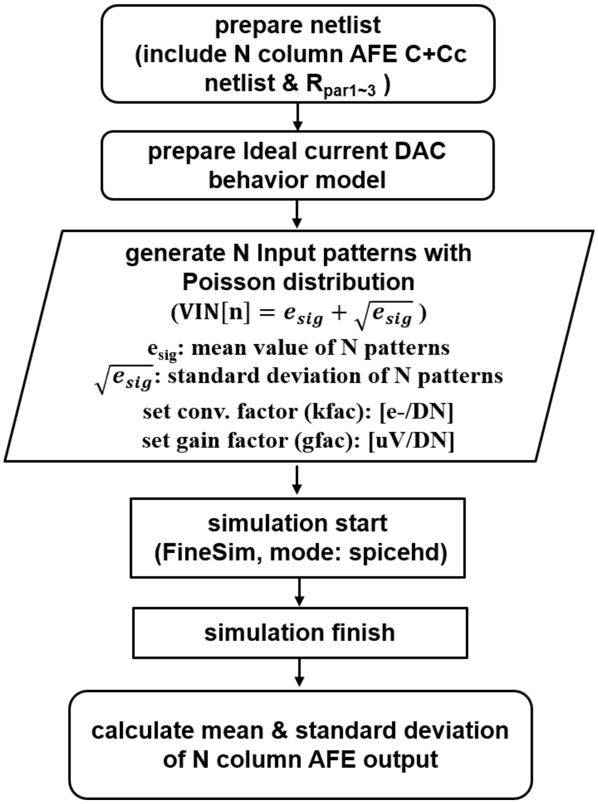

Fig. 3 Proposed simulation flow.

signal mean is "e_{sig}" and standard deviation is "square root of e_{sig}". Five simulation cases of signal mean (e_{sig}) =1000e- ~3000e- are performed. In each case, the 1648 input signals with voltage swing of the Poisson distribution are used as column ADC inputs. Because the random data are picked carefully, the standard deviation of the generated 1648 input signals are very close to ideal shot noises, as shown in Table III. In this work, there is only 0.001% error between ideal and generated shot noise. The estimated conversion factor (e-/DN) and gain factor (uV/DN) are applied to convert input signal unit from electron to voltage in the simulation. A transient simulation is performed without mismatch model.

In the simulation, we use Synopsys "FineSim" (mode: spicehd) to speed up simulation time and keep reasonable accuracy. When transient simulation finishes, the signal mean and noise (standard deviation) can be calculated from 1648 column circuits outputs. Unlike the convention transient noise and frequency domain noise simulation, we calculate the kickback noise effect from total 1648 column circuits outputs since kickback effect is caused by the fact that global bias voltages of comparators are coupled by early flipped comparators, and then affect later flipped comparators bias point. With kickback effect, the histogram of 1648 column circuits outputs is not the same as the input signal histogram which has the Poisson distribution, as shown in Table III.

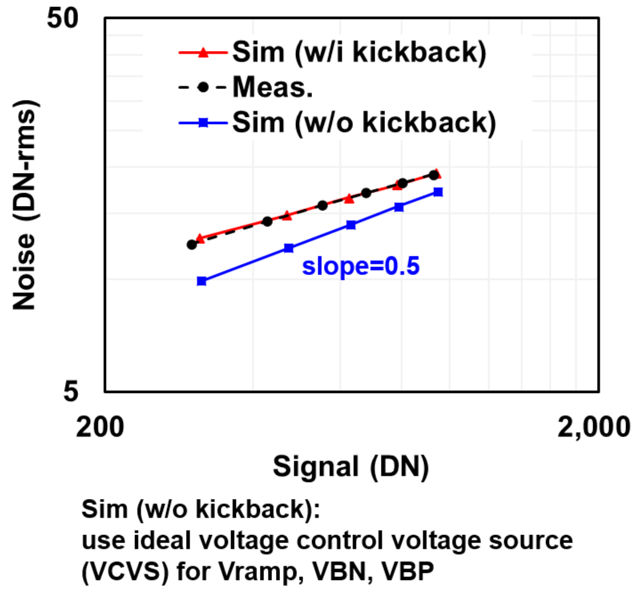

Fig. 4 Simulated noise-to-signal plot.

Fig. 4 shows the simulation result. The simulation results (red line) match the measurement data well in the signal range of 300DN~1000DN. On the other hand, the transient simulation result without kickback noise is also presented (blue line). The ideal voltage-controlled voltage sources (VCVS) for Vramp, VBN and VBP without R_{par1}, R_{par2} and R_{par3} are used and connected to all comparators to get rid of voltage coupling. The result shows a slope of 0.5 in noise-to-signal log-log plot, which matches input signal patterns with the Poisson distribution. The proposed simulation flow excludes device flicker and thermal noises and only includes photon shot noise to evaluate the kickback noise effect from the circuit. In measurement, with proper light intensity and exposure setting, photon shot noise becomes the major noise source which is much larger than the flicker and thermal noises from the readout chain. The proposed method can also be used in design phase to check the kickback effect.

IV. Measurement Validation

A special measurement setup is proposed to verify the hypothesis, as illustrated in Fig. 5. Two black tapes are sticked on the glass of the chip to produce a light shield image. The column mean signal of the image is shown in Fig. 5 as well. Since the light shield setup, the central pixels have higher signal than the pixels in the left and right side of the array. This method creates a signal gradient cross column, so the comparators flip time are dispersed in the whole A/D conversion period. The accumulated kickback effect become less, and the impact of kickback noise on PTC measurement should be mitigated.

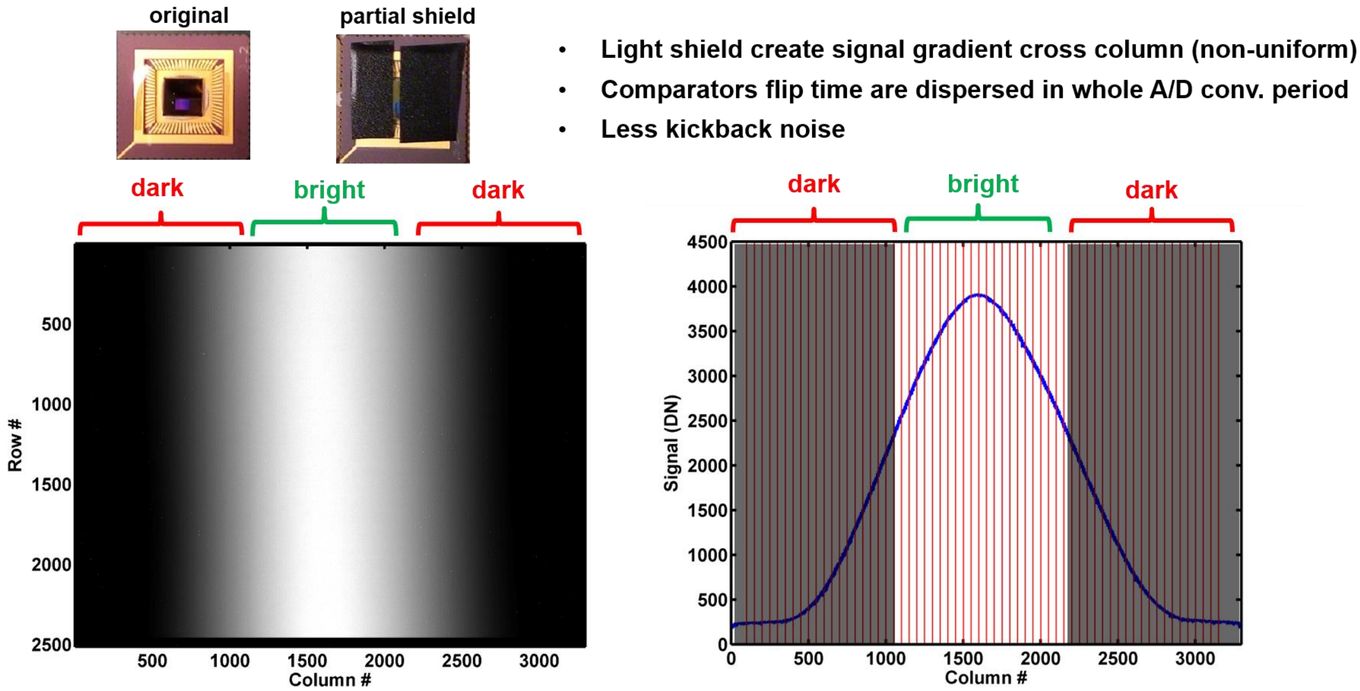

Fig. 5 A special measurement setup to mitigate the kickback noise.

The whole array data can be divided into many groups, and each group includes $50^{H}x2512^{V}$ pixels. Fig. 6 shows the measured data from the central group with peak column signal. The slope matches the theoretical value of 0.5 well. This implies that the kickback noise of the comparator in SS ADC must be minimized for better noise performance. The measured conversion factor is around 3.3e-/DN.

V. Conclusions

In this work, the impact of the kickback noise of the comparator in the single-slope ADC on the PTC measurement is presented. The kickback noise affects the PTC characterization result, and the calculated conversion factor becomes inaccurate. A simulation flow is proposed to simulate this effect with acceptable simulation time and accuracy. The simulation results match the measurement data well. A special test condition is also used to verify the hypothesis. The test condition creates non-uniform images with column gradient to mitigate the kickback effect. The test chip setting is kept the same. The result shows that the measured PTC slope matches the ideal value well.

References

[1] J. R. Janesick, *Photon Transfer* DN→λ. SPIE, 2007.
[2] P. M. Figueiredo. *et al.*,*ISCAS*,2004,pp.I-537-540.

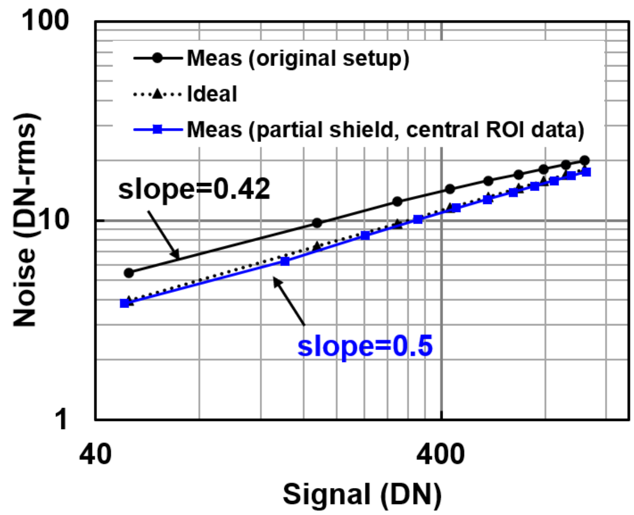

Fig. 6 Measured noise to signal plot without shielding (black) and the central ROI data (blue) with partial shielding.