Low-noise and High-performance 3-D Pixel Transistor for Sub-micron CMOS Image Sensors Applications

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***Abstract*— We demonstrated a back-illuminated CMOS image sensor, employing fin field-effect transistors (FinFETs) for in-pixel source-follower (SF) amplifiers. For comparison, two types of SF amplifiers i.e. planar type and FinFET were fabricated and the latter was formed by simply adding a Si etch step on the transistor channel region. Interface trap density was measured to be similar for both, indicating that the etched channel surface of FinFET was comparable to the pristine Si surface of the planar SF. Furthermore, the FinFET SF has increased the trans-conductance (g_m) by 37% compared to the planar SF, which also led to improvement of random telegraph signal (RTS) noise by 30% without any image performance degradation. Such improvements are indicative of increase of the effective channel width by the fin structure. We firmly believe that the integration of FinFET transistors to a pixel array accelerates scaling down of a pixel pitch, which is crucial for image sensors in the mobile market.**

Keywords—CMOS Image Sensors, Fin Field-effect Transistors, Source-follower Amplifiers, Random Telegraph Signal Noise.

I. INTRODUCTION

CMOS image sensor (CIS) industry moves fast toward small-pitch (<1um), high-resolution (>100 Mega-pixels) sensors for the past years by the strong demands from growing mobile markets [1]. In order to make pixel-pitch smaller, transistors in each pixel should be scaled down as well. Such scaling inherently deteriorates electrical characteristics of transistors such as trans-conductance (g_m), turn-off leakage current, or flicker (*1/f*) noise. Among in-pixel transistors, a pixel amplifier or a source follower (SF) transistor, in particular, is of utmost importance because it determines linearity and noise performances of pixel. For instance, low trans-conductance (g_m) of SF results in the large RC delay which causes the column-wise fixed pattern noise (CFPN) for CISs with columnar analog-to-digital converters. In addition, the smaller the SF channel area is, the more severe temporal signal fluctuation, i.e. random telegraph signal (RTS) noise occurs due to capture-emission of electrons by interface traps at the SF channel. Therefore, maximizing the effective channel width of SF in the given pixel area is the key to the continuing pixel shrink.

In this work, we incorporated 3-dimensional (3-D) fin-type SF transistors into a submicron-pitched image sensors to overcome such fundamental limitations, which is the first demonstration to our best knowledge. The fabrication processes are presented followed by excellent device performance improvements i.e. g_m by 37% compared to the planar counterpart as well as image quality improvement of RTS noise by 30% without compromising other sensor performances.

II. DEVICE FABRICATION

In order to study a FinFET pixel amplifier, we fabricated a 4-transistor active pixel sensor (4-T APS) with 0.64-μm pixel pitch where each photodiode (PD) is isolated by full-depth deep trench isolation (DTI) [2]. Four floating diffusion (FD) nodes i.e. four PDs are shared over the same color filter in order to realize pixel-level adaptive gain control as well as to increase pixel sensitivity at a low illumination condition. Consequently, multiple in-pixel SF amplifiers from the shared pixels should be connected through metal interconnects.

In general, fin field-effect transistors (FinFETs) are formed using double patterning technology (DPT) which is restrictive applying to pixel transistors due to increased fabrication cost. In this work, however a single photolithography patterning prior to a Si dry etch step was utilized to form a FinFET SF as shown in Figure 1(a)-(b). Fabrication processes of the 3-D FinFET SF are illustrated in Figure 1(c). First, the active Si region was defined by the shallow trench isolation (STI), followed by boron ion-implantation to form p-type body nodes. Then, a single exposure photolithography patterned two rectangles etched into Si active region to form a fin-type

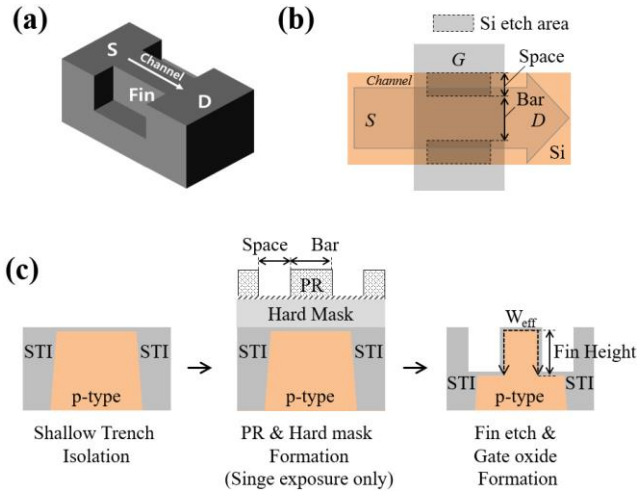

Figure 1. (a) A schematic illustration of 3-D FinFET in-pixel SF transistor. (b) The bar and space patterns and (c) the fabrication processes to etch Si to form FinFET structure with single-step photolithography.

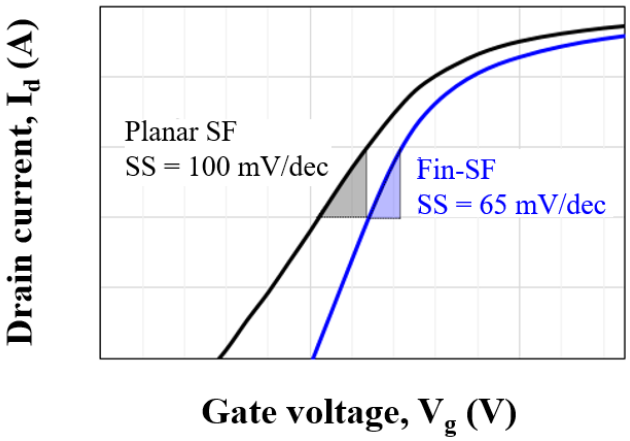

Figure 2. Current-voltage (*I-V*) cureves of the drain currents and gate voltages of in-pixel SF transistors with a FinFET structure (blue) and a planar structure (black).

Si gate with bar and space patterns as shown in Figure 1(b), which defines the channel width. Subsequently, various Si etch depths were applied to define the channel height. As a result, the width and height of the SF channel determine the effective channel width (W_{eff}) that is a critical factor for device performances such as g_m. The gate oxide around the 3-D Si channel was grown by an advanced thermal oxidation technique which helped remove the etch damages on the channel. Poly-Si was deposited and patterned to wrap around the fin-type channel, followed by metallization.

III. Results and Discussion

Test structures of SF amplifiers electrically isolated from the pixel array were placed adjacently to the actual sensor chips and measured for correlation between device performances and sensor characteristics. Figure 2(a) shows current-voltage (*I-V*) characteristics of the fabricated FinFET SF compared to a planar one. The sub-threshold swing was 65 mV per a decade which is superior to 100 mV of that of the planar counterpart, which suggests that gate-controllability was improved and in turn leakage current at the off stage was suppressed. However, SF amplifiers in pixels are operated at saturation mode and therefore, g_m at the actual pixel operation conditions are much more important in terms of pixel linearity and noise performances of sensors. The g_m values of a FinFET SF with the fin height of *A* Å increased by 17% compared to the planar SF as shown in Figure 3. Moreover, g_m increases proportionally as the fin height increases up to *C* Å where g_m enhancement over the planar SF reaches 37%.

$$W_{eff} = \frac{L \cdot (g_m{}^2)}{2\mu C_{ox} I_{bias}} \qquad (1)$$

The effective channel width, W_{eff} was estimated by using the Equation (1) and the increase of g_m at *C* Å, by 37% corresponds to the increase of 88% in W_{eff}. This indicates that the fully wrapped-around 3-D channel of a FinFET SF was formed and controlled by the voltage at the poly-silicon gate without any short channel effects or punch-through between the source and drain nodes.

In spite of the improved g_m, the degradation of the interface between the etched Si channel and gate dielectrics is of concern since the 3-D fin-type channel was formed by dry etch. Poor interface quality increases the interface trap density (N_{it}), which results in current fluctuation over time. Such temporal current fluctuation causes flickering pixels at low illumination which worsens the one of sensor performance metrics i.e. RTS noise. N_{it} values of both types of SFs were measured using a charge pumping method as shown in Figure 4. It shows there is no significant degradation of N_{it} for a FinFET SF.

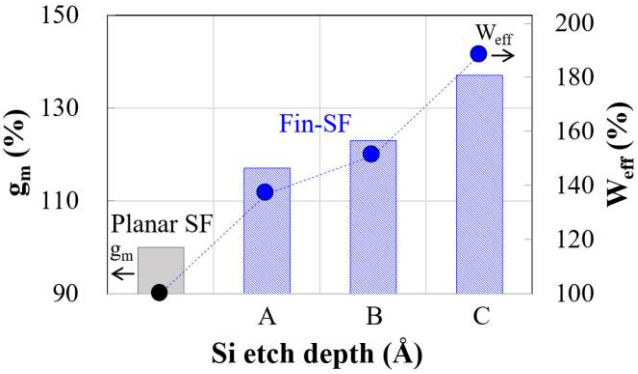

Figure 3. The trans-conductance (g_m) of both planar and the FinFET SF (in-left axis) transistors depending on the fin height and corresponding W_{eff} (in-right axis) calculated with Equation (1).

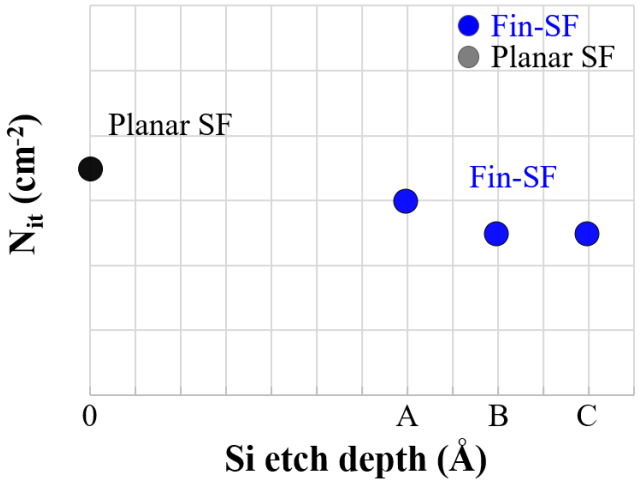

Figure 4. The interface trap density (N_{it}) both planar (black) and the FinFET SF transistor (blue) depending on the fin height.

To quantitatively evaluate the RTS noise, two consecutive frames of images were taken at dark condition with a high analog gain. Then pixel-by-pixel output differences were plotted in histogram as shown in Figure 5. First, the distributions near the zero difference i.e. the peak of the histogram almost completely overlap for both types of SFs, which implies that the thermal noise components are comparable regardless of the SF types. Meanwhile, the tails of the distribution vary, which suggests that the types of SFs influence the flicker noises a.k.a *1/f* noises. The slope of tails in log-scale is steeper for a FinFET SF which means that the temporal current fluctuations in FinFET SFs have been lowered. [3-5] The *1/f* noise is mainly governed by channel area (W_{eff}×L) and the FinFET SF increases channel area at the given layout due to the 3-D nature of the transistor channel. The histograms in Figure 5(a) show more improvement of the RTS noise as the fin height increases. It also improved as the number of fin is increased in Figure 5(b). It gives one a more degree of freedom in optimizing the design of a FinFET SF.

In addition, the RTS noise in the unit of parts-per-million (ppm) was obtained by counting the number of pixels that showed higher differences than a certain criterion. The RTS in ppm is lower for a FinFET SF due to the larger channel area. It was also found that the larger fin height or the more numbers of fins further reduce the RTS which matches the assessment with the RTS improvement due to the increase of the effective channel area. We also measured the RTS noise in a wafer-level testing showing a significant decrease from 100% to 32.4% ppm as shown in Figure 6. Therefore the RTS noise improvement by almost 70% utilizing a FinFET SF is viable option for a mass production of CIS chips.

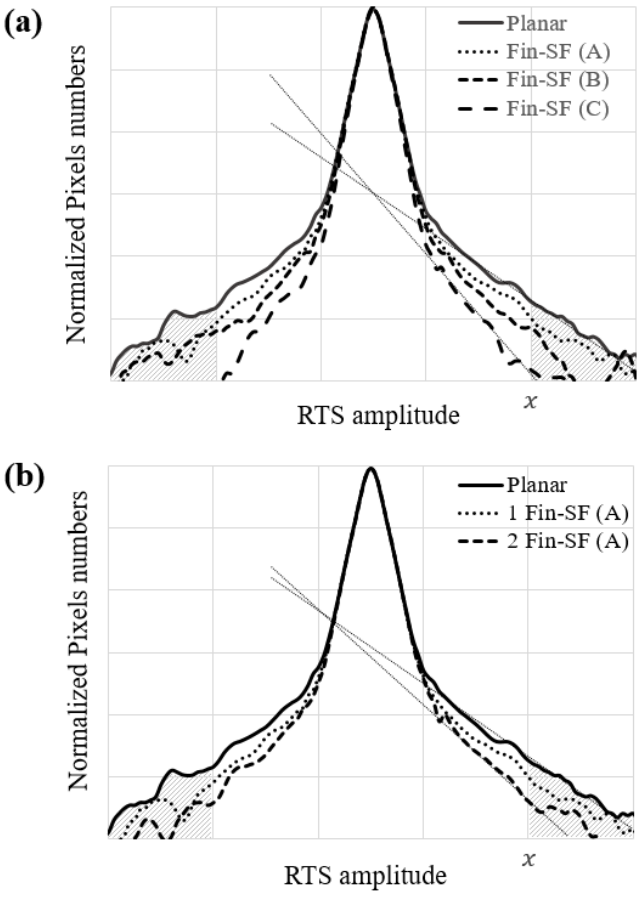

Figure 5. The distribution of pixel-by-pixel output differences in two consecutive frames at dark condition with an in-pixel SF of a FinFET type and a planar type compared by (a) the fin height and (b) the number of fins in a SF transistor.

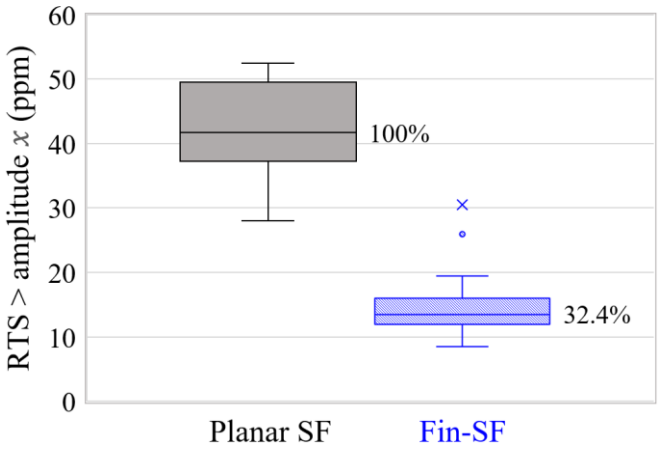

Figure 6. The wafer-level testing results of the RTS noise in ppm with in-pixel SF of the Planar type and the Fin type.

Other pixel performances were characterized to confirm that the RTS noise improvement by a FinFET SF. As summarized in Table 1, there is no significant deterioration in other pixel performances including full well capacity (FWC) and conversion gain (C.G) with a FinFET SF while the flicker noise component of random temporal noise (R.N) and the RTS noise were improved.

	Planar SF	**Fin-SF**
RTS> amplitude x	100%	32.4%
R.N (flicker)	100%	81%
C.G	100%	102%
FWC	100%	98%

Table 1. The summary of typical pixel performances with in-pixel SF transistor of a planar and a FinFET SF

IV. CONCLUSION

We demonstrated a 3-D FinFET type in-pixel SF transistor integrated to a submicron pixel chip for the first time known today. A cost-effective single photolithography was used to form the fin channels unlike the conventional double patterning processes. By adopting a FinFET SF, sub-threshold swing and trans-conductance of SFs were improved which ensured an adequate pixel linearity. Furthermore, the effective channel width significantly enhanced and consequently it improved the RTS noise. The RTS improvement caused no side-effects in other pixel performances. This achievement may allow further scaling down in pixel pitch without inevitable deterioration of the RTS noise performance as the SF area is minimized for the future image sensors in a small form factor and high resolution.

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