Innovating CMOS pixel potentials and Full Well Capacity extraction methods from test structures.

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Abstract*—In addition to product level measurements, parameters extraction on test structures is a powerful tool for pixel and technology development and also for device level reliability study or process monitoring. In this paper is proposed a method in order to extract pixels potentials of interest such as the photodiode pinning potential or the potential under a transistor gate. It is based on the use of the EKV model together with measurements on adequate test structures. Thanks to the so-called "Y function series resistance correction", the method can even be applied to test structures including devices in series as in real pixel. A second developed method is proposed to extract the Full Well Capacity considering different contributors thanks to simple I(V) and capacitance measurements on test structures. This method highlights the strong dependence of this parameter on the experimental conditions. Both methods are validated thanks to TCAD simulations.

I.INTRODUCTION

Characterizing potentials in pixels like the photodiode pinned potential or the potential under a switched off transfer gate can be interesting to ensure that the charge retention and transfer will be optimum and so that pixels could operate properly with required features. Important parameters such as the Full Well Capacity (FWC) or the lag depend on these potentials. Some potentials of interest are represented on Fig.1, showing an example of a 6T global shutter pixel. In this paper is proposed a new way of characterizing potentials and the Full Well Capacity on test structures. Such characterizations performed at device level on test structures are very useful for process and pixel developments, process monitoring, reliability study and TCAD calibration. In Section II, a quick review of the state of the art concerning the measurement of potentials and Full Well Capacity on test structures is done. The new method proposed in order to extract potentials based on the EKV model is described in Section III. The method developed to extract the Full Well Capacity on test structures is detailed in Section IV.

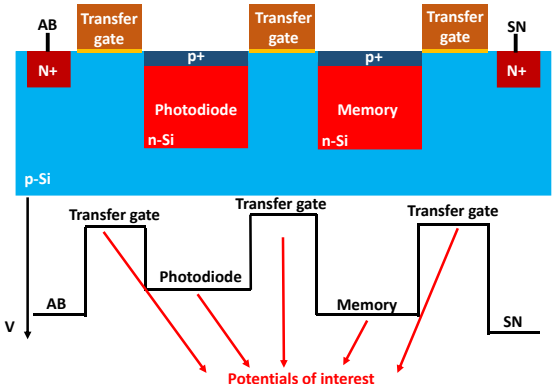

Fig.1 : Example of a global shutter pixel cross-section with potentials of interest that could be interesting to extract. The pixel includes a pinned photodiode, a memory, two transfer-gates, a sense node, and also an antiblooming node controlled by a gate that could also reset the photodiode.

II.STATE OF THE ART

A. Potentials measurements

Absolute potentials measurements by injection techniques already exist at imager product level [1] [2] [3] and enable extractions such as the pinning voltage V_{pinned}, which is the photodiode potential when it is free of charge, and the potential under a switched off transfer gate located just after a photodiode. In order to extract a specific potential in a pixel array, the measurement must not be disturbed by other elements of the readout chain. Therefore, an alternative is to perform the measurement on test structures, by ensuring that a representative device environment is well reproduced. Here too, several methods exist. As presented in [1] [4], either these methods provide absolute potentials and can only be used on photodiodes (JFET and capacitive methods) either they can be applied on both photodiodes and transistors but do not provide absolute potential (floating source and current methods).

In this paper, a new method based on the current method is proposed (already published in [4]) by applying the EKV (Enz-Krummenacher-Vittoz) model, making it valid for the extraction of most of the potentials in a pixel: pinning voltage, potential under a gate at high or low bias, or any other fixed potentials within a pixel. This improved method allows precise and absolute potential barriers extraction.

B. Full Well Capacity measurements

The Full Well Capacity, which described the capacity of the photodiode to store charge, depends directly on the potentials surrounding the photodiode as shown on Fig.1. A typical measurement method on the whole sensor consists in measuring the signal stored in the photodiode as a function of time under illumination or in the dark. When the integrated charge reaches saturation, the Full Well Capacity is extracted. It is generally given as a single value but it depends on experimental conditions such as the luminous flux for example. Different conditions give different extracted values and so have to be specified together.

To our knowledge, no method exists on test structures. However, working on test structures allows in a simpler way the study of the impact of process or

geometry variations, of the different contributions (photodiode capacitance and potentials surrounding the photodiode) on this parameter. Also, by comparing the values extracted both on test structures and complete sensors, it can be determined if the Full Well Capacity is limited by the photodiode or by the readout circuitry for example.

Firstly, the method to extract potential within a pixel is presented in detail, then the Full Well Capacity extraction is studied later on.

III.NEW POTENTIALS EXTRACTION METHOD BASED ON THE EKV MODEL

As it is presented in [4], the extraction of potentials of interest can be performed thanks to Id(Vs) characteristics associated with the EKV model [5], which describes the measured transistor drain current and integrates the potential parameter in order to make the extraction simple. The potential V_p is employed, which is the potential for which the inversion charge becomes zero (pinch off), for a given gate voltage V_g (Fig.2). V_p is then assimilated to the potential of interest which has to be extracted. More details are available in [4].

In order to allow the extractions, the linear regime of the EKV model is used for a given V_g with the source voltage $V_s < V_p$ and the drain voltage $V_d < V_p$ and typically $V_\Delta = V_d - V_s = 10mV$:

$$I_d = n\beta\left(V_p - V_s - \frac{V_\Delta}{2}\right)V_\Delta \qquad (1)$$

with $n = \frac{\partial V_p}{\partial V_g}$, $\beta = \mu_n C_{ox}\frac{W}{L}$ (L and W gate dimensions), μ_n the electron mobility, C_{ox} the oxide capacitance, V_p the pinch off voltage and V_s the source voltage. From a simple Id(Vs) measurement, a linear regression seems to be enough to extract the potential V_p. However, in case of strong series resistances such as in pixel environment, the curve is no longer perfectly linear, disturbing the extraction. To avoid this resistance issue, the Y function usually used for the threshold voltage extractions and only available for the linear régime is applied [6]. The Y function applied to the EKV model is described as:

$$Y = \frac{I_d}{\sqrt{|g_{ms}|}} = \sqrt{n\beta V_\Delta}\left(V_p - V_s - \frac{V_\Delta}{2}\right) \qquad (2)$$

with $g_{ms} = \frac{\partial I_d}{\partial V_s}$. It can be seen that the function is linear with V_s, the extraction of V_p is then straightforward; when the Y function becomes zero, $V_s = V_p - \frac{V_\Delta}{2}$. An example of extraction on a transistor can be seen in Fig.3.

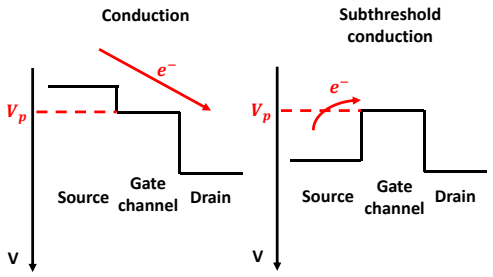

Fig.2 : Potential diagram showing the two regimes of a transistor MOS driven by the V_p potential.

The proposed extraction method initially based on EKV model for MOS transistor operation remains valid to extract photodiode pinning voltage. Photodiodes are assumed to be similar to a JFET for which the expression in the linear regime is very closed to the EKV model for MOS [7]. All these results were verified thanks to TCAD simulations [4] and therefore this new method can be applied on test structures like the ones presented on Fig.4.

This method can also be applied on more complex structures such as a pinned photodiode with a transfer transistor in series as shown in Fig.5. To keep the pixel environment strictly unchanged, even more complex structures can be used for example including an antiblooming node. In such cases, devices in series comes with associated series resistances but thanks to the Y function, their impact can be eliminated. This enables for example to investigate potential barriers between a photodiode and a transfer gate which is a key parameter, as it drives the charge retention capability of a photodiode and then its Full Well Capacity if it is limited

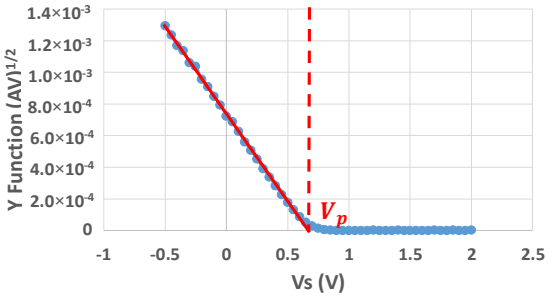

Fig.3 : Y function applied on a Id(Vs) curve to extract the potential of interest.

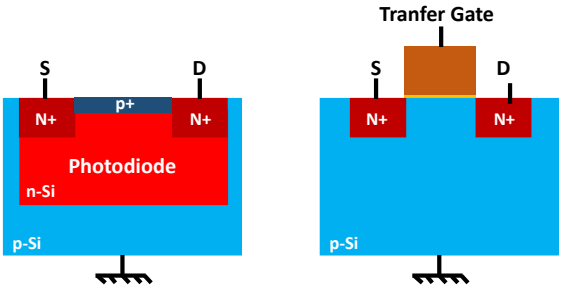

Fig.4 : Photodiode and transistor test structures used to extract the photodiode pinning potential and the potential under a switched off transistor

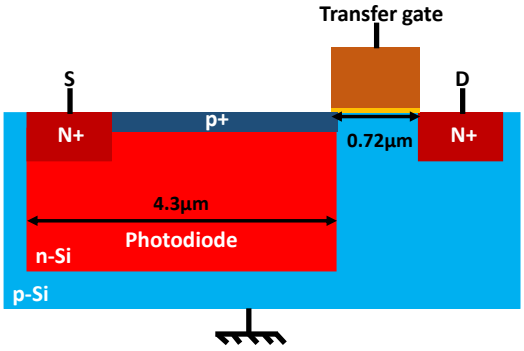

Fig.5 : Schematic diagram of a test structure including a pinned photodiode and a transfer gate in series in order to extract the potential barrier between the two.

by the transfer gate. As for a single device, Id(Vs) curves are measured to extract the limiting potential V_{lim} of the structure for several V_g as described previously. As an example, the structure shown in Fig.5 enables the extraction of the limiting potential of the structure depending on the applied gate voltage as presented in Fig.6 [4]. Therefore, with this type of structure it is possible to extract the potential barrier between the empty photodiode and the switched off transistor which gives information about the storage capability of the photodiode.

IV.FULL WELL CAPACITY EXTRACTION ON TEST STRUCTURES

In the previous section was presented the possible extraction of potential barriers which are key parameters for Full Well Capacity. This section presents a new methodology to go further and extract a Full Well Capacity value on test structures. The Full Well Capacity depends on several parameter as it can be seen with the relation (3) [8]:

$$FWC = \frac{1}{q}\int_{V_{eq}}^{V_{pinned}} C_{PD}(V)\, dV \qquad (3)$$

with q the elementary charge, V_{eq} the equilibrium potential of the photodiode and $C_{PD}(V)$ the photodiode capacitance. Under experimental conditions (temperature, illumination, etc.), the photodiode fills up and so its potential will decrease until reaching an equilibrium V_{eq} achieved when the incoming current (photogenerated and dark currents) is equal to the outgoing current (transistor's subthreshold current). This equilibrium state depends strongly on the experimental conditions [8].

In order to extract a value of the Full Well Capacity, V_{pinned}, V_{eq} and $C_{PD}(V)$ have to be known. It can be noticed that V_{pinned} can be extracted thanks to the method described in section III on a test structure such as the one presented in Fig.4. The following sections will focus on V_{eq} extraction and $C_{PD}(V)$ measurement.

A. Photodiode equilibrium potential extraction under given experimental conditions.

Extracting the equilibrium potential of the photodiode under given experimental conditions can be performed thanks to the Id(Vs) curve used to extract the potential under the gate of the transistor (for instance in Fig.5) for a given V_g. Indeed, when the potential V_p for a given V_g is lower than V_{pinned} the Id(Vs) subthreshold part of the curve represents the different equilibrium potentials reachable by the photodiode. As previously stated, the equilibrium is reached when the photogenerated and dark currents are equal to the transistor's subthreshold current. Firstly, the photogenerated and dark currents have to be known. It can be done by measuring the dark current and the quantum efficiency on whole sensors and by knowing the luminous flux. Secondly, the sum of these dark and photogenerated currents gives the equilibrium subthreshold current $I_{subtheq}$. Finally, the V_{eq} potential is then extracted as the Vs for this $I_{subtheq}$ current on the Id(Vs) curve as shown on Fig.7. This result can be verified thanks to Sentaurus Sprocess 2D TCAD simulations. The Id(Vs) curve can be simulated from the TCAD structure shown on Fig.8. On a similar structure where the source is removed, the photocurrent and dark currents are simulated for different light flux and the equilibrium potential (quasi Fermi potential) is extracted directly on this simulated structure. It is therefore possible to obtain a curve representing the incoming currents (dark and photogenerated currents) I_{in} in the photodiode as a function of the equilibrium potential extracted for the different light flux. The comparison between the obtained $I_{in}(V_{eq})$ and the Id(Vs) curves for the same V_g, here $0V$, is available on Fig.8. The two curves are almost overlapping proving that the methodology presented here to extract the equilibrium potential of the photodiode for given experimental conditions is coherent (only a 4mV discrepancy is noted on Fig.8 between the two curves). Similar agreements are obtained when varying V_g, the temperature or the device geometry.

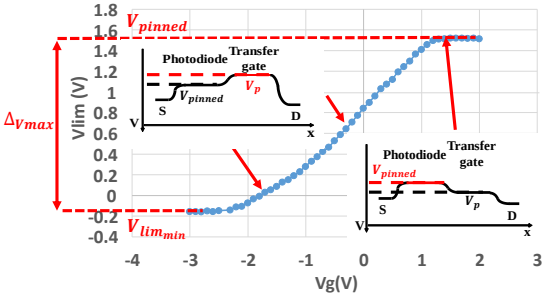

Fig.6 : Limiting potential extraction as a function of Vg applied on the gate of the Fig.4 structure. This measurement allows the extraction of the potential barrier between the empty photodiode and the closed transfer gate.

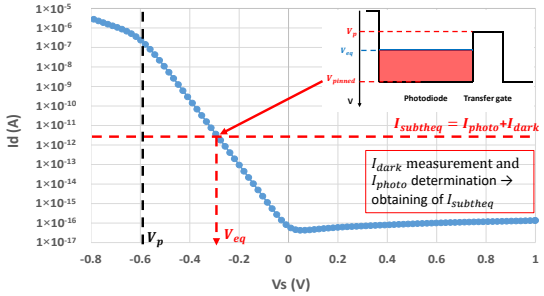

Fig. 7: I(V) measurement obtained on a Fig.3 like structure for $V_g = 0V$ to extract the equilibrium potential of the photodiode as a fonction of the experimental conditions.

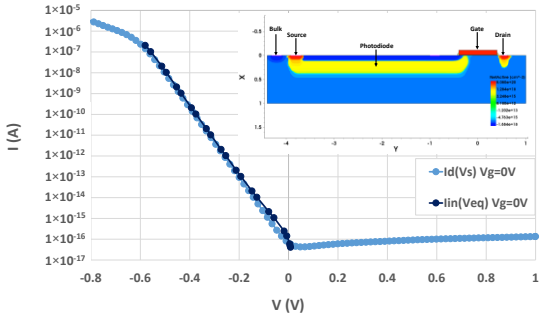

Fig. 8: Comparison between the simulated Id(Vs) curve and the Iin(Veq) curve with Iin the incoming current of the photodiode.

B. Photodiode capacitance measurement and Full Well Capacity extraction.

Now that all the potentials needed to extract the Full Well Capacity are known, it is necessary to extract the capacitance of the photodiode as a function of its potential according to the relation (3). The capacitance of the photodiode can be measured between the antiblooming node and the bulk on structures like the one shown on Fig.1 implemented in an array and with a sufficient gate voltage to open the access to the diode. An example of a C(V) measurement is available with the Fig.9. It can be noticed that for potential higher than the pinning potential of the photodiode, a parasitic capacitance remains that needs to be removed because it actually does not participate in the capacitance of the photodiode. The examination of the parasitic capacitance's behavior with voltage or even simulations can enable to identify the contributions and mechanisms and then to extrapolate them to lower voltage range where they have to be subtracted to isolate the photodiode's capacitance. Here only a relatively simple junction capacitance model is used [9], globally for drain/substrate and channel/substrate junctions identified contributions. It stays empirical and could be refined. It has been noted that errors are more important for low potentials where correction's weight is stronger and probably less accurate since extrapolated further.

Knowing the different potentials and the capacitance measurement, it is possible to extract the Full Well Capacity for given experimental conditions by integrating the capacitance from the pinning potential to the equilibrium one (Fig.9). TCAD simulations are used in order to validate the Full Well Capacity extraction method. The different potentials are obtained by using Id(Vs) curves on the same simulated structure used to validate the equilibrium potential extraction (Fig.8). The capacitance extraction is performed on the drain of the same structure where the source is removed. On this last structure, a reference Full Well is also extracted directly by integration of the electrons stored in the photodiode of the structure. This exercise can be ran for example for different V_g applied on the transfer transistor gate which affects the Full Well Capacity. The result can be seen on Fig.10. The two Full Well Capacities are very closed which validate the methodology to extract this parameter on test structures and together the understanding on the equilibrium potentials that can be picked on Id(Vs) curves. This exercise has also been performed varying the luminous flux, the temperature, or the structure

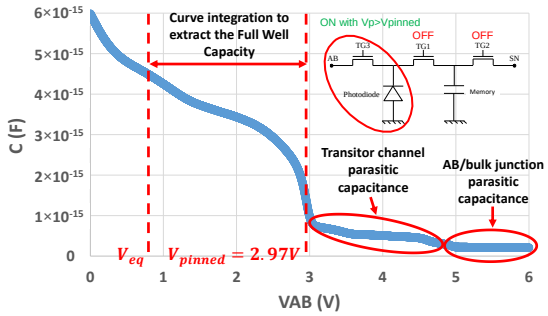

Fig. 9: Photodiode capacitance measurement with presence of parasitic capacitances which need to be removed.

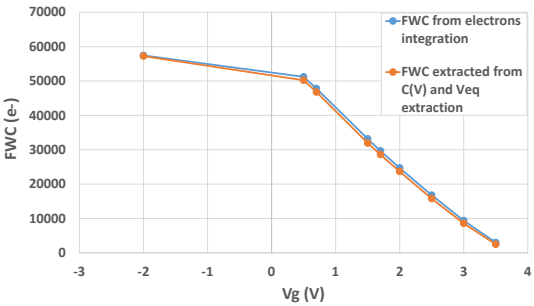

Fig. 10: Comparison of the Full Well Capacity extracted directly on the simulated structure in the dark and the one extracted on the simulated capacitance measurement.

geometry with also very good matching between extracted Full Well values.

V.CONCLUSION

A new method based on EKV model has been developed that enables to extract absolute potentials from test structures measurements. It can be applied to most pixel potentials, in particular under transfer gates or in pinned photodiodes. It is based on Id(Vs) curves. The subthreshold regions of these same curves also give possible photodiodes' equilibrium potentials, depending on experimental conditions. These potentials together with photodiode C(V) which can also be measured on test structures enable to retrieve the corresponding Full Well Capacities. All these approaches give fully consistent results that are also confirmed by simulations. These test structure level extractions have enabled to consolidate our understanding of the mechanisms involved in the Full Well Capacity. They can also enable to discriminate the capacitance and barrier contributions to this parameter. More generally, such test structure level extractions can be very helpful for mechanisms understanding, for pixel and technology developments, process monitoring, device level reliability studies or TCAD calibration, several of these being often more complicated at product level.

References:

[1] A. Pelamatti, V. Goiffon, A. De Ipanema Moreira, P. Magnan, C. Virmontois, O. Saint-Pé et M. Breart De Boisanger, «Comparison of pinning voltage estimation methods in pinned photodiode CMOS image sensors,» IEEE Journal of the Electron Devices Society, vol. 4, n° 12, pp. 99-108, 2016.

[2] J. Tan, B. Bernhard and J. P. Theuwissen, "Analyzing the Radiation Degradation of 4-Transistor Deep Submicron Technology CMOS Image Sensors," IEEE Sensors Journal, vol. 12, no. 16, pp. 2278-2286, 2012.

[3] X. Yang, G. Xiaoliang and A. J. Theuwissen, "Investigating transfer gate potential barrier by Feed-Forward effect measurement," in International image sensors workshop (IISW), Vaals, 2015.

[4] C. Doyen, S. Ricq, P. Fonteneau, O. Marcelot et P. Magnan, «CMOS pixel potentials extraction method from test structures based on EKV model,» IEEE Transactions on Electron Devices, vol.68, no. 6, pp. 2835-2840, 2021.

[5] C. C. Enz, F. Krummenacher et E. A. Vittoz, «An analytical MOS transistor model valid in all regions of operation and dedicated to low voltage and low current application,» Analog Integrated Circuits and Signal Processing, vol. 8, pp. 83-114, 1995.

[6] G. Ghibaudo, «New method for the extraction of MOSFET parameters,» IEEE Electron Letters, vol. 24, pp. 543-545, 1988.

[7] A. S. Sedra et K. C. Smith, Microelectronic Circuits 6th edition, Oxford University Press, 2009.

[8] A. Pelamatti, «Estimation and modeling of key design parameters of pinned photodiode CMOS image sensors for high temporal resolution applications», PhD, Toulouse, 2015.

[9] S. M. Sze, Physics of Semiconductor Devices, John Wiley and Sons, 1981.