A 1.3M Pixel 34,700fps Global-Shutter BSI Imager with HDR and Motion Blur Suppression Capability

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Introduction

High speed imaging sensors are an indispensable tool for capturing fast transient phenomena, with applications spanning a wide spectrum, such as scientific research, machine vision for the manufacturing and automotive fields etc. In this paper, we demonstrate a CMOS BSI imager featuring a 1280(H) x 1024(V) array of 10T global shutter (GS) & high dynamic range (HDR) pixels at a frame rate higher than 30,000fps with motion blur suppression capability.

Global shutter Pixel with HDR

The pixel as shown in Figure 1 has 5 NMOS transistors and 5 transfer gates (TG) among which 2 TGs, i.e., TG3A and TG3B, can biased at 3 different levels.

The operation principle for GS and HDR is explained by the timing diagram shown in Figure 2. For FRAME A, During the integration time TintA, TG3A is biased at at intermediate level so that when the amount of the integrated charges is larger than QFW of SN node, the extra charges will overflow to the capacitor CA. At the beginning of FRAME A readout, FD and the capacitor CB are reset, then TG1 is toggled to transfer charges from PPD to SN, then TG3A is toggled again in case not all charges are transferred to SN due to Vth variation of TG3A. TGF is the electronic shutter or “flush” gate to adjust the integration time. During FRAME A readout, TG3B can be biased at intermediate level as we did for FRAME A. To readout the pixel, first we sample the reset level ‘R1’ on FD, then toggle TG2, sample the signal level ‘S1’. The CDSed signal ‘R1-S1’ will be used as high gain (HG) signal, then MA is turned on to merge the charges on CA and FD. The merged signal ‘S2’ will be used as low gain (LG) signal.

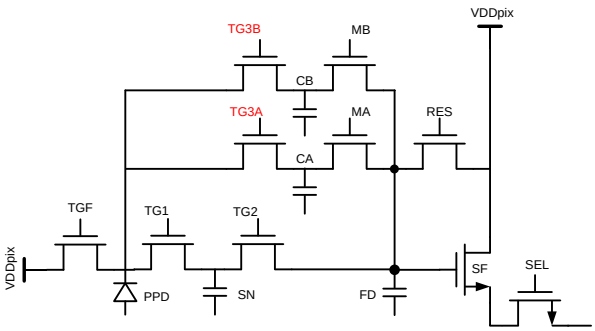

Figure 1 Global shutter pixel with HDR capability

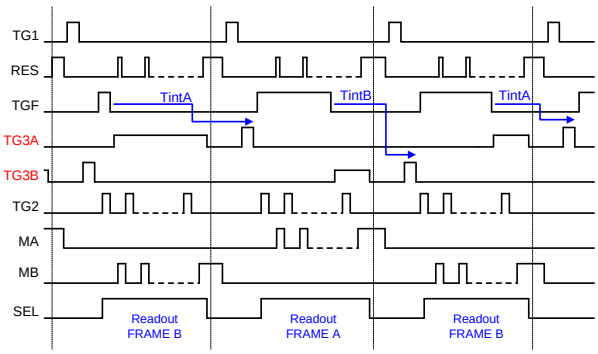

Figure 2 Timing diagram of pixel control

The advantages of this GS pixel are that it can select true CDS for low noise and HDR capability, the integration time can change from frame to frame which is necessary for “frame-to-frame intermittent tracking” method to suppress motion blur.

Sensor Architecture

The architecture of the imager is shown in Figure 3. The active pixel array is surrounded by black pixels. The pixel driver and Y scanner locate at both West and East sides of the array. At North and South sides, the readout circuits consist of column S&H stage and readout buffer, X scanner, single-to-differential (S2D) amplifier array whose gain is programmable ranging from 0.5 to 4, and output buffers. A symbolic pixel readout chain is shown in Figure 4. The column S&H stage and readout buffer are shown in Figure 5. The S&H can also provide column

gain by stacking the 4 sampling capacitors. The SPI, clock generators and other supporting circuits are at the four corners of the sensor. The array is split into 4 quadrants. Within each quadrant, every 8(H) x 16(V) pixels form a

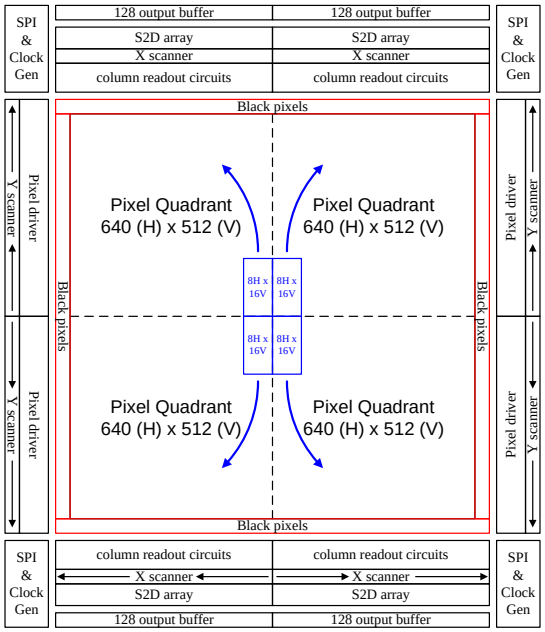

Figure 3 Architecture of the imager

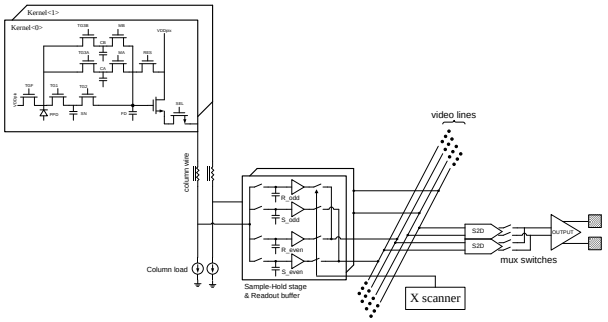

Figure 4 symbolic pixel readout chain

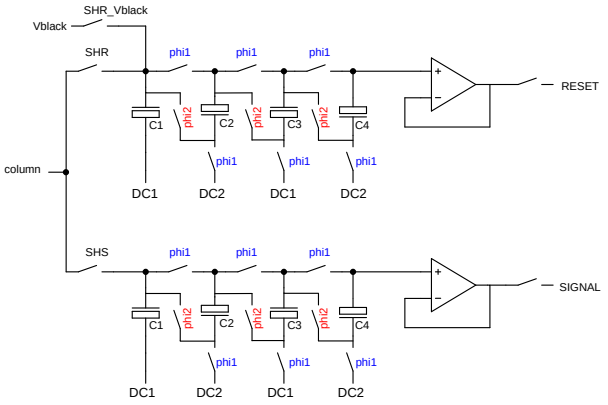

Figure 5 S&H stage and readout buffer

'kernel' and the signals from these pixels will be available at the 128 output buffers at the same time. Each output channel can run at 100Mpix/s. The readout starts from the center of the array.

Motion Blur Suppression

The sensor can use the "frame-to-frame intermittent tracking" method described in [5] to suppress the motion blur. The timing diagram to control the pixel with this technique is shown in Figure 6. To use this technique effectively, the integration time can vary significantly from frame to frame, and it may be much longer or much shorter than the frame readout time.

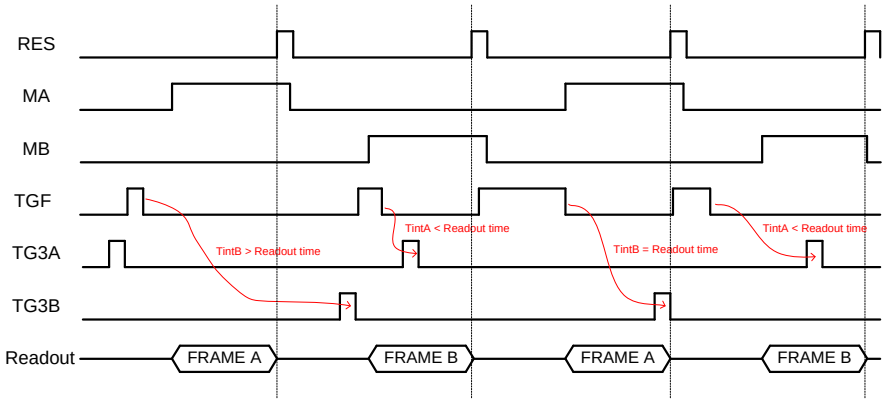

Figure 6 Timing diagram of pixel control with motion-blur-suppression technique

x4 Frame Rate

The sensor can use the 'KernelScan' method to increase the 'effective' frame rate without increasing the clock speed and overall pixel rate, in exchange of lower resolution. For every 2x2 pixel as shown in Figure 7, the start and stop of the integration times of pixels A, B, C, and D can be independently controlled as shown in Figure 8. In this way, the 'effective' frame rate is increased by a factor of 4 and the proposed motion blue suppression technique can also be used. Compared with prior arts in [3], alternating the positions of A, B, C, D pixels for every

2 rows can compensate the small shifts in positions between 2 consecutive images, and breaking the repetitivity can also reduce the Moiré effect.

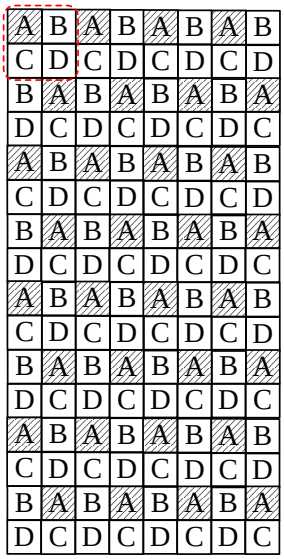

Figure 7 Pixel arrangement for 'KernelScan'

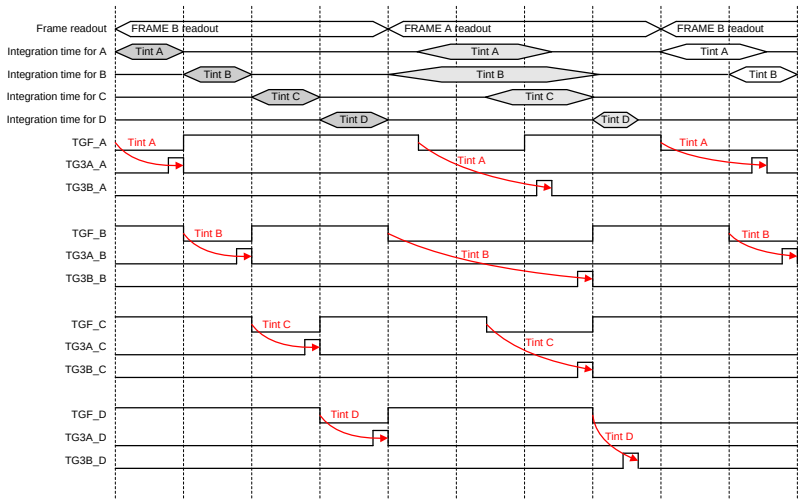

Figure 8 Timing diagram of pixel control for 'KernelScan'

Sensor Performance

The photo response of the sensor is shown in Figure 9. The QFW is 9.5ke- in HG mode, and 106.5ke- in LG mode. The noise histograms of both HG and LG are shown in Figure 10. The measured key performance parameters are listed in Table 1. A series of images are shown in the next page. The images are showing a steel stick drops and breaks a wine glass. The signal processing applied to these images are only dark frame correction and histogram equalization.

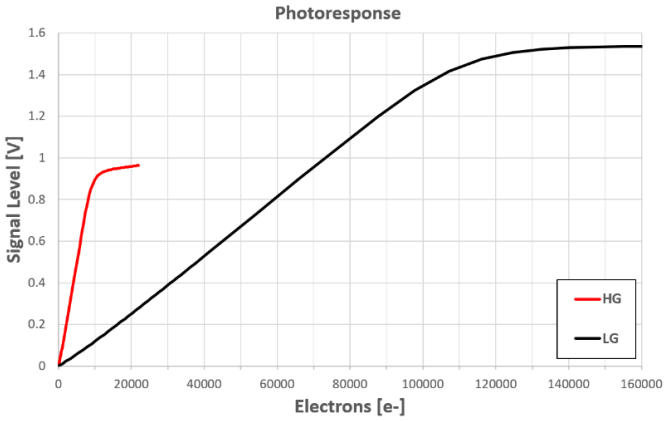

Figure 9 Photoresponse of the sensor

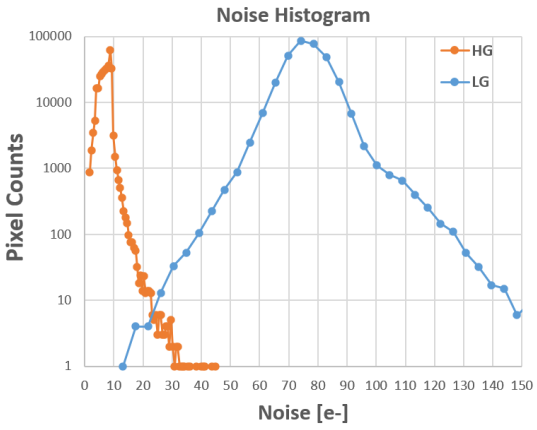

Figure 10 Noise histogram

Table 1 Measured key performance parameters of the sensor

Measured key performance parameters of the sensor	
Pixel array size	1280 x 1024
Pixel pitch	16µm
Frame rate (Full frame, HG only)	34,700fps
Frame rate of minimum ROI	2,000,000fps
Full well capacity (FD + CA/CB)	106.5ke-
Average Noise (CDS) @RT, S2D gain = 1	7.4e- RMS
Image lag @50% FW	< 1%
Linearity (0~90% FW)	< 1%
Power consumption	16.5W

Acknowledgement

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