SPAD based Time of Flight Pixel Circuits for Large Scale Arrays

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***Abstract*—Large-scale 3D time of flight sensors face several challenges: high power consumption, large pixel pitch, mostly single-bin operation and/or a low count depth where multi-bin pixels are implemented. This paper presents a 2-bin and 4-bin SPAD pixel circuit with a 7 – 10 ENOB full well capacity and < 20 nW/MHz power consumption, at pixel pitches of 4.8 µm and 7.1 µm respectively.**

I. Introduction

Time of flight (TOF) sensor arrays of up to 1 MP have been designed with various detector elements, such as fast photodiodes / photogates, CAPD (current-assisted photodiode) and SPAD (single photon avalanche diode). The main challenge for all remain their high power consumption, but also fitting the counting electronics underneath the detector element to allow for a modern 3D stacked chip design. Proposed techniques to combat high power consumption such as peak current spreading to minimise peak power consumption in [1], [2] and turning off SPADs after a pixel full-well has been reached [3] have been presented in literature. However, to achieve large scale arrays using SPADs the power consumption of the pixel circuitry and its size needs to be aggressively reduced in tandem with SPAD pitch. Existing SPAD based sensors still incur large pixel pitches, mostly single-bin operation and low count depths for multi-bin operation. Furthermore, aggressive use of voltage and technology scaling has recently brought SPAD detector pitches down to 6 – 7 µm [3], which has the benefit of reduced detector power due to lower avalanche currents, but also means pixel circuits must shrink to match these pitches. The challenge is to achieve this without compromising pixel performance.

We present two SPAD and analogue counter based TOF pixel circuits fabricated in STMicroelectronics' 40 nm FSI process with all pixel designs being 3D-stacking ready: a 2-bin pixel at 4.8µm pitch and a 4-bin pixel at 7.1µm pitch. Various power saving strategies are exploited in the pixel designs such as using a dynamic comparator [4] or LVDS (low voltage differential signaling) latch front-end allowing low swing clock distribution (full swing CMOS level is reconstructed in-pixel) as well as utilizing a CTA analogue counter [5-9] as a small area, low power photon counter. Together these building blocks result in pixels allowing multi-bin operation at a high full-well capacity (FWC), low power consumption and pixel pitches capable of matching today's small SPAD detectors. The multi-bit operation reduces the readout data rate by a factor of 2^{FWC} compared to single-bit pixels and contrary to digital pixel designs the pixel pitches achieved by using analogue pixels mean large-scale sensors up to 1 MP become feasible. In addition, the LVDS clocking scheme in combination with a fast comparator and SPAD edge time result in an estimated demodulation contrast comparable to photodiode-based pixels.

II. Test Chip Overview

A test chip of 3x3 pixel matrices of both pixel types was manufactured in ST's 40nm FSI process. Both pixels consist of one or two LVDS latches and two or four CTA counter bins and also include a SPAD front-end quench transistor and inverter chain.

A. Pixel Building Blocks

An LVDS latch is employed as a SPAD event-driven pixel front end in place of a traditional flip-flop. Referring to Fig. 1 (a) and (b), it resolves a pair of LVDS clock signals PHI and PHIB into full swing outputs VA and VB on the rising edge of every SPAD pulse. Two types of LVDS latches are investigated: Fig. 1 (a) a 4T stacked and (b) a 3T stacked latch. The 4T stacked latch is an adapted version of the conventional strong-arm latch structure and operates as follows: the LVDS clocks swing 200 mV_{p-p} around a common mode voltage V_{CM} to keep the input pair biased around their threshold voltage. When no SPAD event is present the latch is in the reset state and the nodes VA' and VB' are reset high through transistors M8 and M9. When a SPAD event occurs, if PHI is higher than PHIB, then the difference in V_{GS} of the input pair results in node VA' discharging faster than VB' and positive feedback via the inverters M3/M4 and M5/M6 causes the outputs to move to opposite states; in this case VA' = VSS and VB' = VDD. By inverting the signals the latch provides active high, two-bin time binning for the CTA counters. The 3T stacked latch in Fig. 1(b) on the other hand is proposed to allow lower VDD operation by removing the latch turn-off transistor M7 in Fig. 1(a) from the stack. The functionality is instead moved to the input pair of the 3T latch by including switches M7 – M10 in Fig. 1(b). The 3T latch operation remains the same, but switches M9 and M10 now keep the input pair gate voltage at VSS when no SPAD event is present, and releases the pulldown and activates the clock sampling switches M7 and M8 when a SPAD event occurs. Removing one transistor from the stack allows the 3T stacked latch to operate at supply voltages as low as 0.6 V (simulated results) further reducing its power consumption.

After a SPAD event has been resolved by the LVDS latch it is counted by the CTA analogue counter structure shown in Fig. 2. The counter consists of the three transistors M0 – M2 and capacitors C_{int} (MOM + MOS) and C_p (parasitic), and a source follower and read switch (M3 and M4) are added for readout. The counter

operation is as follows: first the capacitor C_{int} is reset to V_{cap} = VRT by pulsing V_{rst} low. We implement a PMOS reset transistor for the pixels to a) provide a hard-reset of the pixel and b) place the transistor into cut-off during integration by including a separate bulk connection to bias the reset supply VRT lower than the bulk voltage VRTB during integration. Second, a time resolved SPAD event pulses the counter input V_{in}, starting a charge transfer from C_{int} to C_p lasting until transistor M1 is pushed into the cutoff region by the rising source voltage. Thus, a constant amount of charge is transferred from C_{int} to C_p for every SPAD event, causing the voltage V_{cap} to reduce by a step $\Delta V \approx C_p/C_{int}(V_{in}-V_{th}-V_s)$. The dependency of the step size on V_s gives bias voltage control of the desired full well capacity (FWC) and step size. Finally, the tail transistor M2 will discharge the parasitic node C_p and prepare the counter for the next SPAD event.

B. Pixel Test Structures

Combining one LVDS latch with two CTA counters provides a 2-bin pixel as shown in Fig. 3 and combining two latches with four CTA counters and a 4-to-1 one-hot decoder achieves 4-bin operation as shown in Fig. 4. Both pixels also contain an inverter chain and quench transistor as a SPAD front-end. To test the pixels in an imaging array environment all test structures have been built as a 3x3 pixel matrix (layouts shown in Fig. 10 on the last page), where the pixel under test sits in the middle while the surrounding pixels are biased but inactive. A timing diagram showing the counting operation of the 4-bin pixel is shown in Fig. 5 where four SPAD events are counted into four time bins.

The first power saving feature of these pixels is a result of the LVDS latches operating on a pair of low-swing LVDS clocks instead of full-swing CMOS clocks. The clock distribution power scales with the square of the clock voltage and can roughly modelled as $P_{CLK} = fCV^2$; comparing 200 mV LVDS clocks to full-swing CMOS clocks at 3.3 V, this can result in a dynamic power saving of a factor of 136 (e.g. 3.3^2 V / $2*0.2^2$ V). The second power saving feature is the inherently low power CTA counter that consumes its peak power during the reset of its ~ 20 fF integration capacitor, which is negligible compared to the LVDS latch power. The LVDS clocks distributed to the pixels are a pair of 180 degrees offset clocks for the 2-bin pixel, and two pairs of LVDS clocks phase offset by 90 degrees for the 4-bin pixel (see Fig. 5).

III. Results

The measurement platform and test equipment used to characterize the pixels is shown in Fig. 6. The setup consists of an FPGA, a generic supporting PCB with voltage regulators and a chip socket, an oscilloscope, a source meter and a delay generator. The test procedures were automated using Python scripts to enable large data collection. It should be noted that due to the test platform used and the pixel column voltage being measured off-chip, the read noise across the measurements is relatively high at ~ 2 mV. An on-chip ADC is expected to improve this limitation in the future. A comparison with the state of the art is presented in Table 1 and a summary of the measurement results for this work in Table 2.

A. Counting Results

Both pixels achieve a 7 – 10 bit FWC with counter step sizes of 13.7 mV and 1.9 mV respectively. Fig. 7 shows the results from both the 2-bin and 4-bin pixel characterisations where, in order from left to right, the plots show: the counting histograms of the first and last ten counts, the step size across the measurement range, the full scale range, and finally the INL and DNL. For the 7-bit FWC, the histogram peaks are well separated and the counting is shot noise limited, while for the 10-bit FW the read noise dominates and merges the histograms. A linear FWC is achieved for both pixels, with the 2-bin pixel having a DNL range of as low as ± 0.2 LSB and ± 4.4 LSB at 7-bit and 10-bit FWC respectively.

B. Timing Results

A timing characterisation of the counting performance across a clock transition edge for the 2-bin pixel with both the 4T and 3T stacked latches was performed. The measurement was made using a delay generator to provide a clock transition and electrical SPAD trigger pulse to the pixel 100 times for each time delay step with a 5 ps resolution. The output voltage of each bin was then measured and plotted against the trigger delay and the results are shown in Fig. 8. The transition time between the two time bins is 62 – 109 ps showing the potential of the pixels to achieve a demodulation contrast of > 93% @ 300 MHz modulation frequency (bin width = 1.67 ns).

C. Power Measurements and 1MP Projection

The power consumption of the 4T and 3T stacked latches together with the SPAD front end were measured for power supply voltages between 1.2 V – 0.9 V and the results are plotted in Fig. 9. The power consumption across the measured range is 8.6 – 19.3 nW/MHz. While the 3T stacked latch has a slightly higher power consumption than the 4T stacked latch due to the removal of the tail transistor M7 from the stack, the latch power dominates the overall pixel power consumption in both cases as the CTA power is negligible in comparison (i.e. resetting the CTA 20 fF integration capacitor from 0 V to 2.9 V at 30 fps consumes ~ 12 pW for the 2-bin pixel, compared to ~ 10 nW/MHz for the latch). Hence, assuming a frame rate of 30 fps and an integration duty cycle of 33%, the projected power consumption of a 1 MP array becomes 2.8 – 6.4 mW/MHz for the 2-bin pixel and 5.6 – 12.8 mW/MHz for the 4-bin pixel.

IV. Conclusion

This paper presents a 2- and 4-bin pixel design which address the challenges faced by large-scale 3D TOF arrays, namely: small pixel pitch, low power consumption, high bit-depth and multi-bin counting. To the best of the author's knowledge the per pixel power consumptions together with pixel pitches of 4.8 μm and 7.1 μm are the smallest achieved for SPAD based ITOF pixels to date. This work shows the potential of SPAD based sensors to compete in the same space as modulated-photodiode and CAPD based sensors.

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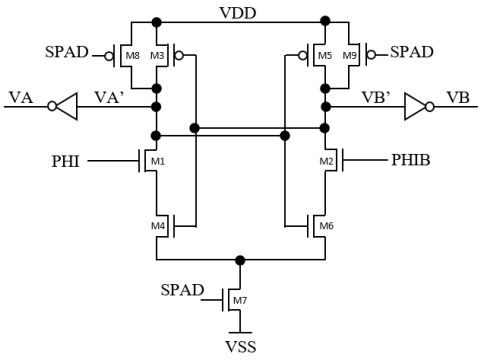


Figure 1 (a): LVDS latch 4T stacked schematic

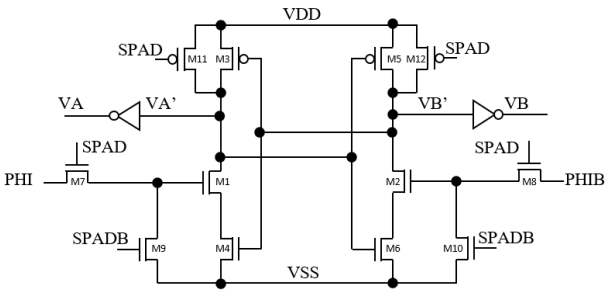


Figure 1 (b): LVDS latch 3T stacked schematic

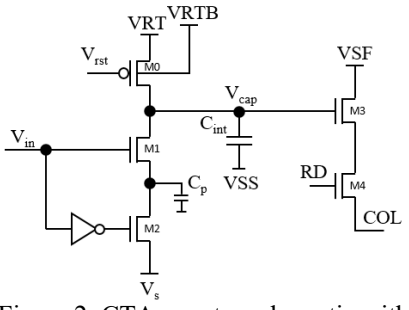


Figure 2: CTA counter schematic with source follower and read switch.

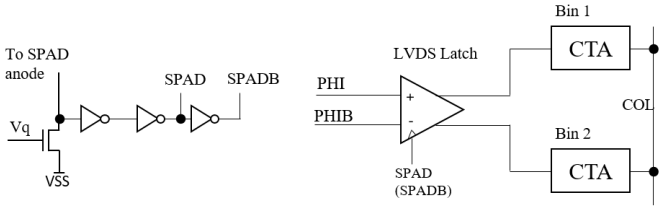


Figure 3: Schematic of 2-bin pixel including SPAD front-end.

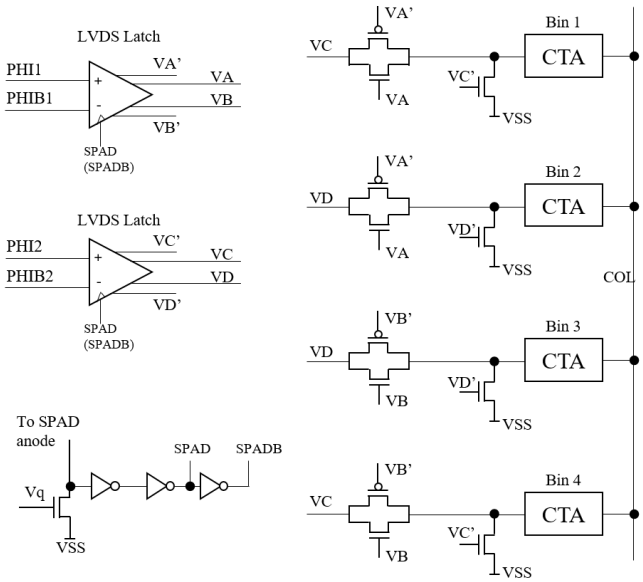


Figure 4: Schematic of 4-bin pixel including SPAD front-end.

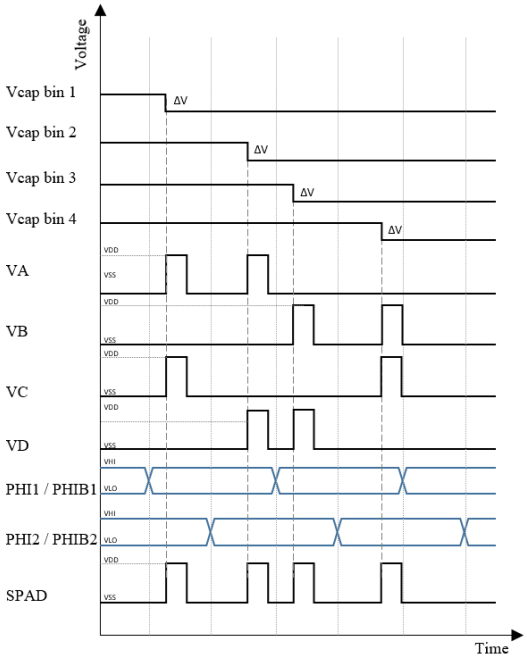
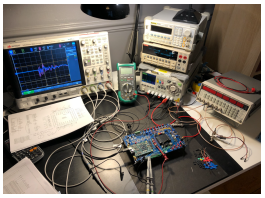


Figure 5: Timing diagram of 4-bin pixel.



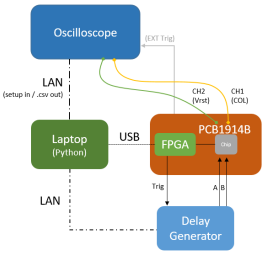


Figure 6: Measurement setup and block diagram of test control and automation

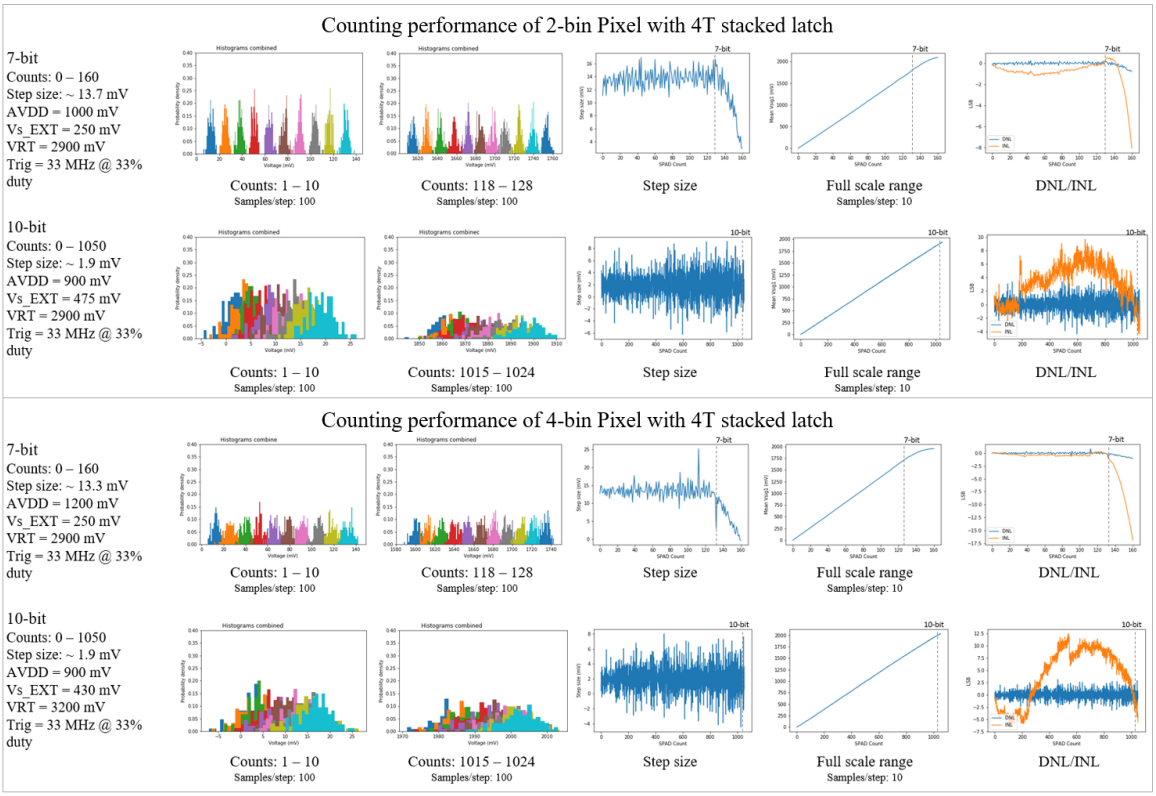


Figure 7: 7- and 10-bit counting performance of the 2- and 4-bin pixels with a 4T stacked latch.

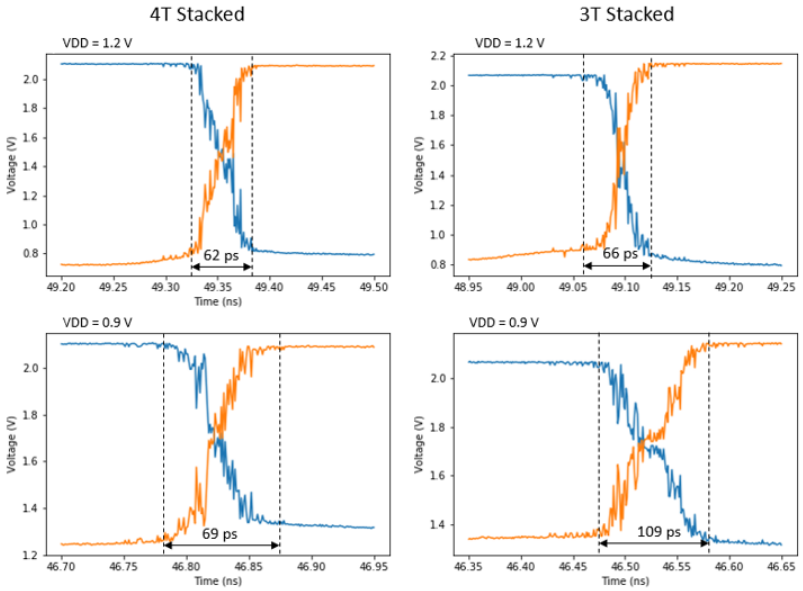


Figure 8: Time bin characterization of the 2-bin pixel with 4T and 3T stacked latch respectively (LVDS diff = 200mV$_{p\text{-}p}$, VHI/VLO = 600mV/400mV, y-axis = SF Vout after integration of 100 steps)

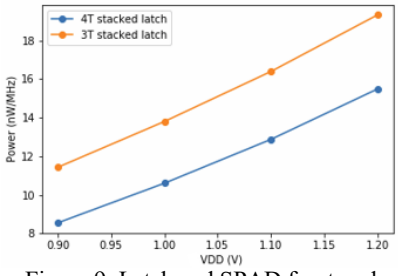


Figure 9: Latch and SPAD front-end power consumption vs. VDD.

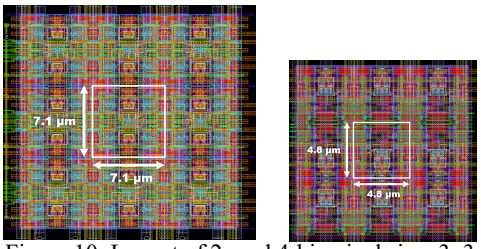


Figure 10: Layout of 2- and 4-bin pixels in a 3x3 matrix (SPAD is placed to the side in this work).

Comparison of state of the art TOF imagers

	This work SPAD	[12] JSSC 2021 SPAD	[3] ISSCC 2021 SPAD	[10] Optica 2020 SPAD	[7] JSSC 2016 SPAD	[1] ISSCC 2018 PD	[2] ISSCC 2021 PD	[11] VLSI 2017 CAPD
Technology	40 nm	110 nm	Stacked 90 nm / 40 nm	180 nm	350 nm HV CMOS	65 nm	Stacked 65 nm / 65 nm	90 nm BSI
Pixel pitch	4.8 µm (2-bin) 7.1 µm (4-bin)	32 µm	12.24 µm	9.4 µm	15 µm	3.5 µm	3.5 µm	10 µm
Number of bins	2 / 4	2	1	1	1	2	4	2
Count depth	7 – 10 bit	9 – bit	9 – bit	1 – bit	5.4 – bit	-	-	-
Resolution	3x3 test structures	64 x 64	160 x 264	1024 x 1000 (1 MP)	160 x 120	1024 x 1024 (1 MP)	1280 x 960 (1.2 MP)	320 x 240 (QVGA)
Modulation frequency	1 – 100 MHz	1.56 – 50 MHz	-	-	-	10 – 320 MHz	10 – 200 MHz	100 MHz
Demodulation contrast	> 93 % @300 MHz (estimated)	-	-	-	-	87 % @200MHz 78 % @300MHz	96 % @100MHz 80 % @200MHz	91 % @ 50 MHz 85 % @100 MHz
Chip power (This work = per MHz SPAD rate)	2.8 mW/MHz (for 1 MP, 2-bin) 5.6 mW/MHz (for 1MP, 4-bin)	42.7 mW (2-bin)	-	535 mW / 284 mW	157 mW / 20.6 mW	650 mW / 150 mW	290 mW (full) 220 mW (2xbin)	-
Frame rate	30 fps	65 fps	60 – 250 fps	24,000 fps (1b)	486 fps	30 fps	60 fps	-

Table 1: Comparison of state of the art TOF imagers.

Pixel Type	**2-bin ITOF**		**4-bin ITOF**	
Bit depth	7-bit	10-bit	7-bit	10-bit
Area / bit (µm2)	1.65	1.15	1.80	1.26
Linear full well (steps)*	140	1050	132	1050
ENOB	7.1	10.0	7.0	10.0
Average step size (mV)	13.7	1.86	13.6	1.94
DNL (Step = LSB)	+0.2/-0.2	+3.9/-4.4	+0.9/-0.4	+3.1/-3.1
INL (Step = LSB)	+0.1/-1.1	9.7/-2.6	+0.3/-0.7	+12.4/-6.5
Read noise (mV)	1.9	1.9	2.6	2.6
Input referred noise (Step = e- equiv.)	0.1	1	0.2	1.3
Per pixel power (nW/MHz)	8.6 – 19.3		17.1 – 38.6	
Predicted 1 MP array power (mW/MHz)	2.8 – 6.4		5.6 – 12.8	

*Linear full well where average DNL < 0

Table 2: Pixel performance summary