A Novel Ultra-High-Speed CMOS Image Sensor Implementation with Variable Spatial and Temporal Resolution using Temporal Pixel Multiplexing

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I. INTRODUCTION

In this paper, we present the first silicon implementation of a CMOS image sensor employing the imaging technique known as temporal pixel multiplexing (TPM). This TPM sensor implementation was primarily developed for optical microscopy applications to enhance spatial and temporal resolutions by obviating the use of DMD[1] mirror technology. It has enabled simultaneous high-speed imaging of cellular activity and high spatial resolution imaging of anatomical structure in the field of light microscopy. However, the scope of the TPM method can be expanded to a broad variety of short time domain studies that involve the visible light spectrum. Examples include but are not limited to life science, materials science, nanotechnology, etc. Here we provide details of the TPM sensor architecture, describe its functionality, present initial test results and explain benefits of the application of the TPM technique. The TPM device is shown in Figure 1.

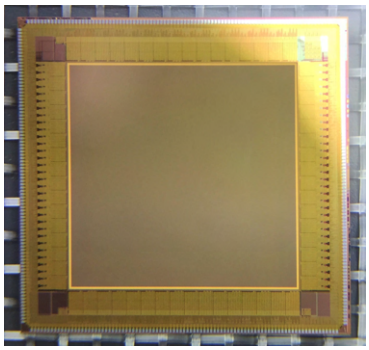


Figure 1: The TPM sensor

II. TPM CONCEPT

TPM[1][2] is a new imaging paradigm allowing all pixels in the array to have either the same integration time (leading to a single high resolution still image), or for adjacent pixels to have staggered integration times (leading to multiple lower resolution still images). Based on the desired trade-off between the number of frames in a high-speed burst and the video resolution, the sensor splits the pixel array into multi-pixel sub-groups defined prior to image capture.

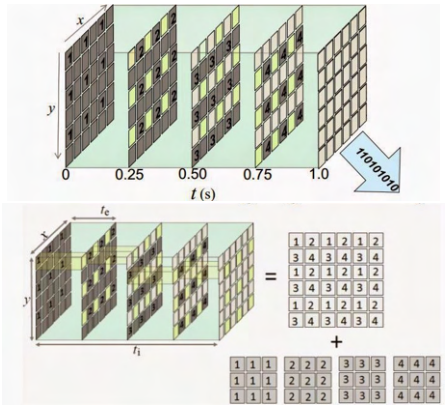


Figure 2: TPM sensor operation with a 2x2 mask

The example shown in Figure 2 demonstrates the TPM operation with a sub-group size of 2 x 2. The resulting output is a single high-resolution image that can be post-processed into a short movie, formed from an ultra-high-speed sequence of lower resolution frames, consisting of pixels which have been exposed at the same time and collected together. In this particular example, the sequence will comprise 4 frames at the resolution of 3 x 3 from the single array.

III. TPM SENSOR

The sensor was designed in a 180 nm, dual oxide, 5 metal, 1 poly CMOS Image Sensor process technology. A single device measures 14.5 mm x 14.5 mm with an imaging area of 10 mm x 10 mm. The sensor has a resolution of 1024 x 1024 pixels, out of which 1000 x 1000 are active, with a pitch of 10 μm. It is read out through 32 analogue amplifiers working at 300 fps.

[1]Digital Micromirror Device.

The TPM pixel is based on a 3T-APS[2] architecture with a partially pinned photodiode (PPPD). The pixel contains 8 transistors and a capacitor used to hold the signal level until it is directed through the analogue readout chain; refer to Figure 3.

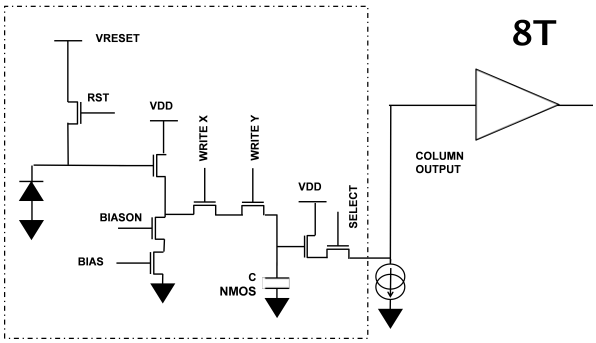


Figure 3: TPM pixel schematic

The pixel has two internal source-followers and two switches that run on the x- and y-axes to implement a pre-specified pattern for TPM exposures. The 1st in-pixel source-follower, which has a BIAS and a BIASON transistors inside the pixel, is used to drive the pixel output voltage through WRITEX and WRITEY control switches onto the internal storage node. Although it means the current is used within the pixel, this bias current can be reduced if the sensor is not operated at the specification frequency. Alternatively, the bias can be turned off via the BIASON transistor for all unexposed pixels. The 2nd in-pixel source-follower is utilised to buffer the voltage across the storage capacitor onto the column readout line.

Due to the TPM operation, the digital system of this sensor is relatively complex. The digital signals required by the TPM pixel are RST, BIASON, WRITEX, WRITEY and SELECT. In order to reduce the load of the line which increases the rise and fall time of each signal, the control signals are split in the middle of the pixel array and driven from both sides. The SELECT signal is controlled by a 10-bit counter placed on the left and right side of the chip, the RST and WRITEX signals - by two separate 1024-bit shift registers placed on the left and right side of the chip, and the BIASON and WRITEY signals - by two separate 1024-bit shift registers placed on the top and bottom side of the chip. The TPM sensor floorplan showing the pixel array and supporting blocks around it is shown in Figure 4.

The readout of the TPM sensor was implemented in the analogue domain, which contains 32 output channels controlled by a 5-bit counter. Half of the pixel columns are read out off the chip at the top and half - at the bottom, resulting in 512 pixel outputs being multiplexed to 16 readout lines per side. The counter performs the decoding which allows each pixel column to access the correct readout channel.

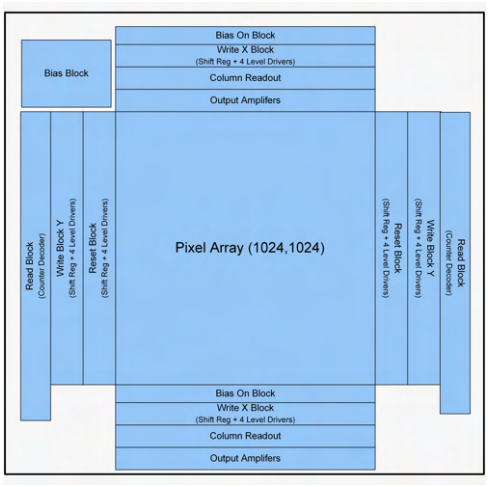


Figure 4: TPM sensor floorplan showing the pixel array and supporting blocks around it

The biasing block, placed in the top left corner of the chip, is used to generate on-chip currents and voltages from a single reference current. It has a digital part which allows the biases to be easily calibrated due to the use of programmable DACs[3]. They comprise a primary DAC and several secondary DACs, each of which (including the primary one) is controlled via a 6-bit shift register. This allows each bias current to be adjusted independently within a 6-bit resolution.

The current TPM sensor design provides a high degree of flexibility in setting the size of multi-pixel sub-groups used to implement temporal pixel multiplexing. In this paper, the example of a 4 x 4 sub-group, which results in 16 frames at the resolution of 256 x 256, will be discussed. Due to the amount of signals which need to be generated, only the inputs to the pixels are shown in the block diagram in Figure 5. Here the pattern clocked through BIASON, WRITEX and WRITEY shift registers should be 1000, whereas the pattern for the RST shift register should be 0111. During the sensor operation, the same pattern should be clocked in continually until every pixel within the TPM mask will have been exposed. The clock frequency for each shift register should be chosen carefully as it will set the reset and integration time for each sub-group of pixels (the maximum clock frequency is 10 MHz which is equivalent to the integration time of 100 ns). Furthermore, the clock frequency for the WRITEX and BIASON shift registers should be 4 times lower than that

[2]Active Pixel Sensor.
[3]Digital-to-Analogue Converters.

for the WRITEY and RST shift registers in order to follow through a 4 x 4 TPM mask correctly. The 4 x 4 TPM mask can be implemented within 16 clock cycles in the manner shown in Figure 6:

- In the 1st clock cycle, the output of all pixel 0s is transferred onto the in-pixel storage node while pixels 4, 8 and 12 integrate but are not written in the pixel memory, and the remaining pixels are kept in reset;
- In the 2nd clock cycle, the output of all pixel 1s is transferred onto the in-pixel storage node while pixels 5, 9 and 13 integrate but are not written in the pixel memory, and the remaining pixels are kept in reset;
- etc.

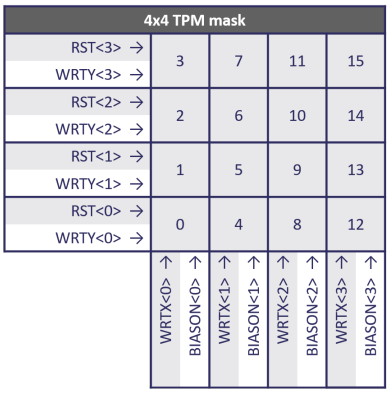


Figure 5: Example of 4x4 TPM mask control

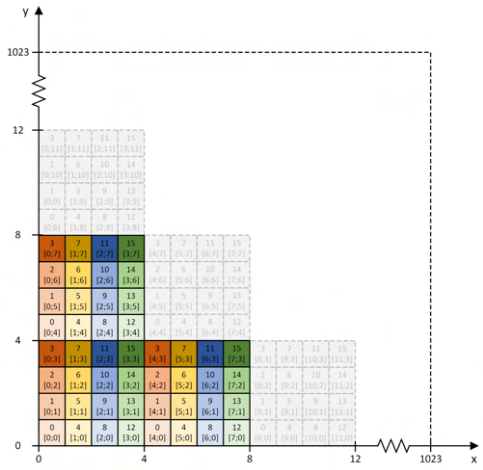


Figure 6: Example of 4x4 TPM mask operation

Having exposed all the pixels within the 4 x 4 mask, the data can be successfully read out off the chip. The resulting output will be a single full resolution (1024 x 1024) image formed from 16 lower resolution (256 x 256) frames, consisting of pixels which have been exposed at the same time and collected together. For instance, as can be seen from Figure 6, all pixel 0s would be assembled into "Frame 0", all pixel 1s - into "Frame 1", etc. These frames can then be post-processed into a short ultra-high-speed movie.

This TPM sensor architecture enables the user to change the TPM mask quite easily by the means of reconfiguring shift registers. If needed, the sensor can even be programmed to be operated in more conventional modes, such as rolling shutter or global shutter.

IV. INITIAL TEST RESULTS

The first results from the TPM sensor testing are presented in this section. The tests were carried out with three slightly different TPM sensor chip implementations, which contain:

1. MOSCAP in-pixel capacitors and 5 μm epi-layer;
2. VIACAP in-pixel capacitors and 5 μm epi-layer;
3. VIACAP in-pixel capacitors and 18 μm epi-layer.

As mentioned in the previous section, the senor can be operated in rolling shutter and global shutter modes in addition to its intended TPM functionality. In this paper, we present results from the characterisation of the device in a rolling shutter mode, in which WRITEX, WRITEY and BIASON switches are always closed and the sensor is effectively operated in the same way as the 3T-APS with a single integration time. The sensor has been characterised using the PTC[4] method, and the resulting PTC plots are shown in Figure 7.

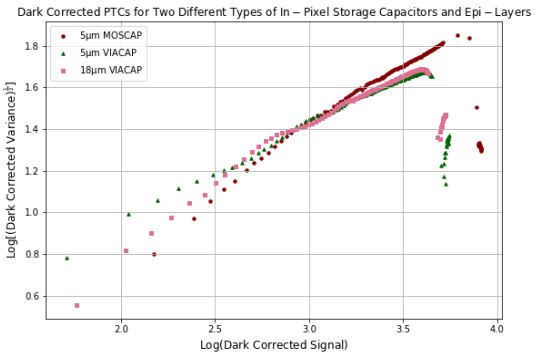
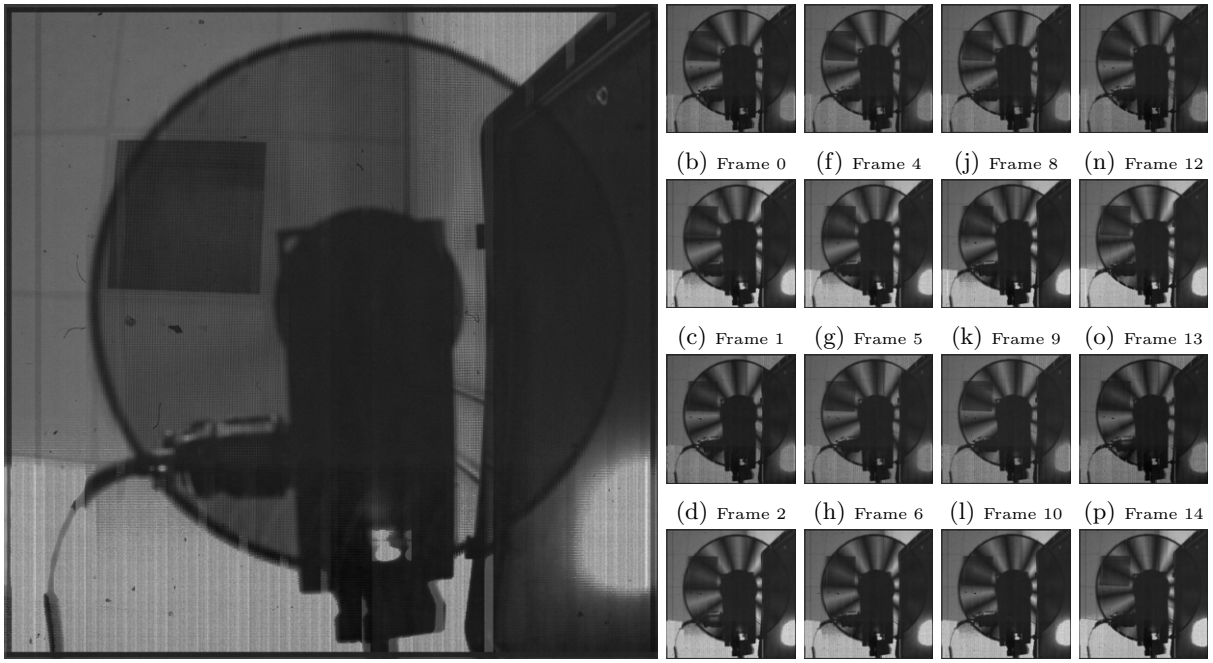


Figure 7: PTCs taken at 1 Mfps from the TPM sensor with MOSCAPs on low-res epi-layer and VIACAPs on both low-res and high-res epi-layers

The TPM functionality was confirmed when the image of the moving chopper was acquired with the TPM sensor using a 4 x 4 mask. During this test, pixels were reordered and grouped into 16 frames from a single picture, which allowed to create a short movie showing the spinning chopper. The resulting images are presented in Figure 8.

[4]Photon Transfer Curve.



(a) Dark-corrected image

(b) Frame 0 (f) Frame 4 (j) Frame 8 (n) Frame 12

(c) Frame 1 (g) Frame 5 (k) Frame 9 (o) Frame 13

(d) Frame 2 (h) Frame 6 (l) Frame 10 (p) Frame 14

(e) Frame 3 (i) Frame 7 (m) Frame 11 (q) Frame 15

Figure 8: The test image of a moving chopper taken with the TPM sensor using 4x4 mask. The integration/write time used was 10 ms with the offset of 10 ms between each sample. The frame rate of this example is well below the full capability of the sensor due to the use of ambient lightning and a relatively low-speed object (46 Hz). a) TPM image after dark frame subtraction; b-q) 16 frames deconstructed from a) and used to make a short movie.

V. CONCLUSIONS

This work demonstrates the TPM concept successfully implemented in a CMOS technology. The TPM sensor presented in this paper features:

- **High resolution:** up to 1K x 1K
- **Very high framing rate:** up to 10 million fps
- **Configurable number of frames**
- **Analogue readout**

For full sensor specifications refer to Table 1. This TPM sensor implementation highly benefits from the capability to retrieve both a high-resolution image and a high-speed image sequence from a single picture without increasing readout noise and bandwidth requirements. Additionally, the utilisation of shift registers makes the TPM sensor easily programmable by a user.

Parameter	Specifications
Pixel type	8T with PPPD
Floating diffusion capacitance	5.6 fF
Conversion gain	17 μV/e-
Maximum full-well capacity	~52.5 ke-
Fill factor	~53%
Pixel unit size	10 μm x 10 μm
Pixel array format	1024 x 1024
Effective pixel array format	1000 x 1000
Sensitive area	10 mm x 10 mm
Minimum integration time	100 ns @ 10 MHz (TPM)
Maximum output voltage swing	1 V
Maximum readout speed	10 MS/s
Readout frame rate	300 fps

Table 1: TPM sensor specifications

VI. REFERENCES

[1] G. Bub, et al., Temporal pixel multiplexing for simultaneous high-speed, high-resolution imaging, *Nature Methods*, 7, 209-211, 2010.

[2] G. Bub, N. Nebeker, and R. Light, New Approaches for High-Speed, High-Resolution Imaging, *Novel Advances in Microsystems Technologies and Their Applications*, 1st Edition, 149-167, 2017.