Charge Level Control with a Capacitive Trench for Imaging Devices

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***Abstract*—**This paper demonstrates the use of capacitive trenches in image sensors for charge level control via electron–hole recombination. The method was implemented and demonstrated on a capacitive trench-based charge transfer device and it is shown that one full well charge (80 000e-) can be removed in about 8µs. The influence of operating conditions on the efficiency of the method is presented.

I. Introduction

Capacitive Deep Trench Isolation (CDTI) trenches are now used in many imaging devices for cross-talk and dark current reduction [1] but also charge storage and/or transfer via electrostatic potential management [2,3,4,5]. In this work, the use of Capacitive Trench for pixel charge level control in image sensors is demonstrated. Indeed, for applications where charge storage is involved, it is shown that these CDTI trenches can also be advantageously used as electron-hole recombination gates in order to control the effective in-pixel charge level, thus replacing a reset transistor or as a dedicated anti-blooming device. The physical principle, which relies on the well-known charge pumping technique mechanisms [6], has already been used in planar MOS gates Charge Coupled Devices (CCDs) to implement an anti-blooming function [7]. Here a CDTI trench-based charge transfer register [5] is used for implementing and validating the charge recombination mechanism via a proper driving of the available CDTI trenches.

II. Charge pumping with a MOS trench

To recombine carriers, the charge pumping technique makes use of the interface traps located at the $Si\text{-}SiO_2$ interface of a MOS gate. The technique can be used with a vertical MOS trench (CDTI) since the physical mechanisms involved are the same. By going from strong inversion to accumulation and inversely, a MOS trench that has access to an electron and a hole source will alternatively build-up a surface population of electrons or holes. The carriers accumulated at the interface will interact freely with any surface defect present here and some of the accumulated charges will be trapped. The Fig. 1 presents an energy band diagram for a n-type MOS trench structure in strong inversion and accumulation regime. In each case, traps below the Fermi level are filled by electrons and those above by holes. When transitioning from one regime to the other, the surface charge layer will flow back to either the electron or hole source. Trapped charges on the other hand will be emitted with a certain time constant dependent on temperature and trap energy level in the bandgap. If the transition is quick enough, some charges will not be released before the build-up of the opposite carrier type at the trench's surface. The electron-hole recombination process is then assisted by the traps and its probability greatly enhanced. Thus, by alternatively pulsing the MOS trench rapidly enough to the appropriate voltages, a current is created via the trap assisted electron–hole recombination process.

III. Application of the method in a imaging device

The charge pumping technique being still applicable for a finite reservoir of electrons generated by light such as in image sensors, a CDTI trench was used as a recombination gate in a 2 phase, capacitive trench based, charge transfer device [5] to test the proposed method. In this register, electrons are not stored and transferred at the surface of planar MOS gates but in the silicon volume in between CDTI trenches. The Fig. 2 presents a planar and cross section schematic view of the structure. The shape of the electrostatic potential well in between two facing MOS trenches, represented Fig. 3, makes that electrons transferred to or generated in the well will be stored in between the trenches and kept distant from the trenches interfaces (up to a certain filling level). The electrostatic potential in between two trenches is directly proportional to the bias of the CDTI gates and to the square of their spacing. Vertically, a p+ pinning implant and the bottom p epi silicon fully close the storage well that is 2µm deep. The aspect ratio of the designed phases being high, the electrostatic potential is imposed primarily by the so called "CDTI storage gates". Charges are transferred from one phase to the next, in a CCD manner, by applying successively high and low voltages to the CDTI storage gates, simultaneously to the CDTI barrier gates that act as phases separation. In storage and light integration mode, the CDTI gates are biased to a lower bias than the grounded bulk and the trenches sidewalls are populated by a hole layer. To test the proposed charge level control method, the CDTI barrier gates are used as recombination gates and clocked independently to the appropriate voltages during a storage period. By increasing the CDTI recombination gates bias, the electrons go from being stored away from the trenches sidewalls, to being pulled towards it and are hence subject to trapping by interface states. By then lowering the CDTI recombination gates bias again, the non-trapped electrons flow back to the original charge packet and a hole layer re-forms at the gate's surface. Charges can then easily recombine via the principle exposed in section II, the hole source being the p+ pinning layer as well as the p epi silicon. The Fig. 4 presents a TCAD, planar electrostatic potential map (at 1µm depth) of a fully depleted 12µm pixel (1 pixel = 2

phases) in storage mode and with recombination gates at a high (3V) bias. It is clearly apparent that for a sufficiently high voltage, the electrostatic potential gradient will pull any stored electrons to the CDTI recombination gates surface. The CDTI recombination gates are thus switched back and forth between a high and a low level at a fixed frequency and with controlled rising / falling edges times to gradually empty the charge well. The CDTI recombination gates are 2µm deep for a length of 1µm. Two recombination gates are shared between three transfer columns. Charges in each transfer columns are binned on the same output node, the separation of a pixel in several columns being a design feature to make wider pixels but to keep the distance between the CDTI trenches short (the electrostatic potential in between the trenches would otherwise increase too much). The CDTI trenches are 200nm wide and filled with p-type polysilicon. The fabricated shift register has 220 CCD stages, 12µm long, 3.8µm large according common three transfer columns.

IV. Results and discussion

To test the recombination capability of the CDTI trenches, each pixel is filled to its full well capacity (~80 000e-) via electrical charge injection. The recombination gates are then switched back and forth between the high and low voltages at a fixed frequency and over a certain duration. The remaining charges are transferred to the readout node and the output signal is compared with subsequent, non-recombined injected charge packets. The number of recombined charges per pulse and pixel was measured as a function of several impactful parameters to study their influence on the electron-hole recombination mechanism. The temperature of the measurement setup room is fixed to 20°C.

First, the quantity of recombined charges was measured with respect to the low and high recombination gates bias. The recombination gates are pulsed between the high and low levels at a frequency of 30kHz. The rising / falling edges times are 10ns and when sweeping the high voltage, the low bias is -1V while for the inverse case, the high bias is 3V. The Fig. 5 presents the results of this measurement. It can be observed that at 3V, the recombination gates are in accumulation while strong inversion is obtained for a -1V bias. At these voltages, the recombined charge is maximum. These biases will thus be used for the following measurements.

Next, the quantity of recombined charges was measured as a function of rising / falling edges times. Again, the recombination gates are pulsed at 30kHz. The results presented Fig. 6 show that as expected, the shorter the pulse ramps, the more charges are recombined. Indeed, as explained in section II, charges susceptible of recombining are those who remained trapped at interface states while the trenches surface has transitioned to either strong inversion or accumulation. The traps having a certain time constant for emission of carriers, the shorter the transition, the more charges remain trapped while the surface electron or hole population builds up and therefore more charges are recombined at each transition.

Finally, the quantity of recombined charges was measured as a function of the recombination gate frequency. The high and low levels are the same as previously and the rising / falling edges times are 10ns. The Fig. 7 presents the result of this measurement. It is observed that the quantity of recombined charges is linearly proportional to the frequency of the pulse applied to the recombination gates, accordingly to the theory of charge pumping [6]. To flush excess charge or to reset a charge well, the mechanism should be as fast as possible in order to integrate the overall sensor operation sequence with minimum impact. Of course, the RC time constant of the CDTI gates limits the rising and falling edges times and the frequency is limited by the time necessary to bring the surface into strong inversion / accumulation just like in a frequency dependent MOS capacitance measurement. For the tested device, no limitation of this type was observed for the explored frequencies. Since the recombination process is still fully efficient at the maximum tested frequency, it means that about 40 impulsions at 5MHz can remove one full well charge in under 8µs. The efficiency of the mechanism being dependent on the density of interface traps at the trenches sidewalls, these measurements also offer a way to characterize CDTI sidewalls defect densities.

V. Conclusion

The use of capacitive trenches for charge level control via electron-hole recombination was demonstrated. The process was shown to be able to flush a large quantity of charges. The method could be used as an anti-blooming device or as a replacement to a reset transistor in any other imaging device that uses CDTI trenches to manage potential wells for charge storage. The technique requires no extra-CDTI gate so it has no impact on the photosensitive area of a pixel.

Acknowledgment

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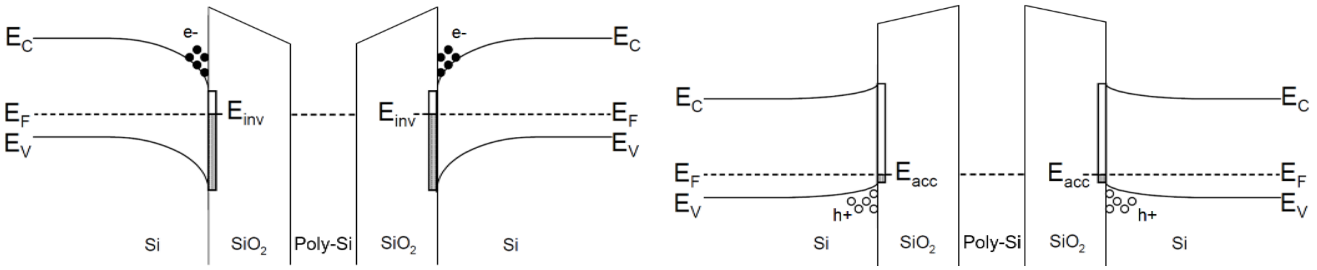

Fig. 1. Energy band diagram for a n-type MOS trench at strong inversion (left) and accumulation (right).

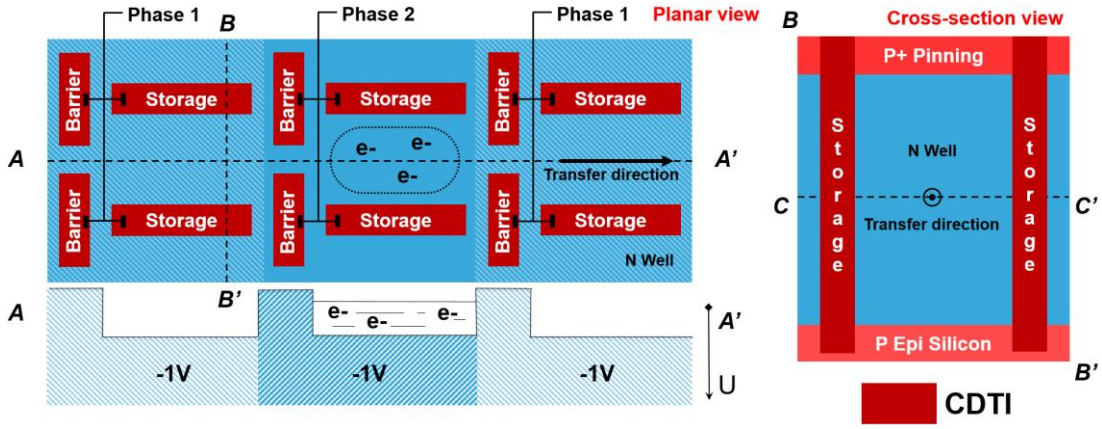

Fig. 2. Planar (left) and cross section along plane BB' (right) schematic views of the 2 phase charge transfer register and 1D schematic electrostatic potential (U) profile along transfer path AA' in light integration / storage state.

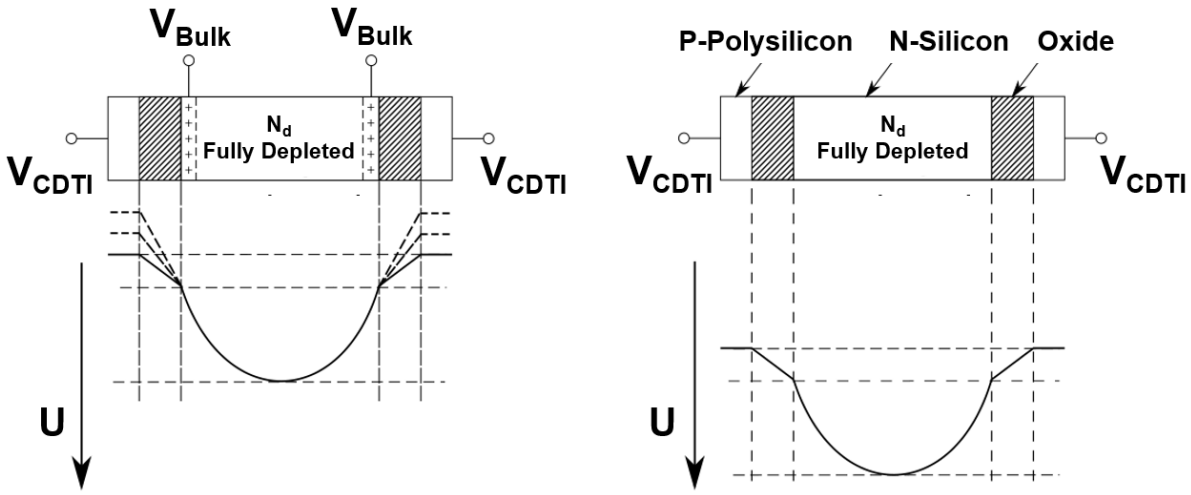

Fig. 3. Electrical representation of the pixel's structure in 1D (along axis CC' from Fig. 2) with electrostatic potential (U) shape for the storage (left) and transfer (right) states. For sufficiently low gates voltages at storage state, the electrostatic potential U is pinned by the bulk voltage (connected to ground) and a hole layer accumulates at the CDTI trenches sidewalls.

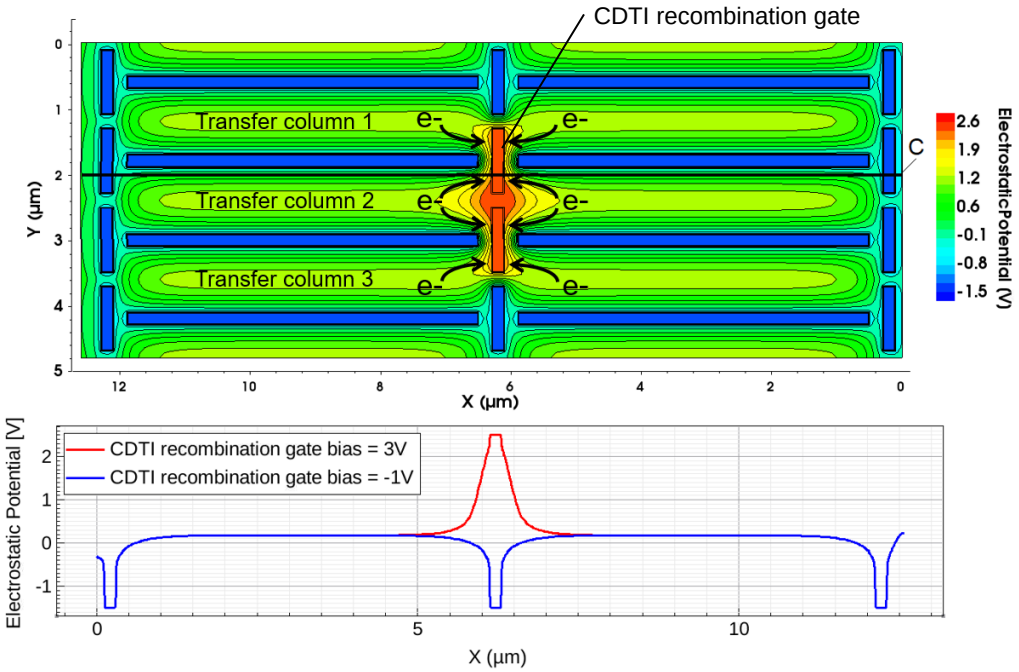

Fig. 4. Planar cross section (at depth 1µm) of the electrostatic potential map for the 12µm pixel from a 3D TCAD simulation with a 3V recombination gates bias (top) and electrostatic potential along the cutline C for a recombination gates bias of 3V and -1V (bottom).

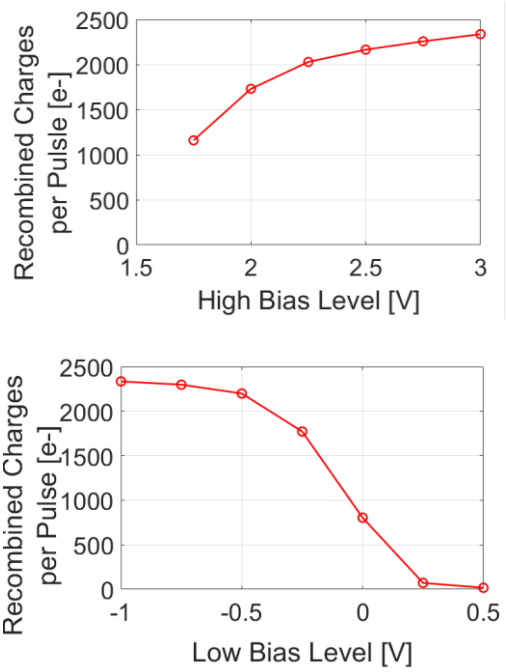

Fig. 5. Recombined charge as a function of the high (top) and low (bottom) recombination gate bias. Low bias is -1V when sweeping the high bias and the high bias is 3V in the inverse case. Measured with a pulse of frequency 30kHz and with a 10ns ramp.

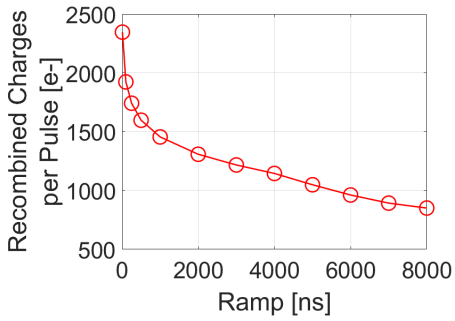

Fig. 6. Recombined charge as a function of recombination gate ramp. Low and high bias -1V and 3V respectively. The pulse frequency is 30kHz.

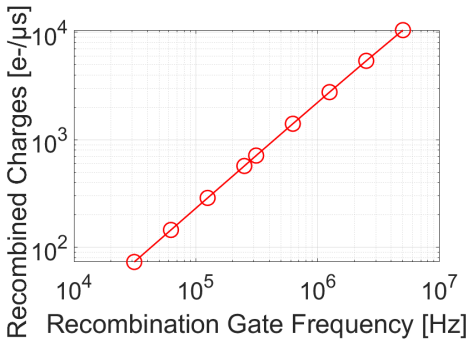

Fig. 7. Recombined charge per microsecond as a function of recombination gate frequency. Measured with a 10ns ramp. Low and high bias -1V and 3V respectively.