A 1280 x 1024 Backside Illuminated CMOS Image Sensor with 0.75e⁻ noise, 25fps and 120mW Power Consumption

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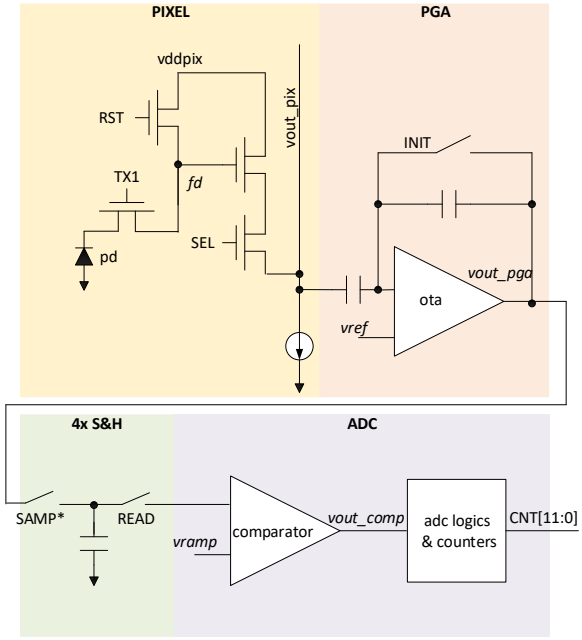
***Abstract*—In this paper, we present a 1" sized, high sensitivity BSI sCMOS image sensor with a resolution of 1.3 MP (1280 x 1024) and large 9.76 µm x 9.76 µm pixels. The demand of low noise CMOS imge sensor (CIS) is endless for scientific applications. Correlated multiple sampling (CMS) [1-4] is a powerful technique widely reported to reduce temporal noise in CIS. However, it also has clear disadvantages, such as lower frame rate and higher power consumption because of multiple A/D conversions. To overcome these two main issues, we present a chip which features both CMS and low power double edge counting ADC[5] to optimize temporal noise, A/D rate and power consumption at the same time. Compared with the sensor presented in [6], dark noise decreases from 1.8e⁻ to 0.75e⁻. Simultaneously, only 120mW power is consumed to run a 1.3Mpix sensor at 25fps.**

Analog signal path

The core analog signal path consists of a classical 4T low noise programmable-gain-amplifier(PGA) [7-8], four sets of sample and hold capacitors and a ramp ADC. Figure1 shows the structure. 4T PPD[9-13] pixel is widely used in low noise CMOS imagers, because it is easier to achieve higher conversion gain and lower dark current with less pixel transistors. The PGA could amplifier pixel signal at the first stage of analog path, thus it relaxes the noise floor of the devices after PGA. Besides, the PGA provides the first correlated-double-sampling(CDS)[14-15] for removing pixel reset KTC noise and offset. Four sets of sample and hold capacitors are implemented for supporting correlated multiple sampling(CMS) [1-4]. Four signals are sampled in serial, then they are merged before A/D conversion. As well known, these four samples contain different noise component, by averaging the high frequency thermal noise could be filtered. Ramp ADC is selected because of its simple structure for column level integration. In this design, the ramp ADC converts pixel reset and signal level four times each. Therefore, the ADC provides four times of CMS as well. The combination of these noise bandwidth limiter results in a significant noise reduction.



SAMP* contains sample_a, sample_b, sample_c, sample_d

Figure1 Readout chain structure

Figure2 illustrates the timing diagram of these analog blocks. There are mainly two phases, pixel reset level reading phase and pixel signal level reading phase. In the first phase, after switching off RST transistors, pixel reset level presents at the pixel bus, *vout_pix*. Then PGA INIT is released and pixel reset level are sampled by SAMP_A, SAMP_B, SAMP_C and SAMP_D in serial. Afterwards, pixel reset level A/D conversion starts by merging these four samples into one voltage. Once comparator

toggles when *vramp* is crossing pixel reset level, counters start counting. When *vramp* comes down, the counters stop counting and hold the values. The above sampling and conversion operations are repeated four times in pixel reset level reading phase. Following charge transfer by pulsing TX1 on and off, pixel signal level reading phase starts, in which similar four repeated sampling and conversion operations are executed. In total, PGA samples pixel reset and signal level 16 times each, and ADC converts pixel reset and signal level 4 times each.

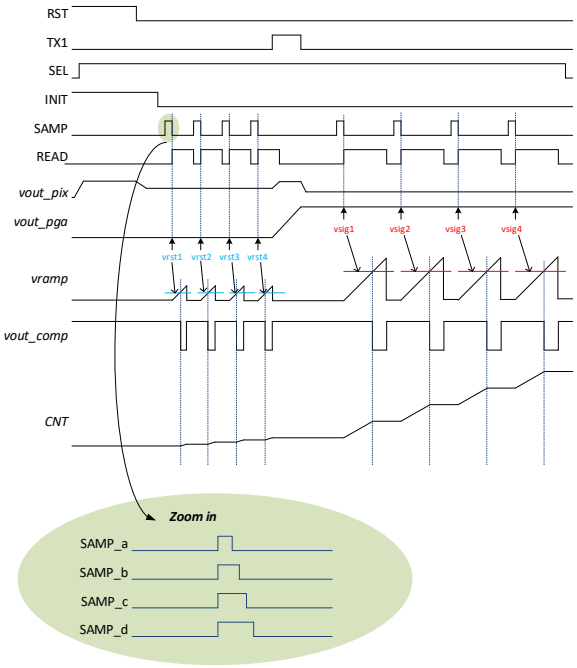


Figure2 Timing diagram of analog path

A measurement was made to compare the dark noise with different bit depth and ramp slope combination: 1) cms_4x, the default setting with four 10-bit ADC; 2) cms_2x, doubled *Vramp* slope with two 11-bit ADC; 3) cms_1x, quad *Vramp* slope with single 12-bit ADC. During this sets of measurement, the line-time and pixel timing were unchanged. Figure3 shows the *Vramp* timing within the measurement.

Noise histogram of the three cases are shown in Figure4. Clearly, both noise peak and noise tail are optimized with the default four 10-bit ADC setting.

The proposed CMS (ADC part) doesn't increase line-time, consume more power nor cost more layout area (counter depth is still 12-bit). However, it could reach a lower noise floor, Table1, than directly single 12-bit ADC.

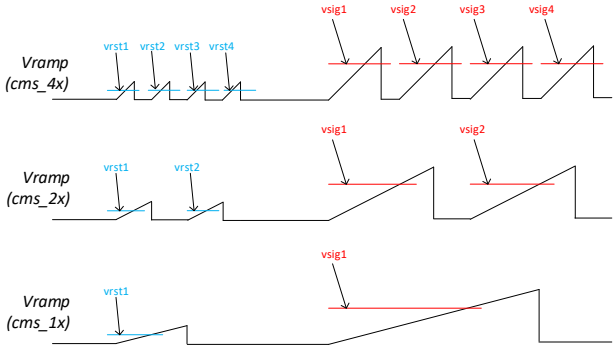


Figure3 *Vramp* diagram with different times of CMS

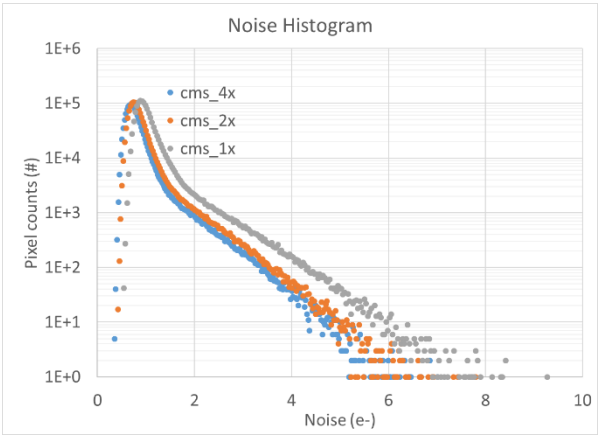


Figure4 Noise histogram

Table1 Dark noise comparison

Sets	Dark noise, peak (e^-)
CMS_4x	0.75
CMS_2x	0.80
CMS_1x	0.96

Low power double edge counter

Each A/D conversion mentioned previously converts the pixel signal into 10-bit digital value. In principle, by summing these four 10-bit numbers in adder could generate a 12-bit data. In this design, the adders are saved because the pluses generated by CMS ADC logics are counted sequentially on ADC counters.

Traditional ramp ADC has two main drawbacks: 1) slow conversion rate at high bit depth; 2) high power consumption because of continuously running counting clocks. We proposed a low power ADC in [5]. This design modifies some logics and realize a low power double edge counting ADC, which doubles conversion rate and significantly reduce power consumption.

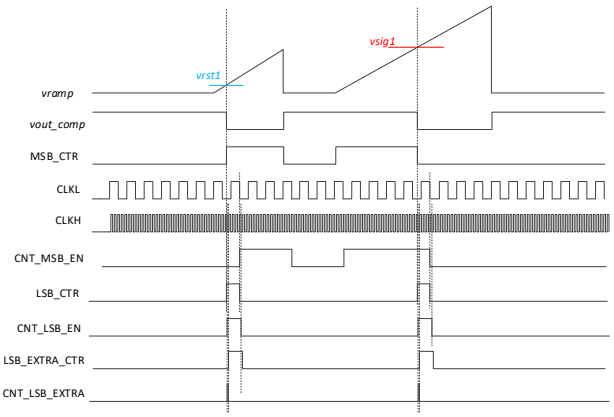


Figure5 Concept of low power double edge counting ADC

Figure5 illustrates a pair of *vrst* and *vsig* converted by low power double edge counting ADC. Thanks to the combination of a high speed clock, CLKH, and a low speed clock, CLKL, the total toggling of counters' flip-flop has a dramatically reduction. The design makes a frequency ratio of 48:1 between CLKH and CLKL, resulting in up to 10 CLKL counts and 47 CLKH counts to cover 9-bit counting range. The extra bit presents CLKH status (high level or low level) when the comparator toggles. The extra bit is generated with simple logic gates, so it costs less area and power. Therefore, the counters only have up to 228 toggling to get a 12-bit result. Comparing to 4095 toggling with traditional ramp ADC, the design reduces power consumption in counters by a factor around 18x.

Measurement Results

The prototype CIS with proposed analog path and ADC was fabricated using 180nm process. Die microphotograph is shown in Figure6. Response curve and nonlinearity are shown in Figure7. Table2 lists main specifications with the proposed low noise operation mode.

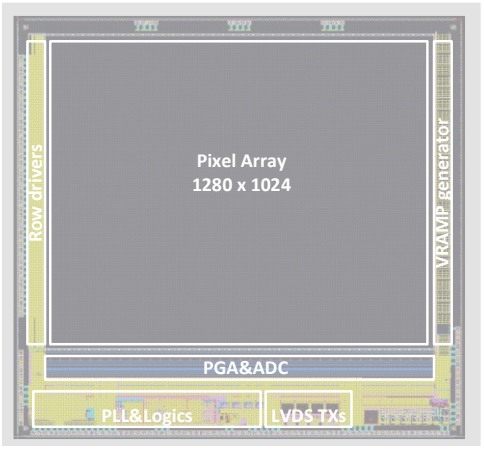


Figure6 Die photograph

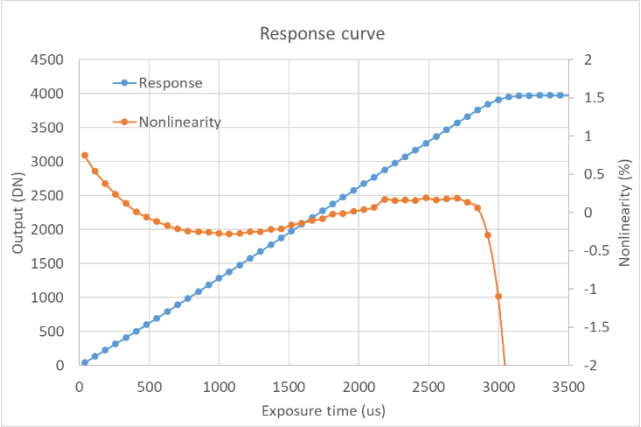


Figure7 Response and nonlinearity

Table2 Specifications with proposed low noise operation mode

Parameters	Value
Process	180nm BSI CIS 1P4M Process
Pixel size	9.76μm
Resolution	1280 x 1024
Supply voltage	3.3V/1.8V
CvG	98uV/e^-
Dark Noise	0.75e^-@16x PGA Gain
Full well	845e^-
Dynamic range	61dB
ADC depth	12bit
Non-linearity	<1%

Dark current	10e⁻/s@20℃
Frame rate	25fps
Power consumption	120mW
Peak QE	90%

References

[1] Sungho Suh,Shinya Itoh,Satoshi Aoyama,et al. Column-Parallel Correlated Multiple Sampling Circuits for CMOS Image Sensors and Their Noise Reduction Effects,ISSN 1424-8220,2010:9140-9154.

[2] Yong Lim, Kyoungmin Koh, Kyungmin,et al. A 1.1e- Temporal Noise 1/3.2-inch 8Mpixel. CMOS Image Sensor using Pseudo-Multiple Sampling[J]. IEEE International Solid_State. Circuit Conference(ISSCC),2010,22(2):396-398.

[3] Assim Boukhayma,Arnaud Peizerat, Christian Enz.A Correlated Multiple Sampling Passive Switched Capacitor Circuit for Low Light CMOS Image Sensors[C].International Conference on Noise and Fluctuations(ICNF),2015.

[4] Jamali-Zavareh, Shiva, Harjani, Ramesh, Jitter Suppression Techniques for High-Speed Sample-and-Hold Circuits[J]. IEEE Transactions on Circuits and Systems,2020,67(1):1-11.

[5] Cheng Ma, X.W., A low power counting method in Ramp ADCs used in CMOS image sensors. IISW, 2013.

[6] Cheng Ma, Yang Liu, Yang Li, Quan Zhou, Xinyang Wang and Yuchun Chang, A 4-M Pixel High Dynamic Range, Low-Noise CMOS Image Sensor with Low-Power Counting ADC, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO.8,AUGUST 2017.

[7] Jingyu Wang, Zhangming Zhu, Shubin Liu, Ruixue Ding, A low-noise programmable gain amplifier with fully balanced differential difference amplifier and class-AB output stage, Microelectronics Journal, vol. 64, pp. 86, 2017.

[8] Bingzhao Zhang, Zhiqun Li, A low power programmable gain amplifier with 70-dB control range in CMOS technology[C]. 2011 IEEE 13th International Conference on Communication Technology (ICCT), Page(s): 1074–1077.

[9] A. Pelamatti et al., Charge transfer inefficiency in pinned photodidode CMOS image sensors: simple Montecarlo modeling and experimental measurement based on a pulsed storage-gate method, Solid-State Electron., vol. 125, pp. 227-233, Nov. 2016.

[10] Y.Li et al., Charge transfer efficiency improvement of a 4-T pixel by the optimization of electrical potential distribution under the transfer gate", J. Semicond. vol. 33, no. 12, pp. 124004, Dec. 2012.

[11] J. Liu, W. Chen, Z. J. Wang, Y. Y. Xue, Z. B.Yao, B.P.He, et al., Simulation and measurement of total ionizing dose radiation induced image lag increase in pinned photodiode CMOS image sensors", Nuclear Instruments and Methods in Physics Research A, vol. 856, pp. 32-35, Jun. 2017.

[12] O. Marcelot, V. Goiffon, F. Nallet and P. Magnan, "Pinned photodiode CMOS image sensor TCAD simulation: In-depth analysis of in-pixel pinning voltage measurement for a diagnostic tool, IEEE Trans. Electron Devices, vol. 64, no. 2, pp. 455-462, Feb. 2017.

[13] C. Cao, B. Shen, B. Zhang, L. Wu and J. Wang, An improved model for the full well capacity in pinned photodiode CMOS image sensors, IEEE J. Electron Devices Soc, vol. 3, no. 4, pp. 306-310, Jul. 2015.

[14] S. Son, S. Jeon, S. Namgung, J. Yoo and M. Song, A one-shot digital correlated double sampling with a differential difference amplifier for a high speed CMOS image sensor, 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp. 1054-1057.

[15] S. Park, T. Cho, M. Kim, H. Park and K. Lee, A shutter-less micro-bolometer thermal imaging system using multiple digital correlated double sampling for mobile applications, Symposium on VLSI Circuits, 2017.