Characterization of Random Telegraph Signal Histogram according to Floating Diffusion Potential in CMOS Image Sensor

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Abstract—This paper introduces the analysis of signal behavior of random telegraph signal (RTS) pixels in CMOS image sensor with applied floating diffusion (FD) voltage. We investigated the temporal behavior of blinking pixels with FD voltage variation, through which we categorized them into three groups according to their electrical behavior. It was also shown that a number of RTS pixels could be effectively decreased by increasing the channel current of SF transistor. It is expected that this result may be a novel implication to understand the noise characteristics of CMOS image sensor.

I. INTRODUCTION

The so-called blinking pixel is one of the main sources of image degradation in CMOS image sensor [1]. It is well known that such noise is induced by device defects located at Si surface, oxide interface trap, or off-state leakages from transistors and FD. Thus, there has been a significant number of studies done to minimize physical defects using fabrication techniques [2-5]. In terms of image processing, it is difficult to suppress or eliminate the noise due to its random behavior. Hence, it is important to thoroughly characterize the noise for better understanding in the viewpoint of pixel design to minimize its occurrence.

II. CLASSIFICATION OF BLINKING PIXELS

The pixels in the samples are monitored during a thousand of frames in order to include pixels even with a small number of occurrences. If they show a large signal difference in subsequent two frames, even only once in all the frames, it is considered as a blinking pixel.

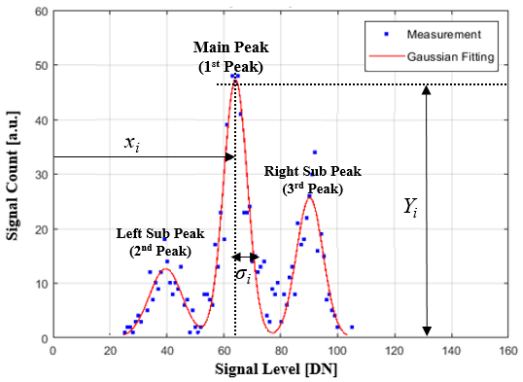


Fig. 1. Parameters used for Gaussian fitting (x_i : signal level of i-th peak, σ_i : standard deviation, Y_i: maximum of signal count)

Its signal histogram is plotted and fitted with Gaussian distribution function (Fig. 1).

$$y_i = Y_i \exp\left(-\frac{1}{2}(x - x_i)^2/\sigma_i^2\right) \quad (1)$$

Figure 2 shows the examples of Gaussian-fitted histograms. The normal pixels typically have a single primary peak. On the other hand, blinking pixels mostly show multiple satellite peaks having various heights and distribution. For detailed understanding on such signal variation, all pixels are classified according to their cause of the signal change. Firstly, the pixels are divided into RTS and temporal noise (TN) group in accordance with the existence of satellite peaks. The pixels in the RTS group show discrete signal change generating the satellite peaks. Meanwhile, in the TN group, primary peaks are broaden instead of displaying distinct satellite peaks.

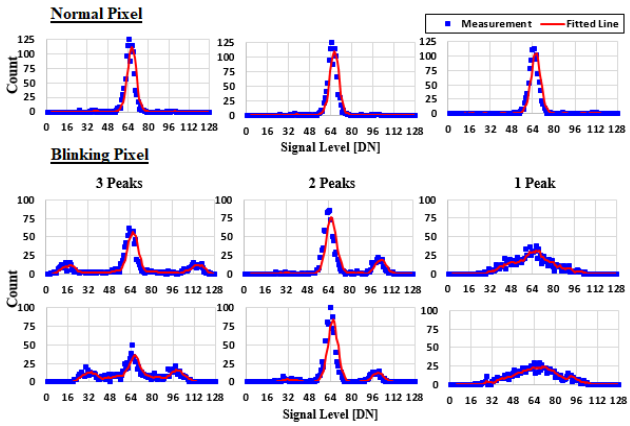


Fig. 2. Measured and fitted signal histograms of normal pixels and blinking pixels

Secondly, the RTS group is divided into two groups according to electrical behaviors. If satellite peaks appear regardless of transfer transistor (TX) operation, it is classified as SF RTS group. The random noise generated from SF can be added to output signal when TX is turned off. If this condition does not meet, it is classified as variable junction leakage (VJL) RTS group. The random signals due to leakages from photodiodes and transistors are easily observed when TX is turned on. The RTS pixel due to gate-induced drain leakage (GIDL) can be detected by changing the level of the negative charge pump (NCP) of TX. In this work, however, the GIDL

group is not observed since the unintentional leakages are restrained appropriately in the investigated samples. Thus, the pixels in the samples are scrutinized three groups: SF RTS, VJL RTS and TN.

	Mechanism	Existence of Sub Peak		Change with NCP	Distribution (%)
		TX OFF	TX ON		
RTS	Source Follower	O	O	X	35.7
	VJL	X	O	X	27.2
	GIDL	O	O	O	-*
TN	Dark Noise	X	X	X	37.1
	GIDL	X	X	O	-*

Fig. 3. Classification of blinking pixels and their characteristics (* : Absence in this work)

III. Effects of Floating Diffusion Voltage

A. *Increase of Occurrence of Satellite Peak with Higher FD Voltage*

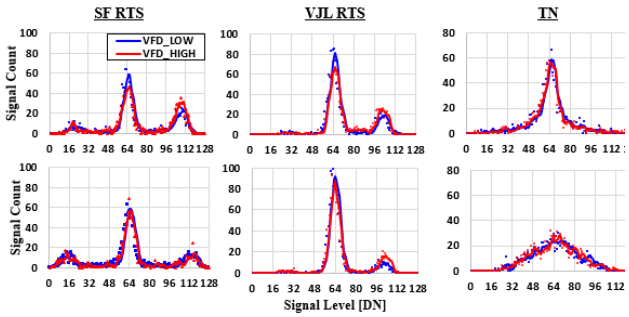


Fig. 4. The difference between the signal histograms at low and high FD voltage

To examine the electrical behavior of the sorted pixels, additional FD voltage is applied to each group. Figure 4 displays the changes of signal histograms with the different FD voltages. The pixels in the TN group exhibit no response to the increased voltage. The histogram of the RTS group pixels, however, show the decreased height of the primary peaks and the increased height of the sub-peaks. The decreased portion of the primary peaks contributes to the increased count of the sub-peaks.

To show clear tendency with respect to signal count (y-axis in Fig. 4), the two histograms of each pixel are subtracted and plotted (Fig. 5). One data point in the figure indicates a single pixel. It can be seen that the signal counts of sub-peaks are increased in most of the pixels with higher FD voltage. In addition, such phenomenon only happens when TX is turned on. This implies that it is basically caused by TX operation and additional FD voltage has negative influence on noise performance. In the same manner, the changes of the signal levels (x-axis in Fig.4) are calculated and shown in Fig. 6. All the peaks are concentrated near the origin, indicating that the FD voltage is not involved in the signal level.

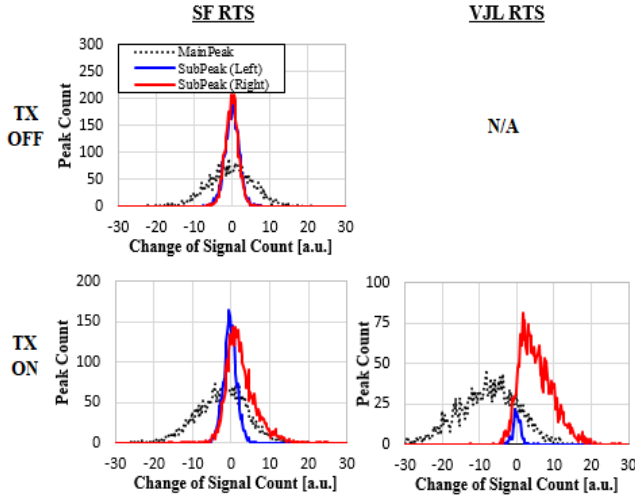


Fig. 5. Changes of RTS signal counts with FD voltage increase. A peak shift to positive direction means that the sub-peaks are more encouraged at higher FD voltage

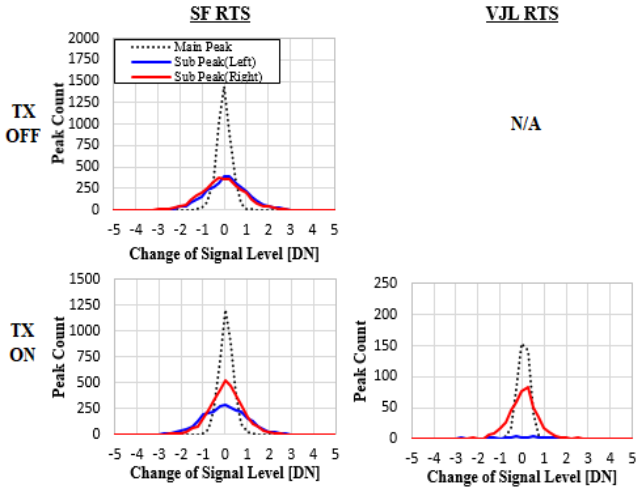
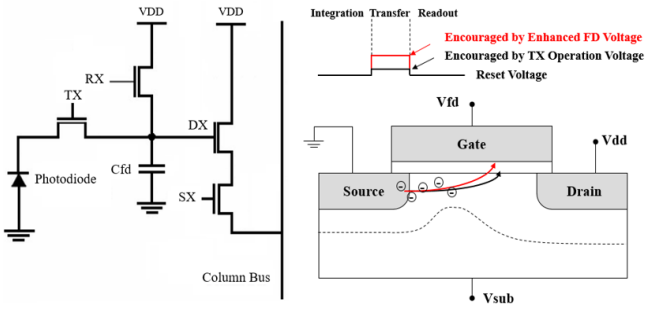


Fig. 6. Changes of RTS signal level with FD voltage increase. In contrast to Fig. 5, the histograms are fixed at the origin. This means that the FD voltage has no effect on the signal level of the sub-peaks.

B. *Enhanced Hot Carrier Injection at DX Oxide Surface*

According to the analysis, the increase of RTS satellite peak happens regardless of the classification type. This implies that it cannot be explained by the previously known RTS mechanisms associated with the device defects [2-5].

Figure 7(a) shows a pixel diagram of CMOS image sensor. The signal generated at FD is transferred to DX and SX. The increased FD voltage, i.e., increased gate voltage of SF transistor attracts more channel electrons toward the gate oxide interface by enhanced vertical electric field. This results in increased probability of charge trapping at gate oxide interface defects.



(a) (b)

Fig. 7. (a) Schematic of 4T CMOS image sensor
(b) Excited electrons in the SF channel due to enhanced FD voltage

The magnitude of RTS fluctuation ($\Delta I_D/I_D$) is shown in equation (4) [6-11]. g_m is channel transconductance, W is channel width, L is channel length, C_{ox} is gate oxide capacitance, and α is an empirical parameter.

$$\frac{\Delta I_D}{I_D} = \alpha \frac{g_m}{I_D} \cdot \frac{q}{WLC_{ox}} \tag{4}$$

This RTS amplitude has only 5% variation in the strong inversion region [8-10]. This results in the restricted signal level variation in Fig. 6.

Moreover, as it is considered that the occurrence changes with higher FD voltage in Fig. 5, we can understand this mechanism by the capture and emission time. The capture and emission time can be expressed as Eq. (2) and (3). ΔE_B indicates the energy level for the trap, and ΔE_{CT} indicates the energy level between the trap and conduction band. σ_0 is trap section, T is the absolute temperature, I_D is the drain current level of MOSFET, and χ and η are parameters for fabrication.

$$\bar{\tau}_c = \frac{\exp\left(\frac{\Delta E_B}{kT}\right)}{I_D T \sigma_0 \chi} \tag{2}$$

$$\bar{\tau}_e = \frac{\exp\left(\frac{\Delta E_B + \Delta E_{CT}}{kT}\right)}{T^2 \sigma_0 \eta} \tag{3}$$

They are bias-dependent as the high voltage promotes the movements of electrons [6,8]. Considering this, we set an analytical model to understand this situation regarding FD voltage and RTS.

C. Modeling with Timing Diagram : Interpretation with PTO

Figure 8 explains the generation of discrete RTS levels in CMOS image sensors with correlated double sampling scheme. The primary peak corresponds to the case (B) and (C) where the level of reset and signal readout is the same. The left and right satellite peaks correspond to the case (A) and (D), respectively due to the different signal level at reset and signal readout state.

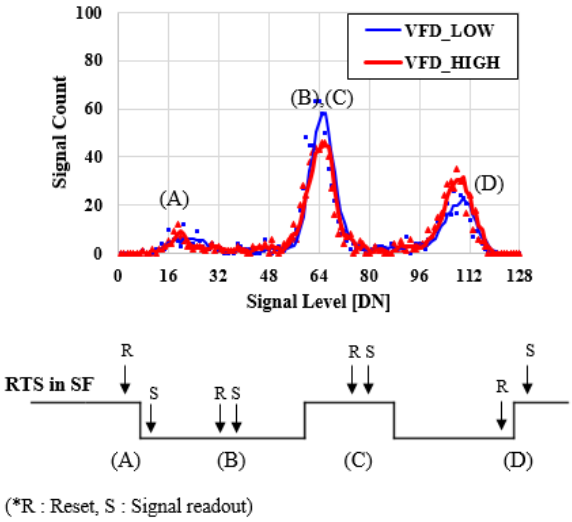


Fig. 8. Diagram explaining the mechanism of discrete RTS levels with correlated double sampling scheme

The probability of each peak can be calculated as (5) and (6), where P_1 and P_2 are the probability that RTS occurs at the reset state and signal readout state. P_1 and P_2 can be described with PTO, which is determined by capture and emission time for the electrons passing through the channel [12-14]. The increment of the satellite peaks when the enhanced voltage is applied can be explained by the PTO variation.

$$P_{left} = P_1(1\text{-}P_2) \tag{5}$$

$$P_{right} = P_2(1\text{-}P_1) \tag{6}$$

$$P(t) = \frac{\bar{\tau}_e}{\bar{\tau}_c + \bar{\tau}_e} + Ke^{-\left(\frac{1}{\bar{\tau}_c} + \frac{1}{\bar{\tau}_e}\right)t} \tag{7}$$

PTO can be divided into transient and steady state. The transient state value describes the change of PTO while FD voltage is modified. When the higher FD voltage is applied, the capture and emission time of activated electrons are reduced. PTO changes larger with the higher FD voltage (Eq. (7)).

Meanwhile, the steady state value of PTO describes the situation that FD voltage is sufficiently stabilized. It is derived from the ratio of the capture and emission time represented as Eq. (8) [6,9]. The equation can be organized by the gate voltage with the variables, K_1 and K_2, as in Eq. (9). By using equation (7) and (9), the relation with the gate voltage and the steady-state value of PTO is defined as equation (10). When the higher FD voltage is applied, the steady state value of PTO becomes increased.

$$\ln\left(\frac{\bar{\tau}_c}{\bar{\tau}_e}\right) = -\frac{1}{kT}\left[\left(E_{C_{ox}} - E_T\right) - \left(E_C - E_F\right) - \phi_0 + q\psi_s + q\frac{x_T}{T_{ox}}\left(V_g - V_{FB} - \psi_s\right)\right] \quad (8)$$

$$\frac{\bar{\tau}_c}{\bar{\tau}_e} = \exp(K_1 - K_2 V_g) \quad (9)$$

$$P(V_g) = \frac{\bar{\tau}_e}{\bar{\tau}_c + \bar{\tau}_e} = \left(1 + \frac{\bar{\tau}_e}{\bar{\tau}_c}\right)^{-1} = \left(1 + \exp(K_1 - K_2 V_g)\right)^{-1} \quad (10)$$

In Fig. 9, a simple timing diagram model is suggested, which shows the change of PTO according to FD voltage level during signal readout process. While the high voltage is applied, both steady and transient response of PTO are accelerated. Especially, the probability P_2 becomes larger than P_1 due to incomplete attenuation when SF is in weak inversion state. It raises the right sub-peak rather than the left one in Fig.4.

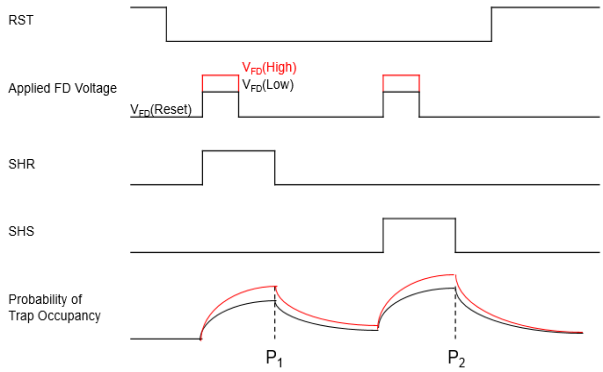


Fig. 9. Timing diagram and probability of trap occupancy

In order to suppress the SF RTS caused by the increased FD voltage, we optimize the drain current level of SF transistor by controlling channel doping and successfully reduce the pixel count in both of SF and VJL RTS groups (Fig. 10). The optimization with channel current is well known solution for minimizing RTS in MOSFET [15,16]. We suggest that this method has also positive effect on managing the random variation due to FD voltage.

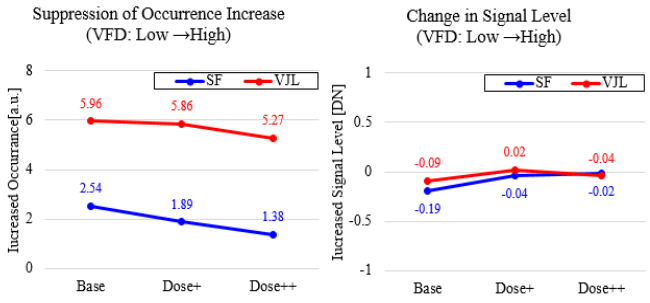


Fig. 10. Suppression of occurrence increase and change in signal level with the FD voltage increment

IV. Conclusion

We established the classification method for blinking pixels in CMOS image sensor chips, according to their electrical behavior. Blinking pixels could be categorized into 5 different groups and it was found that amplitudes of sub-peaks in RTS histogram were affected by FD potential. The RTS characteristics depending on the different level of FD voltage and SF channel transconductance were analyzed in terms of PTO and the timing diagram model. We believe this work can provide the guide for pixel design such as suitable FD voltage level in perspective of RTS property for superior noise performance.

References

[1] C. Leyris, "Impact of Random Telegraph Signal in CMOS Image Sensors for Low-Light Levels," *2006. Proceedings of the 32nd European Solid-State Circuits Conference*, pp. 376-379, 2006.

[2] C. Chao, "Random Telegraph Noises from the Source Follower, the Photodiode Dark Current, and the Gate-Induced Sense Node Leakage in CMOS Image Sensors", *Sensors*, vol. 19, 2019.

[3] V. Goiffon, "New source of random telegraph signal in CMOS image sensors", *Proc. IEEE Int. Image Sensor Workshop (IISW)*, pp. 212-215, Jun. 2011.

[4] B. Pain, "Twinkling pixels: Random telegraph signals at reset gate edge", *Proc. IEEE Int. Image Sensor Workshop (IISW)*, pp. 234-237, Jun. 2007.

[5] J. Jung, "Reduction of Random Noise in Complementary Metal Oxide Semiconductor Image Sensors by Gate Oxide Interface Control", *Japanese Journal of Applied Physics*, vol.45, Apr. 2006.

[6] N. Amarasinghe, "Extraction of oxide trap properties using temperature dependence of random telegraph signals in submicron metal–oxide–semiconductor field-effect transistors", *Japanese Journal of Applied Physics*, vol. 89, Feb. 2001.

[7] G. Wirth, "Modeling of statistical low-frequency noise of deep-submicrometer MOSFETs", *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1576-1588, Jul. 2005.

[8] N. Hamid, "Time-Domain Modeling of Low-Frequency Noise in Deep-Submicrometer MOSFET", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 1, pp. 245-257, Feb. 2008.

[9] K. Hung, "Random telegraph noise of deep-submicrometer MOSFETs", *IEEE Electron Device Letters*, vol. 11, no. 2, pp. 90-92, Feb. 1990.

[10] A. Asenov, "RTS amplitudes in decananometer MOSFETs: 3-D simulation study," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 839-845, Mar. 2003.

[11] J. Pavelka, "Activation energy of RTS noise", *Radioengineering*, vol.20, no. 1, pp. 194-199, Apr. 2011.

[12] X. Wang, "Random telegraph signal in CMOS image sensor pixels", *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, pp. 115-118, Dec. 2006.

[13] C. Chao, "Statistical Analysis of the Random Telegraph Noise in a 1.1 μm Pixel, 8.3 MP CMOS Image Sensor Using On-Chip Time Constant Extraction Method," *Sensors*, vol. 17, no. 12, p. 2704, Nov. 2017.

[14] M. Philippe, "Low-frequency noise impact on CMOS image sensors", *Conference on Design of Circuits and Integrated Systems*, Nov. 2009.

[15] A. Lahav, "Optimization of Random Telegraph Noise Non Uniformity in a CMOS Pixel with a Pinned-Photodiode," *Proc. IEEE Int. Image Sensor Workshop (IISW)*, pp. 230-234, Jun. 2007.

[16] S. Ichino, "Impact of Drain Current to Appearance Probability and Amplitude of Random Telegraph Noise in Low Noise CMOS Image Sensors", *Int. Conf. Solid State Devices and Materials*, pp.331-332, 2017.