A Multi-Simultaneous-Gate CMOS Lock-in Pixel Image Sensor for Time-Resolved Near-Infrared Spectroscopy

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I. INTRODUCTION

Near-infrared spectroscopy (NIRS) is a powerful tool to obtain the non-invasive measurement of biological tissues. Time-resolved NIRS (TR-NIRS) has the advantage over continuous-wave NIRS, i.e. higher sensitivity and penetration depth. The conventional detector of TR-NIRS is a photomultiplier tube (PMT) with time-correlated single-photon counting (TCSPC), which is bulky and not scalable. Recent development has seen the solid-state approach of SPAD and SiPM being used [1], [2]. Pinned photodiode (PPD) based CIS have also been explored for time-resolved applications [3]–[5], however, the limited intrinsic response and sensitivity hinder their use in TR-NIRS. This paper discusses the current preliminary progress of another solid-state approach, a CMOS image sensor-based high-time resolution lock-in pixel for the application of TR-NIRS.

II. PIXEL DESIGN

Figure 1(a) shows the two-gate one-drain modulator architecture, which is based on an 8-tap pixel structure with eight pairs of lateral electric field charge modulator (LEFM) gate [4], where 2 sets of 3-taps are connected to G1 and G2, while another 2-taps are connected to GD. The pixel is designed to enhance the photoelectron transfer speed. Three n-type ion

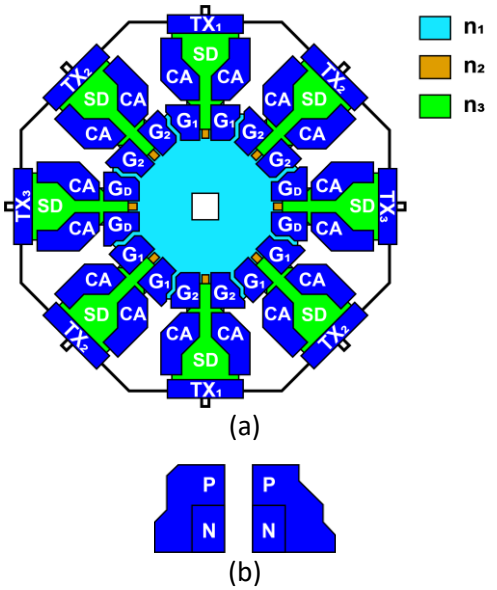


Figure 1: (a) 2-gate 1-drain pixel architecture with 8-tap structure. The pixel is made using 3 n-type doping. (b) Bipolar gate is used to better create potential slope due to work function difference.

implantations are used to create an electric field slope towards the storage diodes (SD). The center of the pixel is void of n-type doping to form a peak of low potential, which increases towards the LEFM gates due to the n_1 layer. n_2 regions extend from the opening of the pair of LEFM gates to the SDs to control and accelerate photoelectron flows. The third n-layer, n_3 further strengthens the electric field and forms the storage well. The modulation gates are bipolar, where the difference in the work function of n-type and p-type gates helps to create a smoother potential slope (Figure

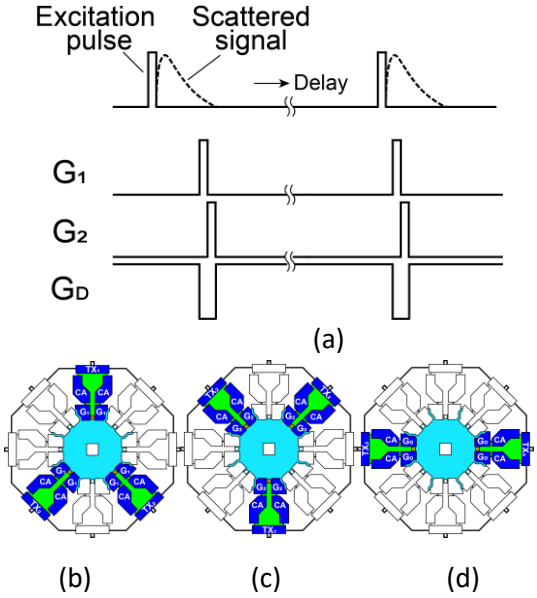


Figure 2: (a) Timing diagram for the pixel operation. Excitation pulse is delay-scanned to obtain full response of the scattered signal. The effective gates when clock b) G1=ON c) G2=ON, d) GD=ON

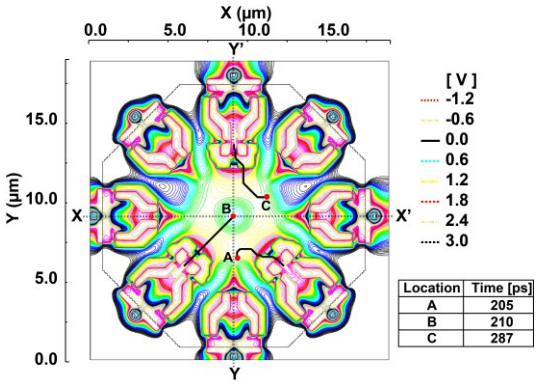


Figure 3: Simulated 2-D potential plot of the modulator showing photoelectrons transfer from the three initial locations at depth of 5 μm towards gates G1.

1b). Figure 2(a) shows the timing diagram of using all eight taps of the pixel for the TR-NIRS measurement, where the laser pulse is scanned to obtain the full response of the scattered signal. Figures 2 (b), (c), and (d) show the effective gates when G1, G2, and GD

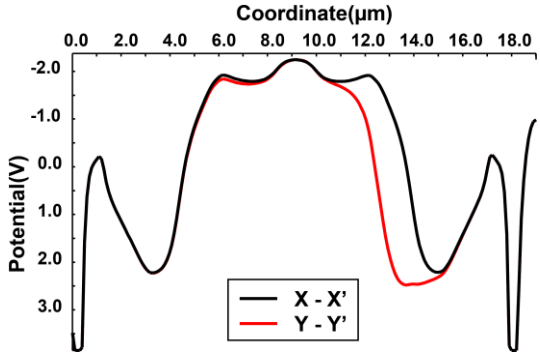


Figure 4: Simulated potential profile across X-X' line (both gates are OFF) and Y-Y' line (Y' side gate is ON).

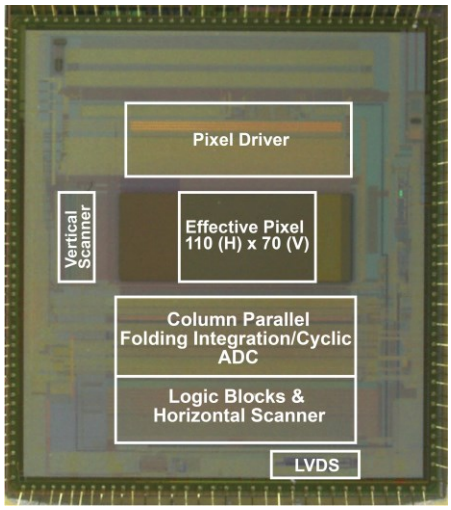


Figure 5: Chip micrograph

are turned ON, respectively. Figure 3 illustrates the simulated 2-D potential plot when G1 is ON, G2 and GD are OFF, and a negative substrate voltage of -3 V is applied. The red dots A, B, and C represent the initial positions of photoelectrons at depth of 5 μm, and the black lines represent the simulated photoelectron transfer paths, achieves a fast transfer time with a maximum of 287 ps, even at the edge of the PPD. Figure 4 shows the simulated potential profiles along X-X' and Y-Y' lines of Figure 3. When both gates are turned off, there is a sufficient barrier to

prevent the charge from moving to the SDs. There are no potential barriers when the gates are turned on, pathing the way for high-speed charge transfer.

III. IMPLEMENTATIONS

A prototype chip for verification has been fabricated using 0.11 µm CIS technology with a pixel array of 186 (H) × 70 (V) (effective pixel 110 (H) × 70 (V)) and pixel pitch of 22.4 µm, as shown in Figure 5. For proof of concept, a preliminary measurement of the intrinsic response using two simultaneous gates (top two gates from Figure 2(c)) and a single time window is conducted with the experimental setup shown in Figure 6. A laser diode of 780 nm wavelength with a pulse width of 80 ps is utilized (LDB-100, Tama Electric Inc., Japan). The trigger signal to the laser diode is scanned by using the phase-locked loop (PLL) from the onboard field-programmable gate array (FPGA) at 104 ps step. The time window of pixel gates is controlled using FPGA. Figure 7(a) shows the pixel response from the two taps in a single time window. The measured signal from both taps are added and averaged over the region of interest (ROI) of 60 × 110 pixels and 11 repetitions. Numerical differentiation is then applied to the resulting response. The intrinsic response time constant of the sensor obtained is 305 ps, as shown in Figure 7(b).

The fast intrinsic response is an essential parameter for a time-resolved detector to obtain higher resolution and accuracy results. Based on the diffusion theory [6], the absorption coefficient can be determined by the slope of the tissue reflectance signal. The measured response is the convolution of tissue reflectance and intrinsic response.

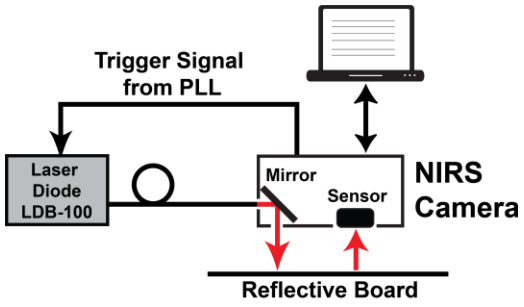
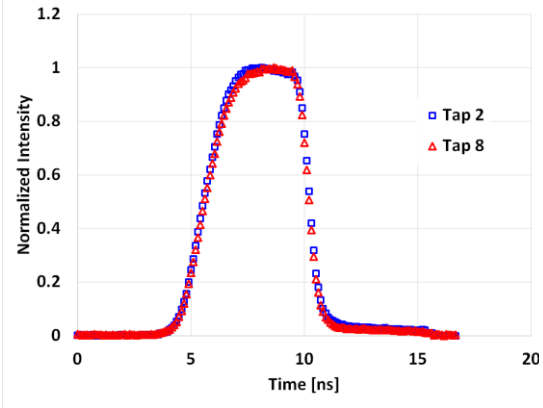
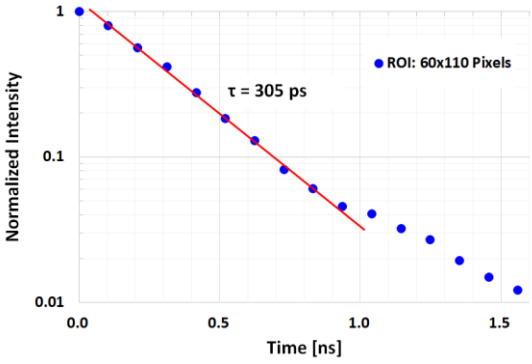


Figure 6: Experimental setup of the intrinsic response measurement. Trigger signal to the laser diode is scanned at 104 ps step by the PLL from onboard FPGA.



(a)



(b)

Figure 7: (a) Pixel response of two taps for laser wavelength of 780 nm, laser pulse width of 80 ps. (b) Intrinsic response of the pixel is obtained to be 305 ps.

Deconvolution or curve fitting can then be employed to recover the real tissue reflectance.

IV. CONCLUSION

This article proposes a CMOS lock-in pixel multi-simultaneous-gate image sensor intended for the TR-NIRS system. The optimization of the pixel structure creates a high potential slope with no barrier to achieve a fast-intrinsic response. Characterization using two taps simultaneous-gate demonstrates the intrinsic response of 305 ps measured by laser diode operating at 780 nm. The developed CIS-based TR-NIRS system aims to be the initial step towards compact, wearable TR-NIRS applications.

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