Dynamic Crosstalk Analysis for Branching Image Sensors

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Abstract This paper reviews the concept of a backside-illuminated image sensor with a branching channel. Further, we present the analysis of the temporal crosstalk due to transient motions of signal electrons with varying voltages applied to the sensor. A Monte Carlo simulation shows that the average arrival time of signal electrons to a floating diffusion is 386 ps, which is equivalent to the frame rate of 2.59 Gfps. The frame count of the sensor is 12 frames. The sensor can operate in two modes: a burst imaging mode and a continuous imaging mode for a frame count of 100 to 1,000 frames. Burst imaging distributes signal electron packets to 12 in-pixel floating diffusions (FDs) in turn. Signal accumulation is also possible for weak incident light from reproducible events by repeating the image capturing process; theoretically, noiseless ultrafast imaging is possible, especially with system cooling. Continuous imaging further transfers the image signals from the FDs continuously to memory elements in a stacked memory chip. The signal transfer rate from each FD is 1/12 of that for image sensors with a single FD, and thus the signal transfer noise decreases by $1/\sqrt{12}$.

Keyword ultra-high-speed imaging, branching image sensor, super-temporal resolution, dynamic analysis, temporal crosstalk

1. Introduction

In 2018, flying light was captured for the first time by our backside-illuminated (BSI) multi-collection-gate image sensor [1]. Being a proof-of-concept sensor, the sensor had a frame count of only 5 or 10 frames. Moreover, the sensor had a low field over the p-wells, which seriously caused long arrival times of signal electrons. To increase the frame count, a BSI CCD/CMOS hybrid branching image sensor called Hanabi was presented [2]. The sensor aims to capture 10 to 50 consecutive images while operating at 1 Gfps. To reduce the arrival time, we proposed an inverted pyramid photodiode (PD). However, the process remains under development. Therefore, in this paper, we use a square PD much narrower than the pixel size for the analysis. We originally named the PD a light/charge guide pipe.

This paper reviews the concept of the Hanabi image sensor with the light/charge guide pipe and presents the analysis of the temporal crosstalk due to transient motions of signal electrons. The paper discussed:

(a) an overview of a BSI branching image sensor, including its fundamental structure, independent analyses on the guide pipe and the branching channel in the diffusion layer, and overall performance of the combined structure of the photodiode and the diffusion layer.

(b) the two operation modes of the sensor, and

(c) the analysis of the temporal crosstalk by dynamic simulation.

2. Overview of a Backside-illuminated Branching Image Sensor 2.1 Fundamental Structure

Figure 1a shows the cross-section of Hanabi, which is composed of an upper light/charge guide pipe to receive light incident at the backside, and a lower diffusion layer on the front side to store signal electrons. Figure 1b shows the configuration of the elements on the front side. The sensor has multiple branching charge transfer gates radially arranged from the center of the pixel.

Figure 1. A BSI CCD/CMOS hybrid branching image sensor, Hanabi: (**a**) a cross-section, (**b**) elements on the front side (GG, guide gate; FG, first-branching gate; SG, second-branching gate; FD, floating diffusion; RS, reset gate; RD, reset drain).

Figure 2. Potential contour lines, where p_{GP} is the concentration of the boron layers over the walls of the guide pipe. With p_{GP} , the potential bends to guide electrons toward the center.

(1) Upper light/charge guide pipe (GP)

The guide pipe is a square photodiode. A thin layer of boron is strongly doped to the wall of the guide pipe to create the bending potential that forces electrons to move toward the center and hence prevents them from colliding with the wall.

Ideally, the average vertical E-field at the center of the guide pipe is fixed at 25 kV/cm, at which electrons approach the saturation drift velocity. Then, the standard deviation of the travel time of electrons inside the guide pipe depends on the length L_{GP} , the width W_{GP} , and the concentration of boron ions p_{GP} implanted in thin layers over the walls of the guide pipe. Figure 2 shows the potential contour lines depending on the boron implantation. A narrow and tall guide pipe increases the collision probability of electrons to the wall. The higher boron concentration forces electrons to move toward the center, thus decreasing the collision probability yet increasing the arrival time. Figure 2c shows the collision rate and the standard deviation of arrival times of electrons in the guide pipe. When g_{GP} > 1e16 cm⁻³, the collision rate decreases to less than 10% while the standard deviation suddenly surges. Therefore, an optimum value of g_{GP} is to be at 1e16 cm⁻³.

(2) Lower branching channels at the front side

A hexagonal guide gate (GG) is located at the center of the pixel. The design follows two-stage branching. Six first-branching gates (FGs) are placed to surround the GG. Then, each FG bifurcates into second-branching gates (SGs). Each SG connects to the storage element consisting of the floating diffusion (FD), a reset gate, and a reset drain.

Figure 3a conceptually shows an ideal channel potential profile from a waiting FD (FDw) to a collecting FG (FDc). The ideal horizontal potential profile linearly increases from an upstream (lowvoltage) SG toward a downstream (high-voltage) SG. From the modulation functions of the channel potentials, the voltage amplitudes applied to each gate are uniquely determined as follows:

a) assume that the amplitude of the SG voltage is 3 V, and the pinning voltage is −6 V, and the low and high voltages of the SG are respectively -6 V and -3 V,

b) from the modulation function of SG, the channel potential is −3.73 V at an upstream SG and −1.78 V at a downstream SG,

c) from Figure 3a, the potentials of upstream and downstream FGs are interpolated. Then, the amplitude of FG is calculated as 1.35 V.

In Figure 3b, the estimated potential values are compared with those calculated by a potential simulation with the gate voltages. The errors range from 0.9% to 13.8%, proving the high efficiency of the proposed simple estimation method of the gate voltages.

(3) Combination of the charge guide pipe and the branching channel

Due to the combination of the guide pipe and the hexagonal gate, electron routes are classified into two parts, as shown in Figure 4:

a) from the upstream SGs to GG: there are three representative

Figure 3. Potential profiles to transfer electrons from an upstream (low-voltage) SG to a collecting FD (FDC): (**a**) a conceptual explanation for estimating gate voltages; (**b**) potential profiles calculated with the proposed systematic estimation procedure.

Figure 4. Equivalent travel routes of signal electrons: (**a**) the combination of the GP and branching channel, (**b**) three representative routes from upstream (low-voltage) SGs to a GG, coded with three colors, (**c**) three representative routes from a GG to an FDC.

Figure 5. An example of local potential adjustments from GG to FD_{21} (downstream green route R^E in Figure 4**c**): (**a-1**), a 2D planar channel potential on the front side before the adjustment, and a route on which the potential is evaluated; (**a-2**): the potentials before and after the modification;

(**b-1**) and (**b-2**), phosphorus masks are shown with green before and after the modification; (**c-1**) and (**c-2**), enlarged figures of the local potentials.

Table 1. Travel times from the center of GG to FD_C before and after detailed modification of a phosphorus mask: electrons start from 1.0 μm above the front side at the center of the pixel.

routes R_A, R_B, and R_C for electrons to converge to GG, as colorcoded in Figure 4b; for example, the green routes from $SG₂₁$ (R_B), SG₃₂, SG₅₁ and SG₆₂ to GG are equivalent, as all these routes start from the corner of the guide gate, where the indices of the gates are shown on FDs in Figure 4a, and

b) from GG to FDc through an FG and an SG downstream: there are three representative routes RD, RE, and R^F for the collected electrons to the verge, as shown in Figure 4c.

The combination causes local potential barriers. Therefore, the design needs to be modified by adjusting a channel mask and the voltage amplitudes of the gates to eliminate the barriers and equalize the travel times of electrons running through different channels, as shown in Figure 5. Table 1 shows the balance of the arrival times of electrons through various channels.

(4) Overall performance

At first, the potential is simulated for the whole structure. Then, a Monte Carlo (MC) simulation is used to measure the temporal resolution from the backside to an FD_C.

Figure 6 shows example trajectories of the signal electrons generated with MC simulations for the modified design. Light is perpendicularly applied to the backside. Table 2 shows the overall performance of the sensor. The sensor has a frame rate of 2.5 Gfps with a frame count of 12. The frame count can increase to 48 frames if a macro-pixel design is applied to four adjacent pixels. When a memory chip is stacked with the sensor chip, the frame count is increased to 100 to 1,000 frames.

Figure 6. Trajectories of signal electrons generated with MC simulations (**a**) trajectories of signal electrons, (**b**) examples of unusual trajectories; A and B take extraordinary long travel times, C moves to a waiting FDw, (**c**) travel times of A, B, and C vs. travel distances from the generation sites to FDs.

3. Sensor Operation

Two operation schemes are proposed.

(1) The burst imaging and image signal accumulation modes, shown in Figure 7: the collecting gates work in turn to transfer electrons to 12 FDs. We can also accumulate signals by repeating the image capturing process for weak incident light from reproducible events. Theoretically, noiseless ultrafast imaging is possible, especially with system cooling.

(2) Short continuous imaging, shown in Figure 8: signal electron packets stored in the FDs are continuously read out to memory elements in a stacked memory chip in turn. The signal transfer rate from each FD is 1/12 of that for image sensors with a single FD, which theoretically decreases the transfer noise by $1/\sqrt{12}$.

4. Temporal Crosstalk by Dynamic Simulation

The temporal crosstalk of the sensor is analyzed by dynamic simulation of electrons with varying voltages applied to collecting gates in the burst imaging mode. Figure 9 shows the results. The first row illustrates the timing map of the branching gates. The second row shows the collection rates for each FD as a function of time, where the collection rate is the ratio of electrons arriving at an FD_C to the total generated electrons. The solid and dashed curves represent the responses when square voltages are applied without and with RC delay τ . The frame interval for the collecting gates is 1 ns. We assume that the frame interval is 3τ .

(1) In the ideal case (square waves), solid curves show that more than 80% of generated electrons are collected with 10% of the temporal crosstalk.

(2) In the practical case (with RC delay), dashed curves show that the response is close to that in the ideal case but reveal some differences:

- the response in the practical case shifts to the right by about 0.125 ns,

- the maximum collection rate is slightly lower than 80%, and

- the head of the distribution is about 3% and lasts for 0.5 ns.

5**. Concluding Remarks**

A branching gate image sensor is proposed, and its fundamental performance is evaluated by potential and MC simulations. The sensor is composed of the upper narrow square PD and the lower diffusion layer with the branching gates. First, the PD and the branching gates are separately analyzed, and then the performance of the combined structure is evaluated. The major contributions are as follows:

- (1) there is an optimum concentration of the Boron implantation along the PD wall, which balances the suppression of the collision rate of electrons to the wall vs. the increase of the frame rate,
- (2) a design procedure of the branching gates is proposed, in which

the overall horizontal potential is linearized, and then the resultant local potential barriers are adjusted, and

(3) the sensor operates at a temporal resolution of about 400 ps with a frame count of 12 frames.

In the near future, when a memory chip is attached to the sensor chip, the frame count can be increased to more than 100 frames.

Figure 7. The diagram of Hanabi with the one-stage branching in the burst imaging mode. In the capturing process, FGs can repeat the operation to accumulate the signals. After completing the process, all signals at FDs are transferred to the stacked memory chip.

References

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Figure 8. The diagram of Hanabi with the one-stage branching in the continuous imaging mode. The read-out circuit at FD1 $(RO₁)$ operates simultaneously with the FG₁ to transfer collected electrons to the stacked memory chip. The speed of RO in this diagram is 3 times slower than that of FG.

Figure 9. The collection rates^{*} at the floating diffusions in the burst mode. The first row shows the operation scheme. The second row and the third row show the responses of FDs when square-wave voltages and RC voltages are applied, respectively. * collection rate: the rate that electrons arrive at the collecting floating diffusion.