Threshold Uniformity Improvement in 1b QIS Readout Circuit

Zhaoyang Yin[1,2] (Student), Jiaju Ma[2], Saleh Masoodian[2] and Eric R. Fossum[1]

[1]Thayer School of Engineering, Dartmouth College, Hanover, NH, USA,

[2]Gigajot Technology, Inc., Pasadena, CA USA

Contact: Zhaoyang.Yin.TH@dartmouth.edu

Abstract— **A new readout architecture for single-bit Quanta Image Sensor (QIS) consisting of an amplifier before a 1-bit quantizer to improve the threshold uniformity of the readout cluster is proposed in this paper.**

A 2048 × 1024 high-speed test chip was implemented with 45nm/65nm stacked backside illuminated (BSI) CMOS image sensor (CIS) process and tested. According to the measured D-log-H results, a good threshold uniformity in the range of 0.3 to 0.8 e- for all readout clusters is demonstrated at 500 frame per second (fps) equivalent timing with 68 mW power consumption. A coarse photon counting histogram (PCH) is obtained by sweeping quantizer threshold, showing 0.35e- r.m.s. read noise (including jot and readout circuit noise).

I. INTRODUCTION

The concept of QIS was first introduced in 2005 as a paradigm shift to take advantage of shrinking pixel sizes [1]. The small pixels in a QIS are called jots and have deep sub-diffraction-limit (SDL) pitch, small full-well capacity (FWC) and deep sub-electron read noise (e.g., < 0.6 μm, 100 e-, and < 0.3 e- r.m.s. respectively). Many efforts have been made to improve the jot performance, including increasing conversion gain (CG) and reducing readout noise [2] [3].

Besides the jot design, another challenge in realizing the QIS concept is implementing the high-speed, low-noise and low-power readout circuitry. A 1-Mjot photon-counting 1b QIS using charge-transfer amplifier (CTA)-based quantizer was designed with cluster-parallel architecture in a 3D stacked process [4]. The quantizer based on CTA readout circuits had significant threshold non-uniformity, likely due to the fluctuation of the common-mode voltage of the jot outputs. As a result, the sensor D-log H characteristics had extreme jot-to-jot variation. A complete redesign of the whole readout circuit is presented in this work as an attempt to address this challenge.

In this paper, a new architecture for 1-bit readout circuits is proposed. A capacitive transimpedance amplifier (CTIA) is added before the quantizer to guarantee the stability of the common-mode voltage of the input signals. To remove the offset caused by the CTIA, a correlated double sampling (CDS) block is utilized to store two signals, one for the reset voltage of the CTIA and the other for the amplified difference between the jot reset signal and exposure signal. The capacitors in the CDS block are large enough to ensure the kT/C noise incurred in the sample and hold process is negligible when compared to the total temporal noise. Although the introduction of the CTIA helps to stabilize the threshold across all of the readout clusters, it results in high power consumption. A pipeline operation mode is also proposed to reduce the power consumption of the CTIA. The CDS block stores two sequential output signals and one is used by the quantizer while the other is being sampled in ping-pong fashion. Thus, the CTIA and quantizer work at the same time. The D-log-H characterization is used to evaluate the performance of the readout cluster [5]. The experimental results show the 1b QIS readout circuits reach 0.5 e- threshold and a good threshold uniformity in the range of 0.3 to 0.8 e- across the whole array is demonstrated, providing a meaningful guidance for the future design of single-bit, QIS devices.

II. SENSOR ARCHITECTURE

The QIS was implemented in a TSMC 45nm/65nm stacked BSI CIS process and the chip area is 6 mm × 3 mm. A photo of the packaged die is shown in Fig. 1. The sensor is designed in a cluster-parallel architecture and includes two jot arrays with different pitch sizes— 1.1um and 4.4um, using the same readout circuit design. The characterization results presented in this paper are mainly focused on the 2048x1024 1.1um jot array. A block diagram of the sensor is depicted in Fig. 2. The readout architecture was improved by the addition of a CTIA with 10x gain before a quantizer to guarantee that the common-mode voltage of the input signals to the quantizer is in an acceptable range. Fig. 3 shows the schematic of the readout architecture. The CTIA and quantizer work in a pipeline mode to reduce the power consumption of the CTIA, the output of which is fed to a CDS block. There are two pairs of capacitors in the block to realize the pipeline operation. One pair stores the current output of the CTIA, and the other pair stores the previous outputs of the CTIA which are fed to the quantizer. The power supplies of the CTIA and quantizer are both 1.2 V.

III. EXPERIMENTAL RESULTS

The main purpose of this paper is to redesign the readout circuitry and improve the threshold uniformity. Thus, mainly the readout circuity testing results are reported here.

The 2Mjot sensor dissipates 68 mW including I/O at full speed, 500 fps. The readout chain variation was first verified at 500 fps, with the jot reset gates always on, keeping the input of the readout chain constant. The output density of the quantizer was measured by sweeping the threshold voltage over the equivalent range from -1.5 e- to +1.5 e-, calibrated from simulation results. Twenty readout clusters were measured, each with 10k samples of the same jot within that cluster. A bit density (due to readout noise) was determined for each cluster, and the standard deviation of the 20 cluster bit densities for each threshold is presented in Fig. 4 as a function of threshold voltage. The standard deviation of the readout chain is about 3.2% in the central region for this statistical measurement.

The D-log-H characteristic of a single-bit QIS is a useful tool for evaluating uniformity as well as proving true single-electron sensitivity. For low light levels, the higher read noise, the larger bit density. Fig. 5 shows the theoretical D-log-H curve for a single-bit QIS with 0.35 e- rms read noise and various quantizer threshold levels [5]. The distribution becomes narrower and bit density smaller at lower exposures with higher threshold. Fig. 6 shows the measured D-log-H curve from the 2Mjot sensor for 20 readout clusters. Compared with Fig. 5, we estimate a variation of about 0.5 +/- 0.15 e- in threshold for the measured clusters.

To verify the threshold uniformity of the whole array, D-log-H curves from the 2Mjot sensor for all the readout clusters were measured and are depicted in Fig. 7. The spread of the D-log-H curves is larger than that in Fig. 6. Compared with Fig. 5, the thresholds of the different clusters can be estimated, and the range of all clusters' thresholds is from 0.3 to 0.8 e-. To show the variation of all clusters more clearly, Fig. 8 shows a map of all cluster bit densities at H = 10^{-3} of the D-log-H curves. From the figure, no clear trend can be found, meaning the variation for all clusters is uniform. The bit density average of each column and row are both calculated, shown in Fig. 9. A trend can be seen for column average in Fig. 9 (a) but still no trend is shown for row average. This is probably caused by the distribution of three CTIA power supply pads, located in the top, left and bottom of the cluster's array.

The PCH is another useful tool for characterizing the performance of the QIS [6]. The probability of a jot outputting voltage U after exposure H at read noise u_n in a PCH graph is:

$$P(U) = \sum_{k=0}^{\infty} \frac{1}{u_n \sqrt{2\pi}} \exp(\frac{-(U-k)^2}{2u_n^2}) \frac{e^{-H} H^k}{k!} \quad (1)$$

In this work, another method is used to acquire a PCH instead of directly measuring the jot output [7]. For a fixed exposure H and a fixed readout circuitry threshold, the output bit density of the quantizer is a single point in the cumulative density function (CDF) of the probability in equation (1). Therefore, if the threshold is swept at a fixed H to get enough data points, a whole CDF curve can be recovered. The PCH curve can be obtained by finding the numerical derivative of the CDF curve. Fig. 10 (a) shows the measured raw CDF. For each point in the CDF curve, 10k samples of the same jot were measured. Due to the nonlinearity in the quantizer threshold range, there is a large deviation between the measured CDF and theoretical CDF (red curve, $H = 2$ and read noise = 0.35 e-) in both low and high threshold, U_{th}, region. Thus, a calibration is applied to the measured CDF curve: step 1, calibrate the low U_{th} region by adjusting the steps of U_{th} in the left side globally; step 2, calibrate the high U_{th} region by adjusting the steps of U_{th} in the right side globally. After the calibration, the measured CDF in Fig. 10 (b) matches the theoretical model better. Fig. 11 shows recovered PCHs from the raw and calibrated CDFs. The measured raw PCH coarsely matches with the theoretical PCH (red curve, $H = 2$ and read noise = 0.35 e-). After the calibration, the matching looks better but the measured PCH is not smooth enough due to the threshold nonlinearity. In addition, PCH @ $H = 1$ is measured to verify the methodology, as shown in Fig. 12. The calibrated PCH and theoretical PCH match despite not being smooth.

A 2048 × 1024 high-speed single-bit QIS test chip for improving readout cluster uniformity was implemented and tested. A good threshold uniformity in the range of 0.3 to 0.8 e- extracted from measured D-log-H results for all readout clusters is demonstrated.

IV. ACKNOWLEDGMENTS

V. REFERENCES

[1] E. R. Fossum, What to do with sub-diffraction-limit (SDL) pixels? —A proposal for a gigapixel digital film sensor (DFS). In IEEE Workshop on CCDs and Adv. Image Sensors, Karuizawa, Japan, June 9 – 11, 2005.

[2] J. Ma, et al., A 0.19e- rms Read Noise 16.7Mpixel Stacked Quanta Image Sensor with 1.1μm-Pitch Backside Illuminated Pixels. *IEEE Electron Device Letters*, 2021, 891-894.

[3] J. Ma, et al., Photon-number-resolving megajot image sensor at room temperature without avalanche gain. *Optica*, 2017, 1474-1481.

[4] S. Masoodian, et al., A 1Mjot 1040fps 0.22e- rms Stacked BSI Quanta Image Sensor with Cluster-Parallel Readout. In Int. Image Sensor Workshop, Hiroshima, Japan, May 30 – June 2, 2017.

[5] E. R. Fossum, Paper in progress.

[6] D. Starkey, et al., Determining conversion gain and read noise using a photon-counting histogram method for deep sub-electron read noise image sensors. *IEEE J. Electron Devices Soc.*, 2016, 129-135.

[7] D. Starkey, et al., A Novel Threshold Calibration Methodology for Quanta Image Sensors (QIS). In Int. Image Sensor Workshop, Snowbird, USA, June 23 – 27, 2019.
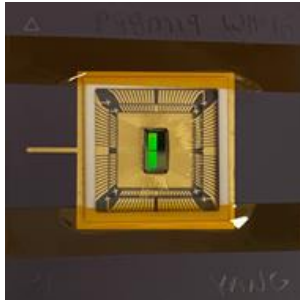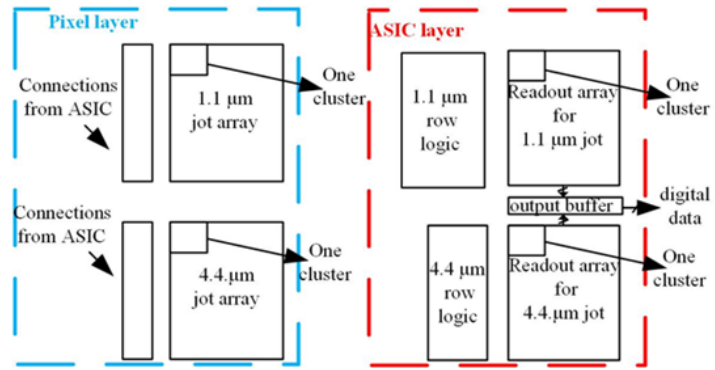
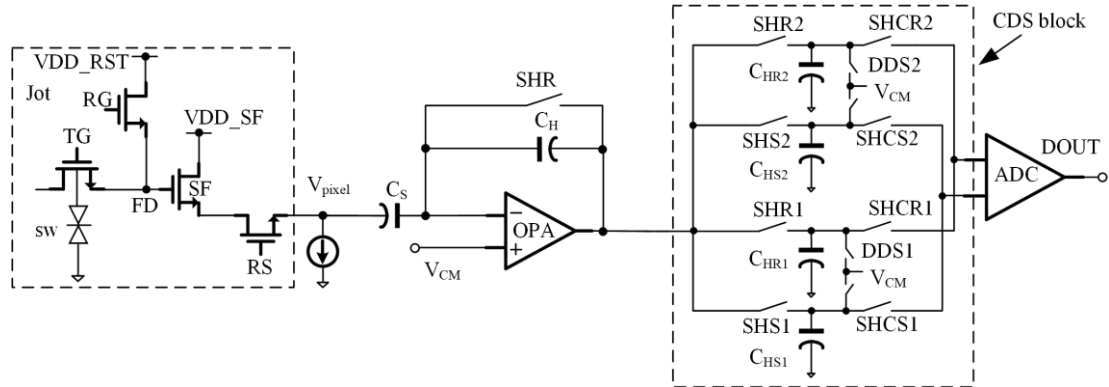Fig. 1. QIS chip.

Fig. 2. Diagram of the sensor.

Fig. 3. Schematic of the readout signal chain.
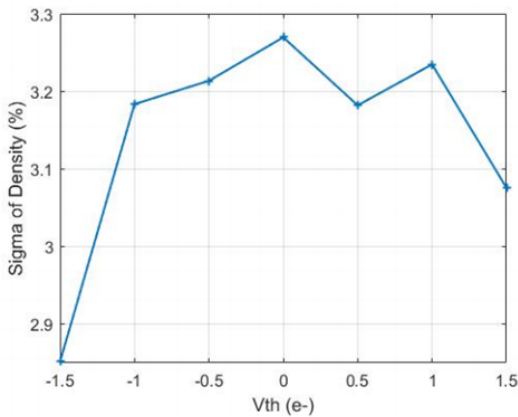
Fig. 4. Variation of readout chain using statistical approach from measurements.
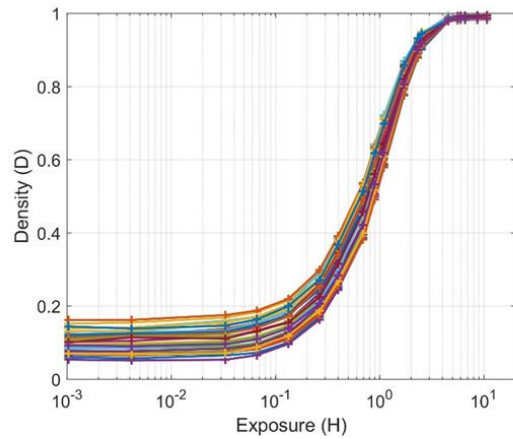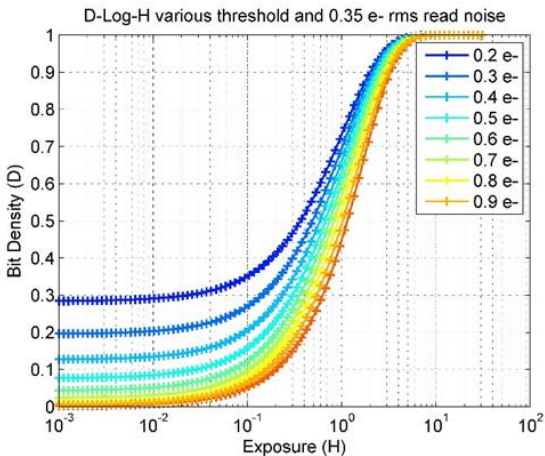

Fig. 5. Theoretical bit density vs. exposure for different thresholds (input-electron referred) with 0.35e- rms read noise.

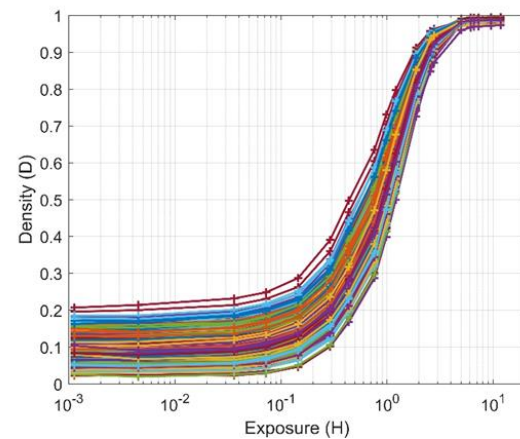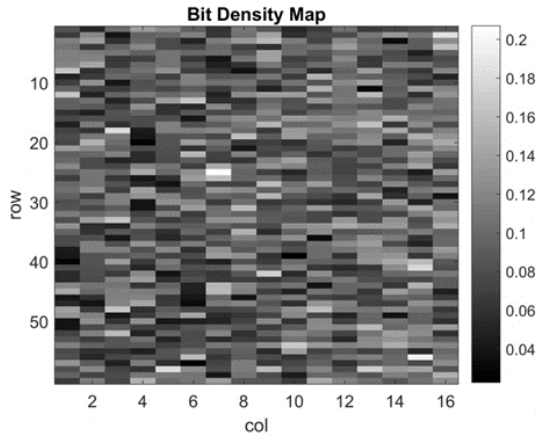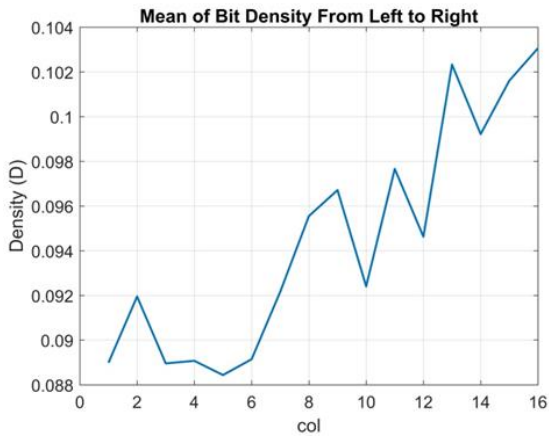Fig. 6. Measured D-log-H for different clusters, demonstrating good uniformity of about 0.5 +/- 0.15 e- in threshold.

Fig. 7. Measured D-log-H for all clusters, demonstrating good uniformity of threshold from 0.3 to 0.8 e-.

Fig. 8. Bit density map for all clusters at H = 10⁻³.

(a) column average
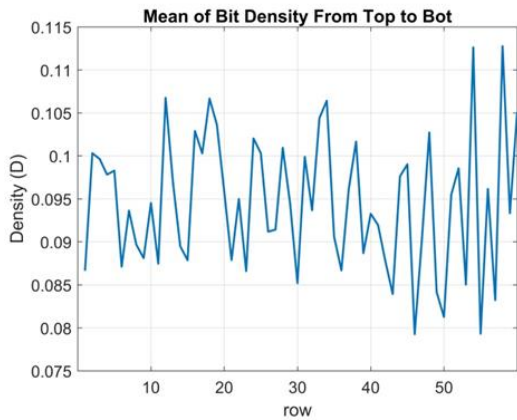
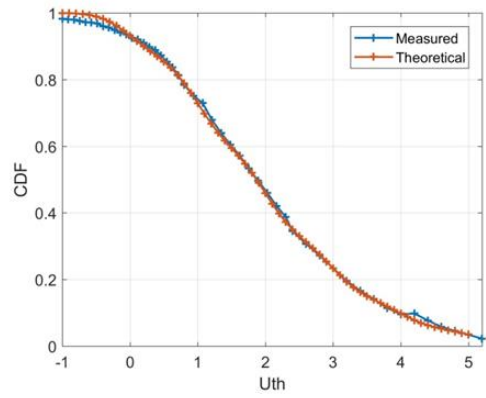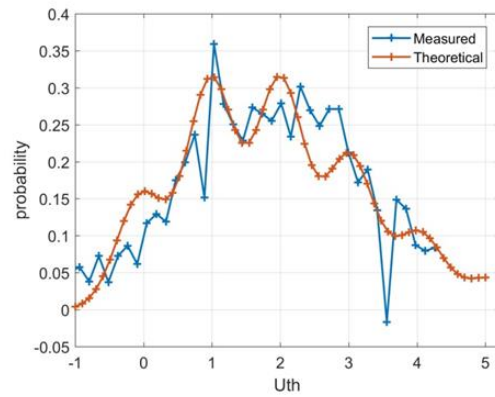

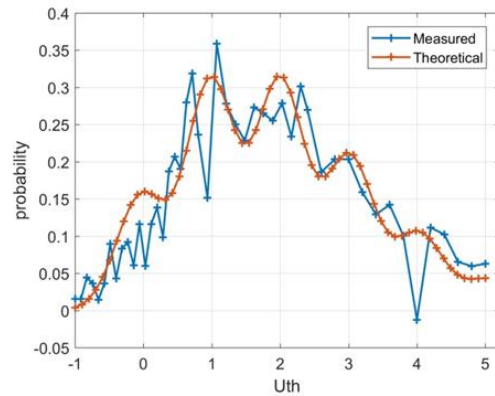(b) row average
Fig. 9. Average bit densities.
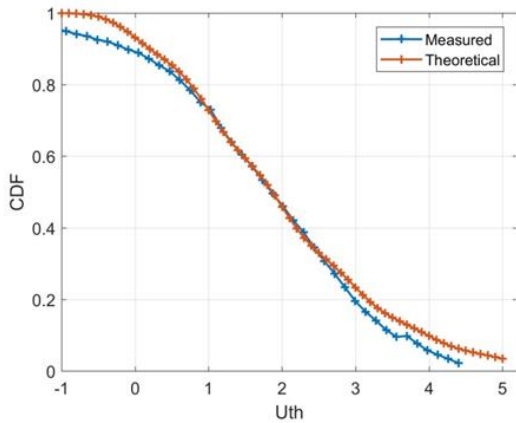
(a) raw CDF

(b) calibrated CDF; red curve is the theoretical CDF @ $H = 2$, read noise 0.35 e-
Fig. 10. Measured CDF by sweeping quantizer threshold.

(a) raw PCH

(b) PCH from calibrated CDF; red curve is the theoretical PCH @ $H = 2$, read noise 0.35 e-
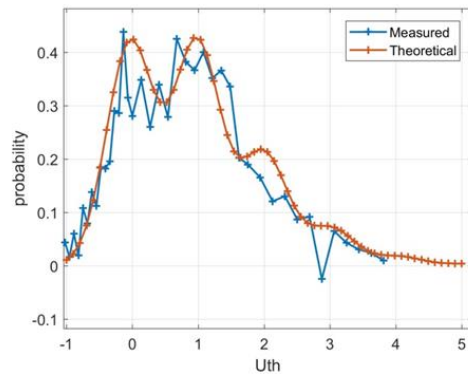Fig. 11. Recovered PCH using numerical differentiation.

Fig. 12. Recovered PCH using numerical differentiation after calibration. The red curve is the theoretical PCH @ $H = 1$, 0.35 e- read noise.