A 40/22nm 200MP Stacked CMOS Image Sensor with 0.61µm Pixel

Masayuki Uchiyama[1], Geunsook Park[1], Sangjoo Lee[1], Tomoyasu Tate[1], Masashi Minagawa[2], Shino Shimoyamada[2], Zhiqiang Lin[1], King W. Yeung[1], Lien Tu[1], Wu-Zang Yang[3], Alan Chih-Wei Hsiung[1], Vincent C. Venezia[1], Lindsay A. Grant[1]

[1]OmniVision Technologies, Santa Clara, CA 95054, USA. [2]OmniVision Technologies Japan, Kanagawa, Japan. [3]OmniVision Technologies Taiwan, Hsinchu, Taiwan.
Tel: +1-408-567-3000, Email: masayuki.uchiyama@ovt.com

***Abstract*—**We developed a new 40/22nm stacked 200 mega-pixel CMOS image sensor (CIS) with a 0.61µm pixel. By using a 22nm logic wafer process node instead of 40nm, digital power consumption was reduced by half while keeping the same clock frequency, and the full high definition (FHD) frame rate was increased from 240fps to 480fps. In this work, we demonstrate a new source follower (SF) transistor architecture with 63% higher SF transconductance (G_m) compared with our former 0.7µm pixel. A full well capacity (FWC) of 5.0ke- was achieved without lag or blooming, with better white pixel (WP) performance compared to the 0.7µm pixel. We demonstrate a 0.61µm quad photodiode (QPD) structure capable of achieving comparable quantum efficiency (QE) performance to 0.7µm QPD in the visible light range.

I. INTRODUCTION

Due to efforts in improving the image quality of multi-camera mobile devices, the demand for high-resolution and small pixel pitch image sensors have been steadily increasing [1]. Despite the pixel pitch scaling below the visible light diffraction limit, better image quality continues to be achieved due to progressive improvements in image signal processing [2].

High-resolution image sensors require lower power consumption and faster read-out speed, as the sensor must manage a large number of pixels at the same time. The wafer stacking process is applied in high-resolution CIS, where pixel and read-out circuitry are implemented in the pixel and logic wafers, respectively, thus allowing each wafer process to be optimized for its own purpose [3]. Lower power consumption and faster read-out can be achieved by adopting advanced process nodes in the logic wafer without impacting the pixel wafer. In addition, more image signal processor functions, such as pixel binning mode or switchable conversion gain (SCG), can be implemented in the logic wafer in smaller area with lower power consumption by adopting advanced process nodes.

Furthermore, small pixel pitch requires dimension shrinkage of the SF transistor and photodiode. A narrower SF transistor width leads to a smaller G_m, which is an important parameter for read-out speed, especially in high-resolution image sensors. In high-resolution image sensors, the bit-line for each pixel array column becomes longer, leading to longer bit-line settling time, resulting in lower read-out speed. The time constant, τ, for the bit-line can be expressed as $\tau = RC = (1/G_m + R_{load})C$, where R_{load} and C are loading resistance and parasitic capacitance of the bit-line, respectively. From the expression, it can be seen that τ is inversely proportional to G_m.

The smaller photodiode size degrades FWC and dark characteristics. To obtain higher FWC, both n-type ion-implantation dose of the photodiode and p-type ion-implantation dose at the isolation between photodiodes must be increased to achieve reasonable isolation potential barriers. However, increased n-type/p-type ion-implantation dose creates high electric fields, which degrade dark current and WP through the defective photodiode silicon surface [4]. Therefore, design of smaller photodiodes requires both n-type/p-type ion-implantation dose tuning and silicon surface defect improvement. In this work, we present a new CIS that addresses above mentioned issues relating to high-resolution and small pixel pitch image sensor.

II. PIXEL ARCHITECTURE AND TECHNOLOGY

Figure 1 shows a block diagram and cross-section of the sensor, which uses OmniVision Gen2 stacking technology [3,5,6]. A CIS-dedicated 40nm process node is adopted in the sensor wafer. In the logic wafer, a 22nm process node is newly adopted instead of the 40nm process node used in our previous small pixel stacking sensors [5,6]. Analog and digital circuitries were designed and optimized for the 22nm process node, achieving lower power consumption and higher read-out speed compared to 40nm process node.

The pixel array size is 200 mega-pixel (16384(H) x 12288(V)), with an optical format of 1/1.28" and a pixel pitch of 0.61µm. A 2x4 shared architecture is adopted, as shown in the circuit schematic in Figure 2.

Figure 3 shows the pixel transistor layout comparison between a conventional and the new layout used in this work. Each transistor is isolated by shallow trench isolation (STI). In the new layout, two SFs are connected in parallel by metal wiring, which provides a larger SF width. By adopting vertical transfer gate (VTG), the photodiode can be shifted to a deeper silicon region, allowing placement of transistors on the photodiode, providing more flexibility in transistor design [5,6]. The larger SF width by two SFs can improve G_m even in smaller pixel pitch, thus giving a reasonable bit-line time constant in the 200 mega-pixel CIS. We also adopted backside deep

trench isolation (BDTI) to isolate each pixel, improving optical cross talk. The combination of STI, VTG and BDTI allows independent layout optimizations for front side and backside silicon, making it suitable for small pixel development. Moreover, as shown in Figure 3, we can include an additional transistor, which can be used for SCG for high dynamic applications [6].

Figure 4 shows TCAD simulations of the sensor's photodiode potential profile in depth direction. The reduction of FWC by pixel pitch shrink was avoided by increasing n-type/p-type ion-implantation dose and optimizing potential profile. We can see the potential smoothly extends in depth to increase FWC without sacrificing lag or blooming. However the degradation of dark current or WP due to higher electric fields located at defective silicon surface is another concern, especially in BDTI interfaces where defects are created by the etching process. We adopted the latest BDTI process, leading to improved WP.

Due to smaller on-chip lens (OCL) fill factor, small pitch pixels suffer from significant QE degradation. QPD, or Quad-Bayer coding with 2x2 OCL, is a design which uses one OCL and the same color filter in a 2x2 pixel array, producing high-resolution and high dynamic range image sensors [7]. QPD is an important technology to improve QE for small pixel image sensors and was implemented in this work.

The following section demonstrates the performance of a new 40/22nm 200 mega-pixel CIS with 0.61μm pixel and implementing QPD, in comparison with a previous generation 0.7μm pixel image sensor.

III. EXPERIMENTAL RESULT

A 22nm process node enabled the reduction of digital power consumption by half while keeping the same clock frequency, and the increase of FHD frame rate from 240fps to 480fps compared to 40nm process node (Figure 5).

The 0.61μm pixel exhibits 63% SF G_m improvement compared to 0.7μm, achieving a reasonable bit-line constant in the 200 mega-pixel image sensor, as shown in Figure 6. Figure 7 shows the FWC trend with respect to pixel pitch. The filled circles and dotted line represent the FWC achieved by simple pixel area scaling, based on a 1.0μm pixel. The empty circles show data from our previous generation 0.8μm and 0.7μm technologies. It can be seen that 0.8μm and 0.7μm FWC are much higher than the value predicted by simple scaling; this enhancement was achieved by deep photodiode technology, in which potential was carefully designed in the deeper silicon region. We adopted the same technology, which we re-designed for 0.61μm, achieving 5.0ke- FWC without lag or blooming. As shown in Figure 8, the 0.61μm pixel WP histogram is improved compared with 0.7μm. Although we increased n-type/p-type ion-implantation dose, resulting in higher electric fields, our latest BDTI technology enabled WP improvement compared to the previous generation.

Figure 9 presents the QPD QE curve comparison between the 0.7μm and 0.61μm pixels. The overall QE performance is comparable to 0.7μm QPD in the visible light range, but some degradation is seen in the near infrared region. Finally, a sample image taken by this sensor is shown in Figure 10.

IV. CONCLUSION

We developed a new 40/22nm 200 mega-pixel stacked image sensor with 0.61μm pixel size. Table 1 shows the performance comparison between the 0.7μm and 0.61μm pixel. Digital power consumption was reduced by half and FHD frame rate was increased from 240fps to 480fps. We achieved 63% higher SF-G_m. FWC of 5.0ke- was achieved without lag or blooming with better WP performance compared with the 0.7μm pixel. We demonstrated comparable QPD QE performance to 0.7μm in the visible light range.

ACKNOWLEDGMENTS

We are grateful to Taiwan Semiconductor Manufacturing Company, Ltd. for chip fabrication and their technological support for both sensor and logic wafers to achieve 200 mega-pixel CIS with 0.61μm pixel.

REFERENCES

[1] Yeongheup Jang *et al.*, "A new PDAF correction method of CMOS image sensor with Nonacell and Super PD to improve image quality in binning mode", *IS&T International Symposium on Electronic Imaging*, pp. 220-1-220-4, 2021.
[2] Albert Theuwissen, "There's More to the Picture Than Meets the Eye*, and in the future it will only become more so", *International Solid-State Circuits Conference (ISSCC)*, pp. 30-35, 2021.
[3] Vincent C. Venezia *et al*., "Second Generation Small Pixel Technology Using Hybrid Bond Stacking", *Sensors*, vol. 18, pp. 667, 2018.
[4] JongEun Park *et al.*, "1/2.74-inch 32Mpixel-Prototype CMOS Image Sensor with 0.64μm Unit Pixels Separated by Full-Depth Deep-Trench Isolation", *International Solid-State Circuits Conference (ISSCC)*, pp. 122-124, 2021.
[5] Takuma Hasegawa *et al*., "A new 0.8μm CMOS image sensor with low RTS noise and high full well capacity", *International Image Sensor Workshop*, pp. 4-7, 2019.
[6] Y. Jay Jung *et al*., "A 64M CMOS Image Sensor using 0.7um pixel with high FWC and switchable conversion gain", *IEEE International Electron Devices Meeting (IEDM)*, pp.16.3.1-16.3.4, 2020.
[7] Tetuya Okawa *et al.*, "A 1/2inch 48M All PDAF CMOS Image Sensor Using 0.8μm Quad Bayer Coding 2x2OCL with 1.0lux Minimum AF Illuminance Level", *IEEE International Electron Devices Meeting (IEDM)*, pp.16.3.1-16.3.4, 2019.

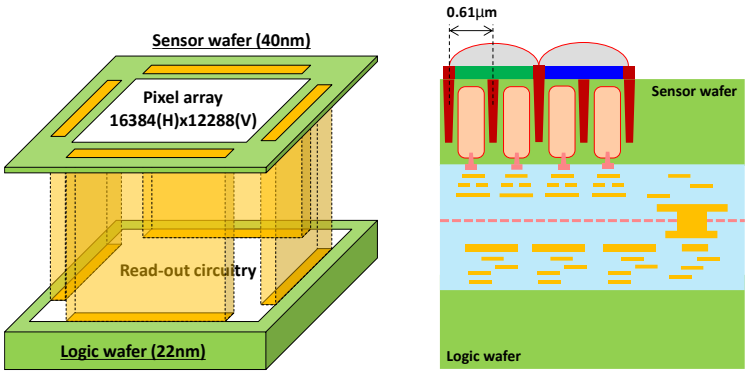

Figure 1: Block diagram and cross-section of the 0.61µm pixel.

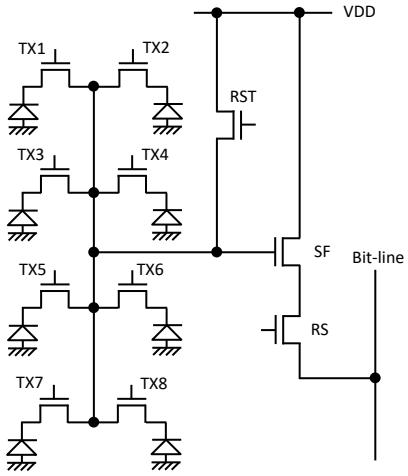

Figure 2: Circuit schematic of the 0.61µm pixel.

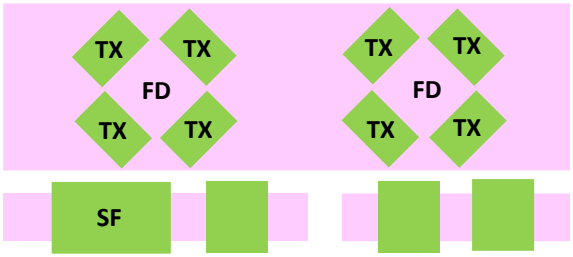

Fig. 3a: Conventional pixel layout.

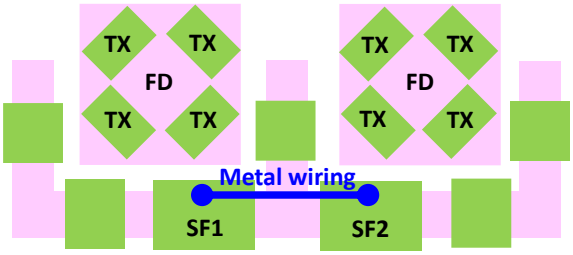

Figure 3b: New pixel layout.

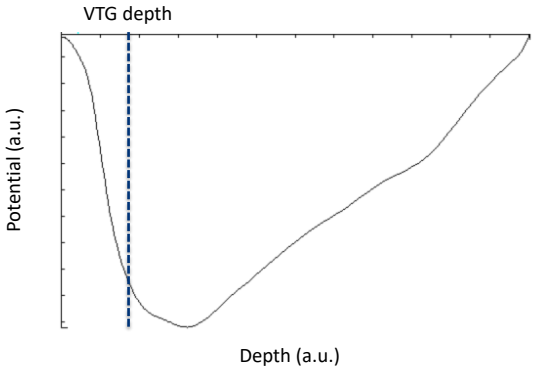

Figure 4: Photodiode potential profile of 0.61µm pixel simulated by TCAD.

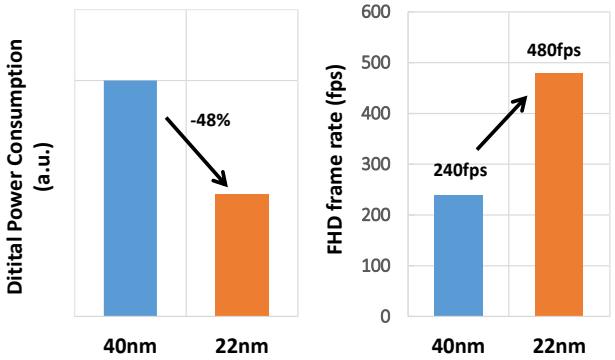

Figure 5: Digital power consumption and FHD frame rate comparison between 40nm and 22nm logic wafer process node.

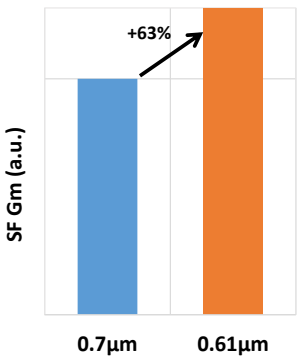

Figure 6: SF G_m comparison between 0.7µm and 0.61µm pixel.

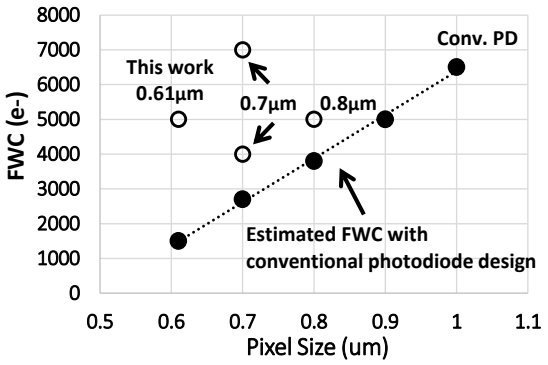

Figure 7: FWC trend with respect to pixel pitch. Filled circles and open circles show estimation and silicon result, respectively.

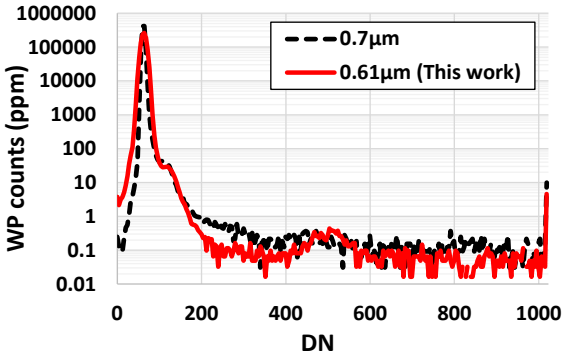

Figure 8: White pixel histogram comparison between 0.7µm and 0.61µm.

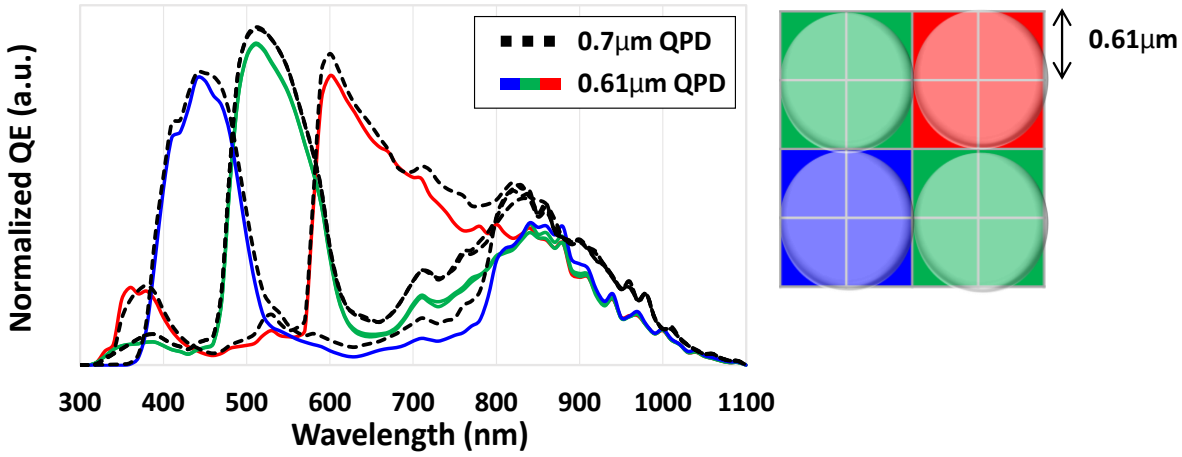

Figure 9: QE curve comparison between 0.7µm and 0.61µm QPD and QPD color filter and OCL structure.

Figure 10: Sample image of this sensor.

Items	Unit	0.7µm	0.61µm
Process node in sensor wafer	NA	40nm	40nm
Process node in logic wafer	NA	40nm	22nm
Digital power consumption	a.u.	1	0.52
FHD frame rate	fps	240	480
SF Gm	a.u.	1	1.63
FWC	e-	7K	5K
Lag	e-	<1	<1
Blooming	%	<1	<1
FPN noise @ 16x	e-	0.22	0.30
Total noise @ 16x	e-	1.20	1.60
RTS (>1mV)	ppm	19	10
WP @ 60C	ppm	40	26
DC @ 60C	e-/s	2.2	1.3

Table 1: Performance comparison between 0.7µm and 0.61µm pixel.