0.64μm-pitch CMOS Image Sensor with Low Leakage Current of Vertical Transfer Gate

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***Abstract*— As the pixel size is scaling down due to the market demand particularly of the mobile CMOS image sensor (CIS) market, the distance between a transfer gate (TG) transistor and a floating diffusion node (FD) is becoming smaller. Consequently, the leakage current at FD nodes by gate-induced drain leakage (GIDL) is a primary source of image defects such as multi-bit white spots particularly where FD nodes are shared for adaptive pixel-level gain control as well as sensitivity improvement at low illumination. In this work, vertically-etched TGs (VTGs) were integrated in a 0.64μm-pixel sensor for better charge transfer from photodiodes as well as smaller pixel area. We found that GIDL of VTGs mainly arises from trap-assisted tunneling (TAT) at the gate controlled FD junction diode with thermal activation. The leakage current exponentially increases with electric field at the drain node of VTGs, which was correlated with overlap capacitance (*Cov*) between VTG and FD. We were able to mitigate multi-bit white spot defects by optimizing the dry etch condition of VTGs and doping profiles of FD in order to minimize the chip-level variation of *Cov*.**

Keywords—CMOS Image Sensor, Transfer Gate Transistor, Gate-induced Drain Leakage, Trap-assisted tunneling.

I. Introduction

Recently, there is a strong drive for smaller pixel size of CMOS image sensors (CISs) in a mobile market. Simultaneously, improvement of pixel sensitivity at low illumination condition is required which leads to sharing more pixels i.e. sharing floating diffusion (FD) nodes over multiple pixels. [1] However, image sensors with such a shared structure are more susceptible to multi-bit white spot defects. In other words, all shared pixel would shine brightly even at a dark condition and it would result in poor dark image quality if one of shared pixels has leakage current directly flowing into FD nodes. For high mobility, most of CISs use n-type metal-oxide semiconductor (nMOS) transistors including switch transistors and source-follower (SF) amplifiers. The node distance between nMOS transfer gate (TG) transistors and n-type contact of TG drain nodes i.e. FD nodes as the pixel pitch decreases. Then the small distance between nodes enhances gate-induced drain leakage (GIDL) which is strongly associated with structural variations such as geometry of poly Si gates and doping profiles of drain nodes. It is known that GIDL current is exponentially increasing with the electric field (e-field) generated the drain nodes. Although FDs are formed as a lightly-doped drain (LDD), GIDL occurs severely when TGs are turned off at a negative bias to completely block any electron influx to photodiodes at dark condition. Another challenge is to suppress within-chip or within-wafer non-uniformity of leakage current at FD nodes, which is related to fabrication variation control. Such non-uniformity worsens not only the image quality but also the product yield.

In this work, we analyzed the leakage mechanisms of the GIDL at TGs and modeled the root cause of statistical GIDL generation. Then, we suggest optimal processes such as FD doping and dry etch in order to suppress the electric field as well as to make GIDL current less susceptible to process variations. We firmly believe that this work helps for CIS products with small pixels and proper image quality.

II. Device fabrication And GIDL Mechanism

In order to study dark leakage current from FD nodes, we fabricated a CIS chip with 0.64μm-pitch pixels where each photodiode is isolated by full-depth deep trench isolation (FDTI). [2] Each pixel has a vertically etched TG (VTG) in order to facilitate the charge transfer to the FD node from a photodiode which is formed into the depth direction along FDTIs. The VTG is normally turned off with a negative bias so that any electrons generated at the etched Si surface of the VTG channel do not move into the photodiode which otherwise generate a white pixel defects. Moreover, the sensor has a pixel-level adaptive gain control functionality achieved by sharing 4 FD nodes and placing serially connected two reset gate transistors. Because of 4-shared pixels, 4-bit white defects (WDs) occurs if one of the shared FD nodes has leakage current as shown in Figure 1a. In order to study relation between e-field and WDs, distances between the VTG gate and the FD contact were varied and multi-bit WDs were counted as shown in Figure 1b. The FD nodes were formed by two subsequent n-type doping steps, i.e. 1) LDD and 2) heavily doped n-type for metal contact. This metal node is connected to the gate of SFs. A Technology Computer Aided Design (TCAD) simulation shows that e-field

at the VTG drain node is inversely proportional to the distance between the VTG gate and the heavily-doped FD contact. Therefore, the increasing number of WDs is explained by e-field increase due the FD doping diffusion into Si under the VTG poly

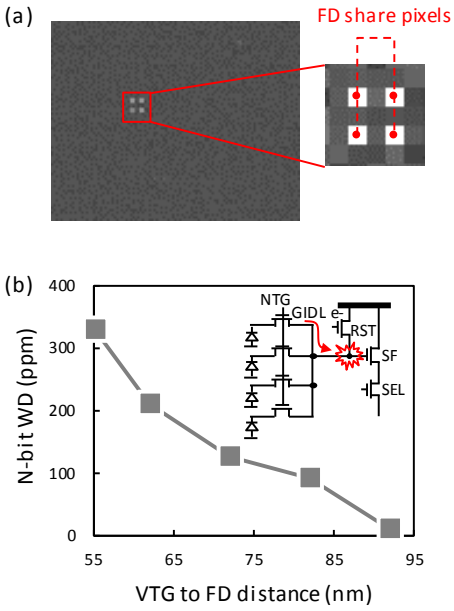

Figure 1. a) The image of white defect (WD) pixels in the fabricated 0.64μm-pixel and the schematic of the pixels sharing floating diffusion (FD) nodes. b) Multi-bit WD counts depending on the VTG to FD distances.

gate. Such high concentration of n-type doping under drain node under a negative bias increases the electron generation through band-to-band tunneling (BTBT) from the significant band bending near gate. As shown in Figure 2a, the gate-FD overlap region is similar to a pMOS transistor at a negative bias and electrons in the valence band of the VTG gate oxide interface are captured at the trap site in the bandgap. Then they tunnel into the conduction band to generate trap-assisted tunneling (TAT) current. BTBT current arises sharply at field above 1MV/cm e.g. donor doping of 2E18cm^{-3} with a reverse bias at 1V. [3] A TCAD simulation shows that relatively low FD doping concentration compared to typical heavily doped contact, the e-field is less than 1MV/cm. Nevertheless, BTBT can be enhanced even with lower e-field by interface traps at the TG channel through TAT.

The mechanism of the VTG GIDL was analyzed by measuring the gate-controlled FD junction diode in other words e-field at the FD node enhanced by the gate e-field, leakage current by electrical test on a wafer level. Figure 2b shows the current-voltage (*I-V*) curve at various temperatures of 298K, 333K, and 353K. Figure 2c shows the activation energy of leakage current at the VTG bias less than -1.5V. It corresponds to an half of silicon bandgap energy of around 0.5eV which is indicative of the TAT as the main leakage mechanism. Figure 2b shows that this is due to Fowler-Nordheim (F-N) tunneling current in the gate oxide and not a BTBT. [4]

Figure 3 shows the *I-V* characteristics of the gate-controlled junction diode varying the temperatures of the source node (FD) and the drain node (V_{PIX}) of the reset gate transistor. Since the doping concentration of the drain node of the reset transistor is almost the same as that of the general *n+* drain node, it appears that the mechanism of the GIDL current is BTBT generated at the drain node. It should be independent of temperature as

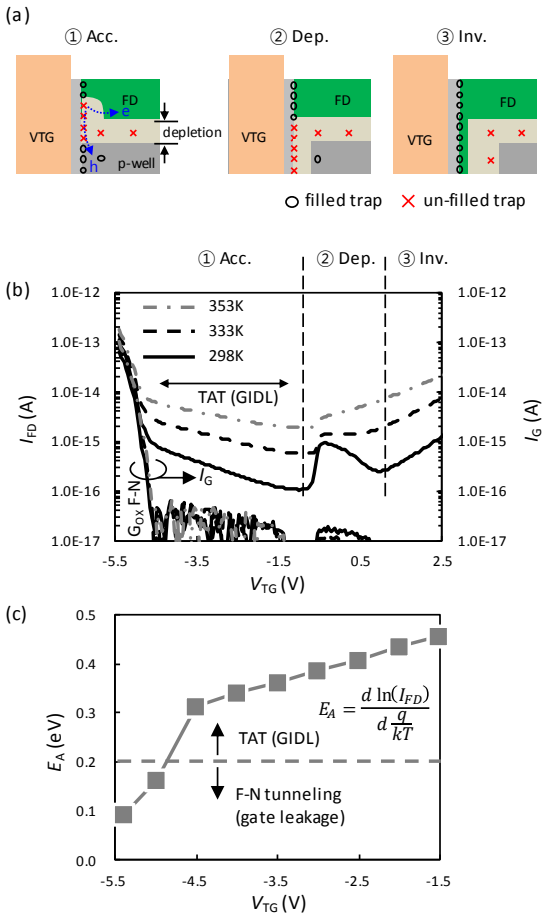

Figure 2. a) FD-body junction in the case of channel surface conditions 1) accumulation, 2) depletion, 3) inversion accompanied by VTG and FD overlap region depletion. b) *I-V* characteristics of gate-controlled FD junction diodes as a function of temperature. c) Activation energy as a function of VTG gate bias shows: 1) F-N tunneling of the gate oxide dominates at low gate bias below -4.5V 2) TAT dominates at gate bias higher than -4.5V.

shown in Figure 3(b). On the other hand, the leakage current is generated by TAT at the drain node of VTGs since the source node of the reset transistor has the same doping concentration as the FD node.

III. Results and Discussion

The GIDL current can be formulated as follows: [3]

$$I_{\mathrm{GIDL}} = A_{\mathrm{GIDL}} E_{n,\max}^2 e^{-B_{\mathrm{GIDL}}/E_{n,\max}} \qquad (1)$$

where A_{GIDL} and B_{GIDL} are the fitting parameters for which A_{GIDL} is proportional to the channel width W and $E_{n,max}$ is the maximum field in the GIDL region of the n+ drain occurring just below the oxide in the gate-drain overlap region. Since the GIDL current is exponentially proportional to the e-field in the gate-drain overlap region, the VTG GIDL current can be effectively enhanced by suppressing the e-field in the VTG and FD overlap region by reducing the FD doping amount. Figure 4 shows the results of the VTG GIDL experiment for two FD doping conditions. Figure 4a shows the experimental results of the relationship between the overlap region capacitance (C_{OV}) and the GIDL current in a VTG transistor according to the FD doping conditions. C_{OV} determines the e-field while GIDL increases exponentially with C_{OV}. It shows a higher C_{OV} value under high FD doping concentration, the same voltage must now drop across the narrower depletion region, resulting in a large e-field. Figure 4b is the result of matching the GIDL current with the multi-bit WD counts in the in-wafer level testing. They are in a good agreement.

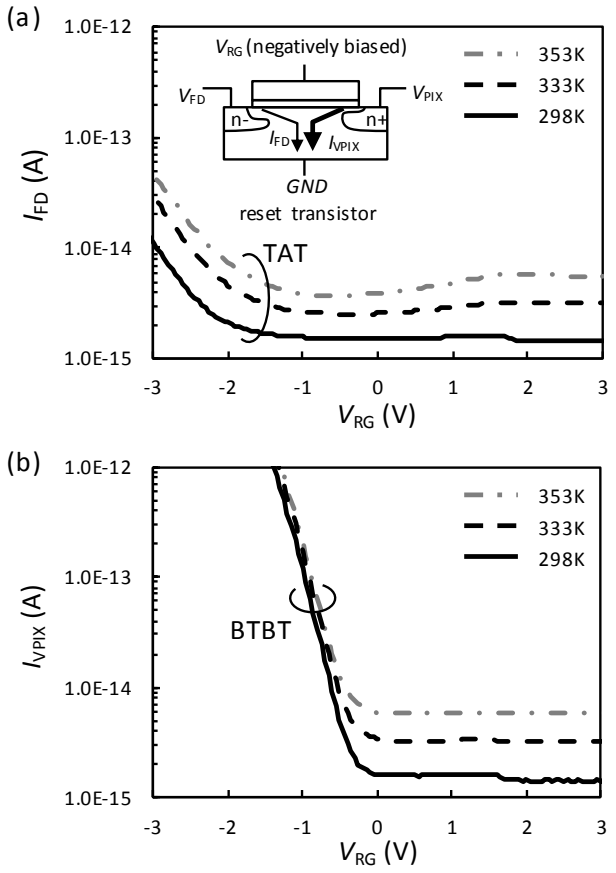

Figure 3. a) *I-V* characteristics of gate-controlled junction diode with different temperature conditions at source node (FD) and b) drain node (V_{PIX}) of reset transistor. Inset: Device structure of the reset transistor with negatively biased V_{RG} conditions for GIDL flowing conditions. The leakage mechanism of source node is TAT (less narrow depletion region) and the drain node is BTBT (narrower depletion region) with the different doping concentrations.

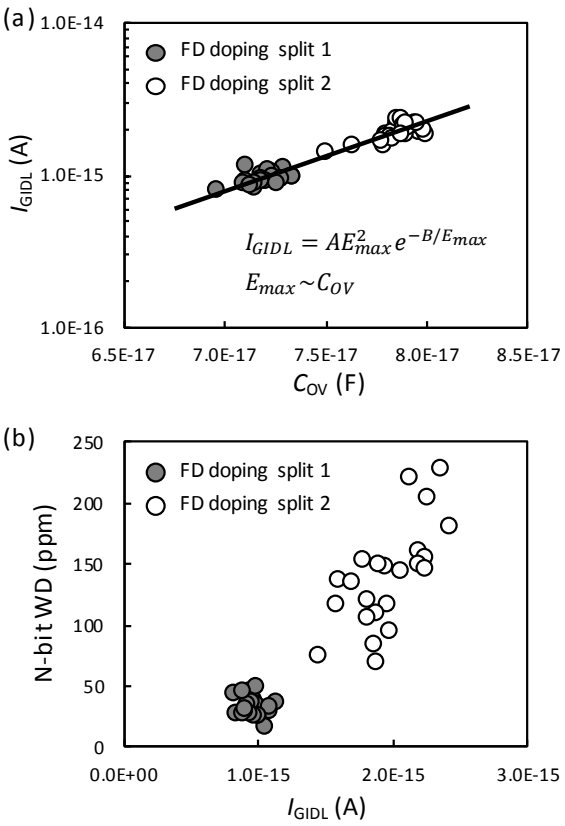

Figure 4. a) C_{OV}- GIDL characteristics and b) GIDL versus N-bit WD characteristics for FD conditions

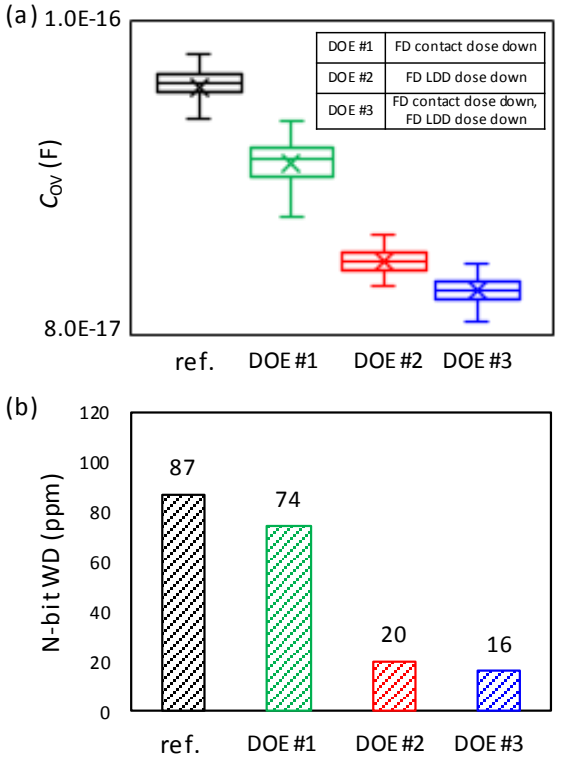

Figure 5. a) Statistical graph with FD doping conditions b) N-bit white pixels with FD doping conditions

In addition to the method of improving N-bit WD in the direction of lowering the e-field center value of the overlapping region of VTG and FD by reducing the FD doping amount, it is possible to improve the N-bit WD in ppm in the direction of improving the electric field distribution while leaving the center value as it is. [5] C_{OV} is a linear function of VTG to FD distance ($d_{VTG\text{-}FD}$) and GIDL current is an exponential function of $d_{VTG\text{-}FD}$. The GIDL of TEG shows the average value of one chip when the process variation of $d_{VTG\text{-}FD}$ is small, but when the variation is large, the GIDL current of the tail pixel can increase several digits, so it indicates the in-chip variation. Figure 6a shows the GCD results for two VTG dry etch conditions. In etching condition 2, the GIDL current is smaller than 1, and the GIDL increase slope with respect to the VTG voltage is about 1/2. Figure 6b shows the C_{OV} and GIDL curves, both etch conditions have the same C_{OV} range, indicating that the within-wafer distribution of both conditions is at the same level.

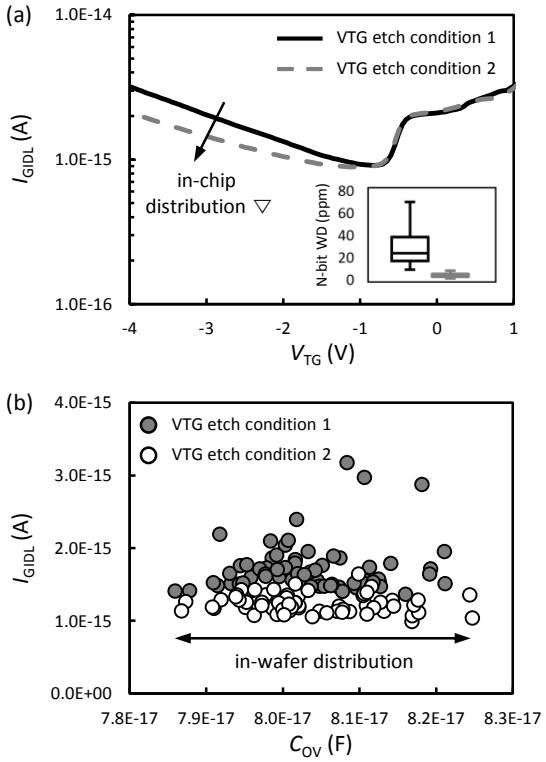

Figure 6. a) *I-V* characteristics of gate-controlled junction diode and b) VTG gate to FD overlap capacitance (C_{OV}) versus GIDL current with different VTG dry etch conditions.

IV. Conclusion

We conducted a study on mechanism of VTG GIDL leakage in order to improve multi-pixel white defects in 0.64-μm pixel. We found that the GIDL current is predominantly due to TAT leakage mechanism. Since the TAT mechanism is exponentially proportional to e-field, we have focused on how to reduce e-field at VTG such as reduction of ion implant doping dose to lower overlap capacitance at the FD nodes on VTG, which led to 80% improvement of multi-bit white defects. In addition, the e-field at the drain nodes of VTG is sensitive to distance between VTG channel and heavily n-type doped FD nodes and therefore it is important to improve the distance variation within a sensor chip to reduce a number of FD-shared multi-bit defects in the unit of ppm. We have developed an optimal etch condition to reduce VTG profile variation. As a result, C_{OV} in wafer level lower a number of pixels that show extremely high leakage current and we were able to improve by 80% in the multi-bit defects compared to the reference chip. We are convinced that this GIDL reduction is critical for better dark image quality particularly for small pixels.

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