Multi-Gate Source-Follower for Quanta Image Sensors (QIS)

Wei Deng (Student) and Eric R. Fossum

Thayer School of Engineering, Dartmouth College, Hanover, NH, USA

Contact: Wei.Deng.TH@dartmouth.edu

***Abstract*—A multi-gate source-follower (MGSF) is introduced to simultaneously reduce 1/f noise and increase pixel conversion gain. 1/f noise generally deteriorates as the SF size becomes smaller although the conversion gain benefits from the scaling. The MGSF can alter this tradeoff and make a low-noise high-conversion-gain QIS achievable. This work paves the way to further reduce the floating diffusion referred read noise in CMOS image sensors and QIS.**

I. Introduction

The Quanta Image Sensor (QIS) is a photon-counting image sensor with ultra-low read noise. The target for the input-referred read noise is below ~0.15e- rms [1], such that accurate single photoelectron counting can be performed. Although the reported read noise record from a single pixel is as low as 0.12e- rms at room temperature [2], the median noise of QIS is still at a level of 0.22e- rms. It is desired to have an array of jots with a median value of read noise below 0.15e- rms so that photon counting with a very low bit-error rate can be achieved across the whole array of jots.

Currently, the in-pixel source-follower (SF) 1/f noise dominates the read noise of QIS and most CMOS image sensors (CIS). Generally, the origin of MOSFET 1/f noise remains controversial and several well-known models such as the McWhorter number fluctuation model [3], Hooge mobility fluctuation model [4] or the Berkeley unified 1/f noise model [5] were developed based on different noise origin assumptions. We previously found that the mobility fluctuation model matches the best with the experimental data for a QIS sensor with small SF [6].

Generally, 1/f noise scales inversely with transistor gate area so that a SF with a larger gate area has a lower 1/f noise [7]. However, a larger area will lead to a larger gate parasitic capacitance, which will cause larger total FD parasitic capacitance and thus reduce the conversion gain (CG). To achieve a higher CG, a smaller gate area is desired. Due to this tradeoff between 1/f noise and CG, the input-referred read noise can only achieve a theoretical minimum level with an optimum SF size [6].

Future input-referred read noise reduction at the pixel level needs to alter this tradeoff. In this paper, an MGSF is designed and fabricated with the aim to increase the pixel conversion gain and reduce the 1/f noise simultaneously.

II. MGSF Design

The new MGSF can improve the tradeoff between 1/f noise and CG. The multi-gate SF consists of the SF modulation gate (MG), i.e., the FD-connected input gate, and dc-biased guard gates (GG). The guard gate is introduced to increase the total effective SF gate area for 1/f noise reduction while the SF modulation gate can be the minimum size allowed so that a higher CG is achieved simultaneously.

Three different configurations of the MGSF are explored. The guard gate of an MGSF can be placed closer to the source end (configuration version V1) or the drain end (V2). The MGSF can also have two guard gates while the modulation gate is placed in-between (V3). The parasitic capacitance between the SF drain/source and the guard gate will not contribute much to FD total capacitance since the modulation gate is separated from the guard gate. A conventional MOSFET SF with the same total gate area as V1 and V2 is included for baseline reference (V0 SF configuration).

The V0 SF and the three versions of MGSF are shown in Figure 1(a)(b)(c)(d), and the corresponding layout in Figure 1(e)(f)(g)(h). A 1x2 shared readout circuitry is used. The pump-gate jot and punch-through reset are implemented to further reduce parasitic capacitance [8].

Figure 2 shows the potential-well diagrams of the MGSFs in operation. As shown in Figure 2(b), the modulation gate is biased at a slightly lower voltage than the guard gate. The gap between MG and GG forms a potential well and is filled with charge carriers. The operation potential-well diagram of MGSF V2, V3 and V0 SF are shown in Figure 2(c), (d) and (a), respectively.

Figure 3 shows a TCAD simulation result from a jot with MGSF V2. When the transfer gate TG is pulsed, 1,140 e- was transferred from the photodiode storage well to the floating diffusion, causing an FD voltage drop of 0.82V (i.e., from 1.41V to 0.59V). The extracted FD-referred CG is thus 716μV/e-. A summary of extraction results from all types of SF devices is shown in Table 1. The extracted FD-referred CG of MGSFs (e.g., 699.7μV/e- for V1, 716.2μV/e- for V2 and 708.7μV/e- for V3) is about 20% higher than that of the V0 SF (e.g., 579.1μV/e-), since the size of the MGSF modulation gate is smaller than the V0 SF gate.

The QIS test chip is shown in Figure 4. Figure 5 shows the schematic of the readout chain. The output of the jot is connected to a correlated double sampling

(CDS) circuit. A programmable gain amplifier (PGA) is utilized to amplify the signal. The signal is then sent off-chip and digitized by an analog-to-digital converter (ADC). During the testing, the gain of the PGA is set to be 10.

The 1/f noise spectrum measurement timing diagram is shown in Figure 6. The jot will be reset first by turning on both the transfer gate and the reset gate. Then the PGA continuously samples the jot output signal for 0.25s with a sampling period of 0.5μs. The data is digitized by an off-chip ADC and stored in a PC memory. The fast Fourier transform (FFT) algorithm was used to convert the data from the time domain to the frequency domain to form the noise spectrum.

III. Characterization Results

MGSF devices are implemented in a TSMC 45/65nm stacked backside-illuminated (BSI) CIS baseline process. The pixel using a shared readout has a pitch of 2.2μm×1.1μm. Punch-through-reset (PTR) operation was expected but the PTR structure was found to be always "on" with reset drain shorted to the SF gate, perhaps due to implant changes. Measurement of read noise by the photon-counting histogram technique [9] was not possible. But, the implementation defect meant we could directly access the SF gate for voltage-domain measurements. The gain and noise for all types of MGSFs were measured. A total of 32 devices of each type were measured.

Figure 7 shows the measured average of transfer curves from 32 SFs of each type. The guard gate is biased at a DC voltage of 2.5V for MGSF. The conventional MOSFET SF and the MGSF configurations show similar transfer characteristics. Although the gain of the V0 SF is slightly higher (e.g., 0.78), the gain of the MGSFs is similar (0.76 for V1, V3 and 0.77 for V2). The gain generally matches the TCAD simulation result although it is 9% smaller, possibly due to the discrepancy between the process flow used in simulation and fabrication. The extracted SF gain and the measured gain are shown in Table 1.

The input-referred noise power spectra for 4 types of SFs are shown in Figure 8. Each curve is an average of the results from 32 devices. Figure 8 shows that the MGSFs have lower noise compared to the V0 SF when the guard gate is biased at 1.5V. This indicates that adding the guard gate helps to reduce the overall 1/f noise even though the modulation SF gate is smaller in area in the MGSF versions – a surprising result.

Also noteworthy is the apparent change in exponent α in the $1/f^{\alpha}$ dependence where α is close to unity in the V2 and V3 MGSF configurations, but $\alpha \approx 1.5$ for the "normal" V0 SF configuration, possibly indicating a change in underlying physical mechanism for the noise. (The exponent is $\alpha \approx 1.2$ for the V1 configuration.) We might further speculate that since the exponent changes mostly for V2 and V3, that the mechanism may be related to the drain (pinchoff) end of the MOSFET.

Figure 9 shows the impact of the guard gate bias voltage V_{GG}. It shows that the 1/f noise spectrum can be modulated by the guard gate bias voltage. For different versions of MGSF, the influence of the guard gate bias is different. The guard gate bias voltage can be used to optimize the 1/f noise of the MGSF. To achieve the lowest noise, the optimum guard gate bias voltage should be used. Overall, compared to the MGSFs with different guard gate bias voltage V_{GG}, the V0 SF has a similar or higher 1/f noise.

IV. Summary

In this paper, a multi-gate source-follower is presented. The MGSF shows similar or lower noise compared to the conventional MOSFET SF with the same total gate area. The bias voltage of the MGSF guard gate can be used to optimize the 1/f noise. The TCAD simulation result shows MGSF has a higher conversion gain compared to the conventional SF due to the small size of the modulation gate. The higher conversion gain and lower 1/f noise together should lead to reduced input-referred read noise. The MGSF may be useful for noise reduction in CIS and QIS devices.

References

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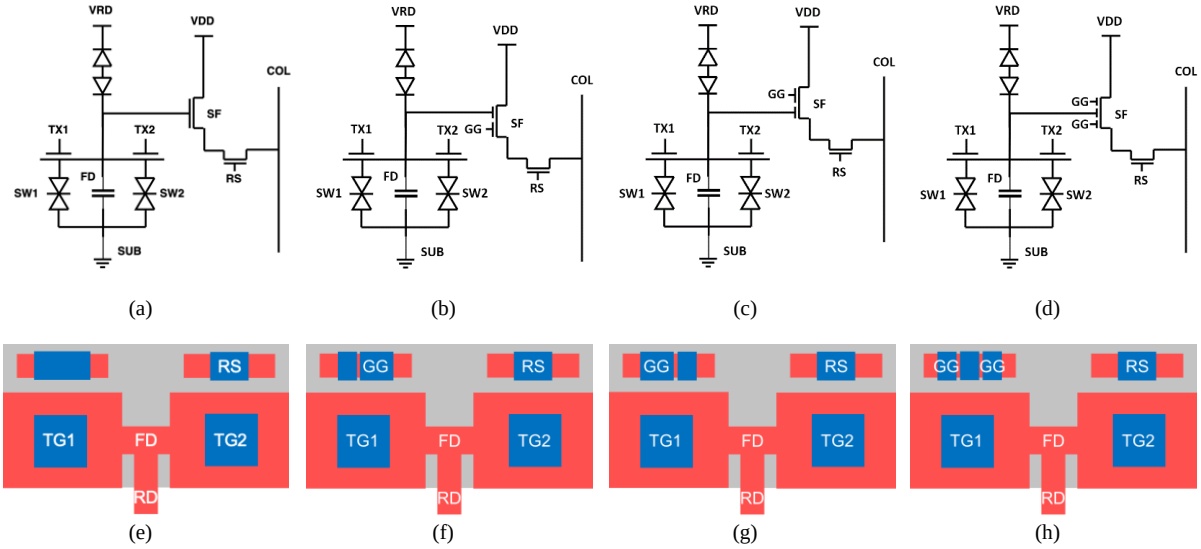


Figure 1. The schematic (a)(b)(c)(d) and layout (e)(f)(g)(h) of V0 SF and MGSF V1, V2, V3, respectively.

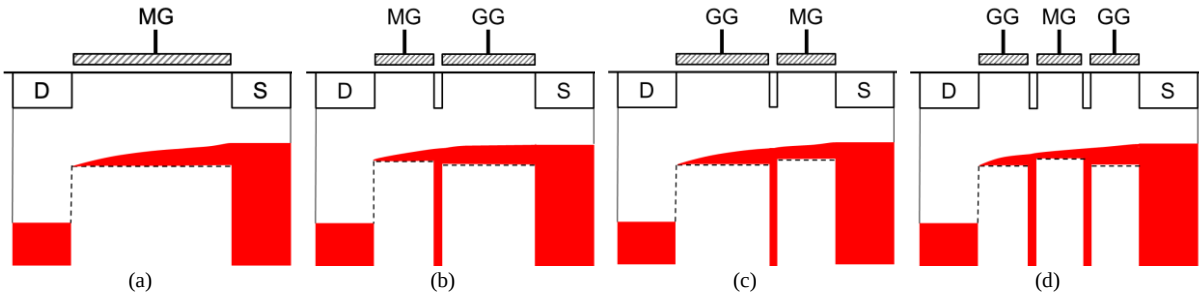


Figure 2. Operation potential-well diagram of (a) V0 SF, (b) MGSF V1, (c) MGSF V2, and (d) MGSF V3.

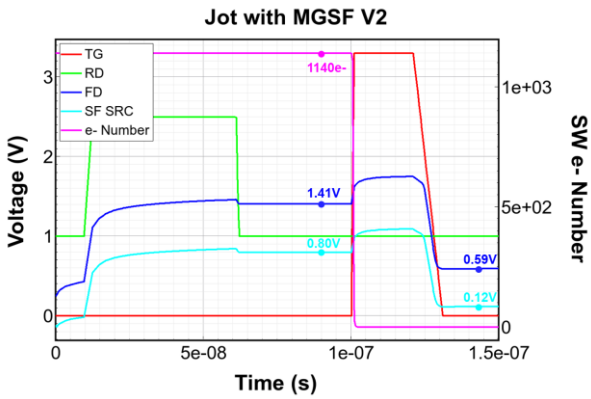


Figure 3. A transient simulation of a jot with MGSF V2 in TCAD.

SF Type	V0 SF	MGSF V1	MGSF V2	MGSF V3
Total Gate Area	0.0826 μm²	0.0826 μm²	0.0826 μm²	0.1134 μm²
C_{FD}	0.278 fF	0.229 fF	0.223 fF	0.226 fF
CG@FD	579.1 μV/e-	699.7 μV/e-	716.2 μV/e-	708.7 μV/e-
SF Gain	0.85	0.83	0.84	0.83
CG@SF SRC	490.7 μV/e-	578.7 μV/e-	598.1 μV/e-	588.1 μV/e-
CG Improvement	N/A	+18%	+22%	+20%
Measured SF Gain	0.78	0.76	0.77	0.76

Table 1. A summary of extraction results from TCAD simulation and the measured SF gain.

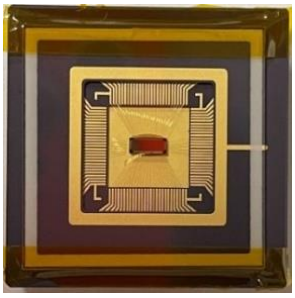


Figure 4. QIS test chip.

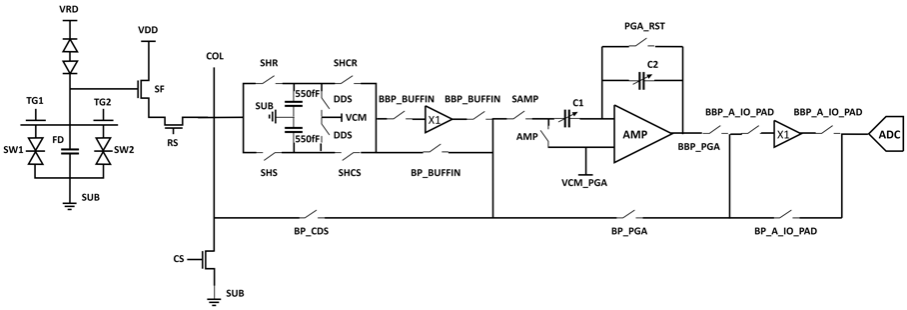


Figure 5. Schematic of the readout signal chain with the conventional SF configuration.

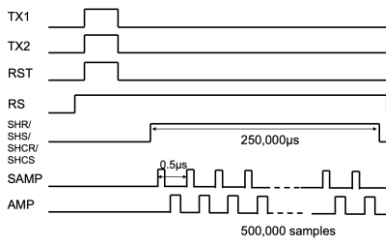


Figure 6. Timing diagram for noise measurement.

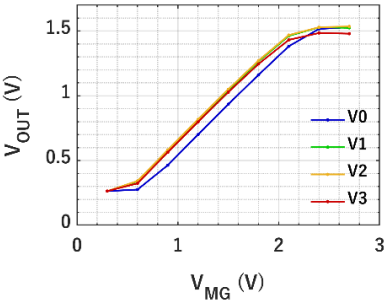


Figure 7. Gain Measurement for 4 types of SFs.

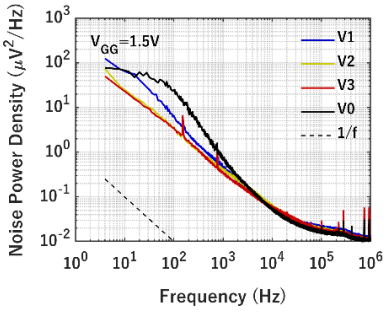
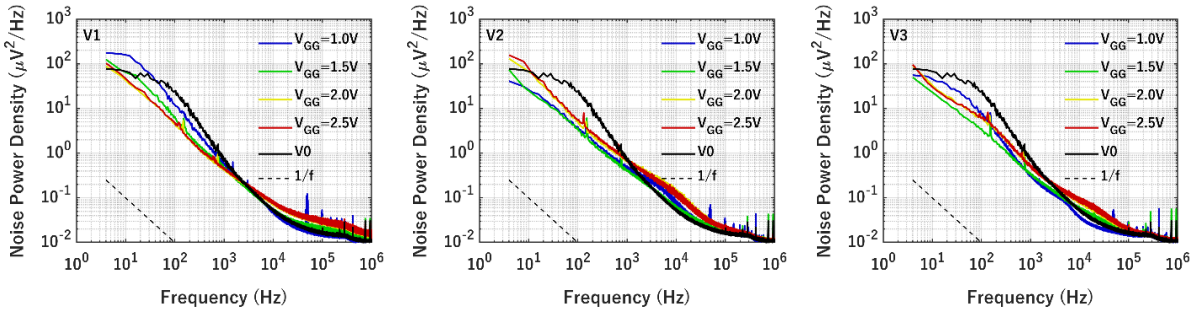


Figure 8. Input-referred noise spectra for 4 types of SFs (SF modulation gate bias voltage V_{MG} = 1.5V, guard gate bias voltage V_{GG} = 1.5V and bias current I_b = 1μA).



(a) (b) (c)

Figure 9. Input-referred noise spectra of 4 types of SFs at different guard gate bias voltages (SF modulation gate bias voltage V_{MG} = 1.5V and bias current I_b = 1μA). (a) MGSF V1. (b) MGSF V2. (c) MGSF V3.