A 124dB Dynamic-Range SPAD Photon Counting Image Sensor Using Subframe Extrapolation

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I. Introduction

Photon-count imaging is a promising technology for capturing images that has a noiseless high-speed readout and a high dynamic range (HDR) [1–8]. We previously demonstrated a single photon avalanche diode (SPAD) photon-counting image sensor with a 124 dB dynamic range (DR) employing a subframe extrapolating architecture for motion artifact suppression [9]. This paper presents the circuit operation for the 124 dB DR sensor, its pixel characteristics, and the complete suppression of parasitic light sensitivity (PLS) in the global shutter (GS) operation with full digital photon counting.

II. Implementation and concept

A back-illuminated SPAD pixel array is stacked on a bottom-tier chip with readout circuit blocks via pixel-parallel Cu–Cu connections, as shown in Fig. 1. Figure 2 shows a simplified schematic of the pixel unit. Each pixel has a 9-bit digital ripple counter (CN), which counts the incident photons. An overflow carry (OF) from the counter returns to the quenching circuit to control the SPAD activation and latches a timing code (TC). The 14-bit TC is distributed to all pixels and overwrites the counter when the OF flag changes. The 9-bit count of photons or the latched 14-bit TC is then read out.

The concept of extrapolating the photon count [8] is illustrated in Fig. 3. All photon counts are accurately obtained without counter overflow under low light conditions. In contrast, under high light conditions, the counter overflows at the number of counter bits (N_{OF}) and the overflowed pixel records the time of overflow T_{OF}. The actual number of incident photons during the entire exposure period (T_{EXP}) is then extrapolated. The signal-to-noise ratio (SNR) after overflow occurs remains at $\sqrt{N_{OF}}$, as shown in Fig. 3(b). Figure 4(a) illustrates the extrapolation error caused by a change in light intensity during exposure. To suppress motion artifacts and increase the maximum SNR, we implemented the subframe readout presented in Fig. 4(b).

III. Circuit operation

Figure 5 shows a timing chart of the photon counting. The exposure period for each frame is split into 20 sub-frames, as shown in Fig. 5(a). Each sub-frame is composed of a GS exposure and a digital readout scan. The pixel array is scanned 20 times for each frame, and the digital outputs are summed at the SRAM of the digital unit. In each sub-frame, photon counting starts after the counter and OF latch are reset by RST_{CN} and RST_{OF}, respectively. The TC is counted until the end of the exposure. After the exposure, the readout scan is performed in 300 ns per row.

Figure 5(b) shows a timing chart of the exposure period under low light conditions. D_{OUT} is triggered by an incident photon and an avalanche current at the SPAD, and then the in-pixel counter counts the photons one by one. The counter does not overflow in a sub-frame, and the pixel outputs the result of the photon count as is. In contrast, under high light conditions (Fig. 5(c)), each pixel autonomously switches its operation when the 9-bit counter overflows. In this case, the pixel deactivates its SPAD and records the 14-bit TC at the time of the overflow. The total output frame is calculated from the output code in each subframe with an overflow flag, as shown in Fig. 6.

The true photon count output is directly added to the total frame output code when the counter has not overflowed. In subframes with counter overflow, the actual incident photons are extrapolated from the TC using $(2^{14} - 1) \times 2^9$/TC. This technique substantially reduces the number of SPAD activations despite a large number of incident photons under high light conditions and reduces the pixel circuit area because a small number of counter bits can be used.

IV. Prototype chip and measurement results

Figure 7 shows a chip micrograph of the fabricated prototype with the subframe readout and extrapolating architecture. The prototype chip was fabricated with a 90 nm SPAD pixel for the top tier and a 40 nm CMOS readout circuit for the bottom tier. In this prototype, the SPAD pixels form a 320×528 pixel array with a pixel pitch of 6.12 μm; however, 2×2 SPADs were placed on

a 12.24 μm pitch pixel readout circuit that is constrained by the readout circuit area with some test equipment. Therefore, three of the four SPADs are unconnected so that the characteristics of the 6.12 μm SPAD may be evaluated. On the bottom tier, a 160×264-pixel circuit array and peripherals are implemented. An on-chip color filter was placed on the SPAD pixel with a 12.24 μm pitch for color imaging.

The design of the 6.12 μm pitch SPAD pixel is based on the 10-μm pixel reported by Ito et al. [10]. Figure 8 shows the measured photo detection efficiency (PDE) for the 6.12 μm pixels. The peak PDE values for the green pixel are 58% and 62.3% with 3V and 4V excess bias (V_{ex}), respectively. This peak PDE is larger than those in previous studies [11–13], because of the optimal potential slope for electron correction in the 7-μm-thick pixel [10]. The dark count rate (DCR) at room temperature is 35.4 cps (counts/s). This is equivalent to a 0.59 count and 0.77 e^-_{rms} for dark shot noise at a 1/60-s exposure. This small dark noise leads to a large DR and acceptable SNR under low light conditions.

The breakdown voltage (V_{bd}) of the SPAD pixel varies, and this induces photo response non-uniformity (PRNU) in the pixel array. However, the PRNU can be reduced by applying excess bias. Figure 9(a) shows the counting operation with respect to V_{ex}. The counting operation starts 1.5 V higher than the actual V_{bd} (V_{ex} = 0 V). This offset from V_{bd} at the starting point corresponds with the threshold voltage for signal pulse detection on the inverter. The variation in the rising edge reflects the V_{bd} variation, and is equal to 200 mV at one σ, as shown in Fig. 9(b). The output count increases gradually after this steep rise because the triggering probability increases. With a higher V_{ex} The triggering probability reaches approximately 100% and the count increase saturates. The PRNU depends on the slope of the counting curve, and a higher V_{ex} reduces it, as shown in Fig 9(c). The PRNU can be reduced to less than 2% when the excess bias is over 3 V. A higher excess bias contributes to a larger PDE and smaller PRNU but induces a higher DCR. We set the excess bias at 3V to optimize the PDE, PRNU, and DCR characteristics.

The results in Fig. 10(a) reveal that a DR of 124 dB is obtained without any dip in the SNR. Here, the maximum output count is over 10^6 count with a dark count of 0.59 count. A 40 dB SNR is maintained over an extended DR because true photon counting is performed for up to 10,240 photons, i.e., 9 bits × 20 subframes. The current consumption at the SPAD anode is efficiently suppressed by the SPAD deactivation after the counter overflow in the extrapolating operation, as shown in Fig. 10(b).

The PLS is completely suppressed with a GS operation caused by the full digital counting. In contrast to other GS methods, which accumulate the incident photon number in the analog domain, the photon number is stored in a digital counter in this prototype, and this is not affected by the general light intensity. Figure 11(a) shows a captured image with a conventional GS image sensor in which PLS is observed. The metal fan blade appears transparent against the high-intensity background light because of the PLS in the readout timing. PLS is not observed with this prototype, as shown in Fig. 11(b). This is because of the complete suppression of PLS in the full digital photon counting. Figure 11(c) shows the measurement results of the output code with SPAD deactivation during the entire exposure period. The output code is completely zero, even with a very high photon incidence, and thus the captured image of a rotating fan blade is not affected by PLS.

Figure 12 shows the measurement results of motion artifact suppression by the subframe readout. The motion artifact was measured using a color stripe on a 1,110-rpm rotating disk (Fig. 12(a)). False color and distortion are observed with a conventional multiple exposure technique and rolling shutter exposure, as shown in Fig. 12(b). Figures 12(c)–(e) are captured images of rotating stripes using 2-, 5-, and 20-subframe operations, respectively. The 20-subframe extrapolation sufficiently suppresses motion artifacts.

Figure 13 shows a HDR image captured using a 250 fps GS with the extrapolating photon count and subframe readout. Because of the GS and 20-subframe HDR operation, no motion artifacts can be observed, even in the image of a 225-rpm rotating fan.

The performance of the prototype is compared with previous studies in Table I. This work achieves both a 250 fps GS and over 120 dB DR using pixel-parallel photon counting without any inter-frame mode change, which also achieves motion artifact suppression without reducing SNR over the 124 dB DR. Compared to full photon counting, which consumes a large amount of energy in proportion to the number of photons under high light conditions [3], the prototype with the extrapolating architecture drastically reduces the power by a factor of 100 at 10^6 incident photons.

References

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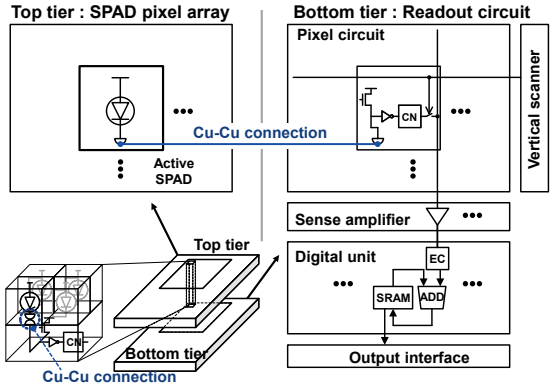

Fig. 1. Simplified block diagram of the prototype.

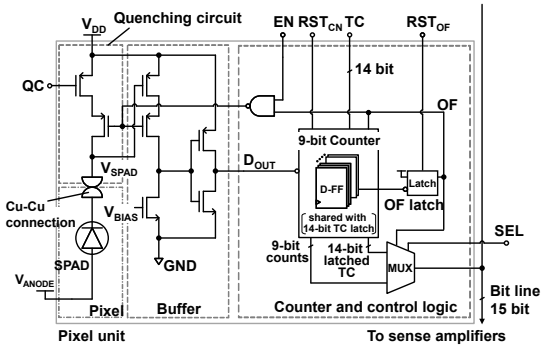

Fig. 2. Simplified circuit diagram of a pixel unit.

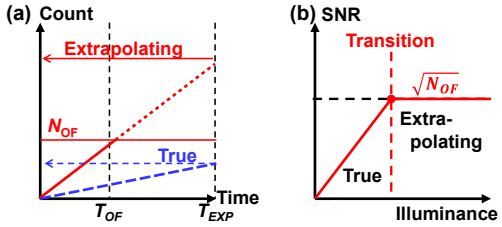

Fig. 3. Concept of photon count extrapolation.

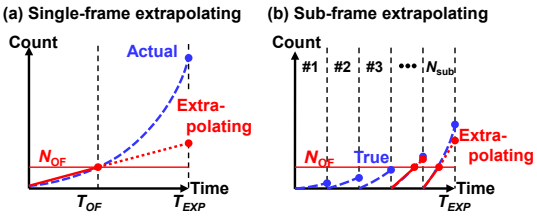

Fig. 4. Extrapolation error caused by a change in light intensity during exposure.

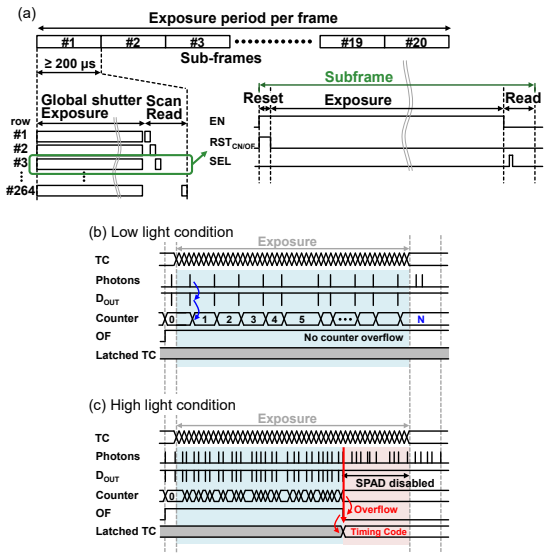

Fig. 5. Timing chart for circuit operation.

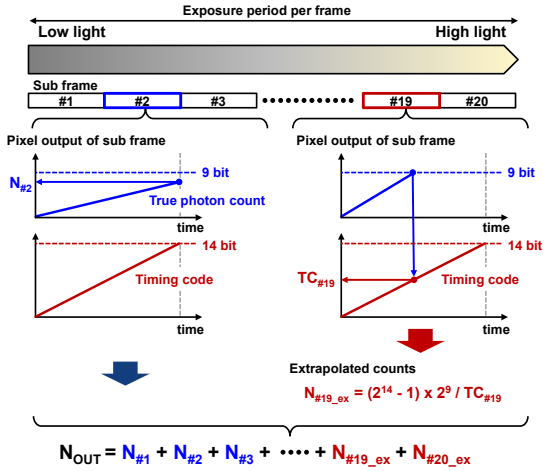

Fig. 6. Single frame reconstruction from 20 subframes.

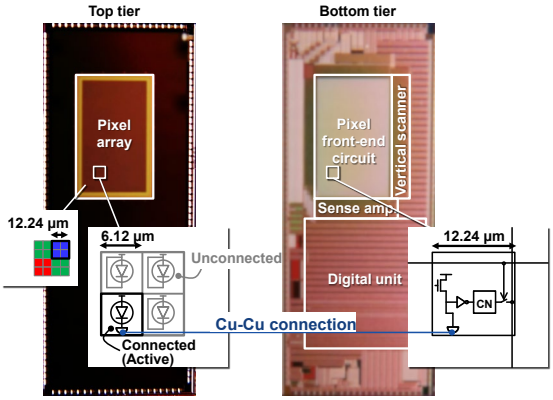

Fig. 7. Prototype chip.

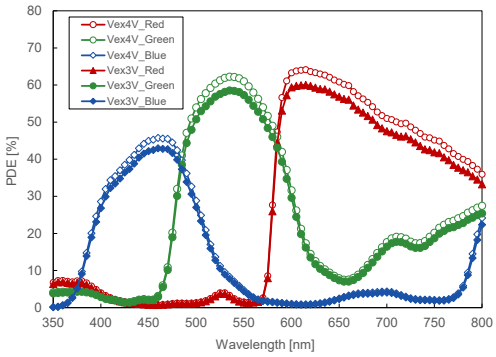

Fig. 8. Measurement results of PDE with V_{ex} = 3 V and 4 V.

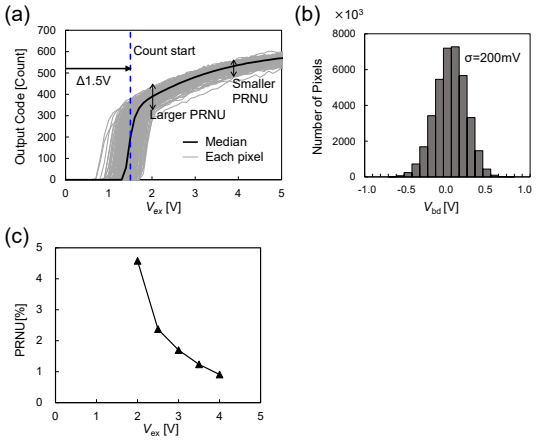

Fig. 9. Output count and PRNU dependence with respect to applied voltage on V_{ex}.

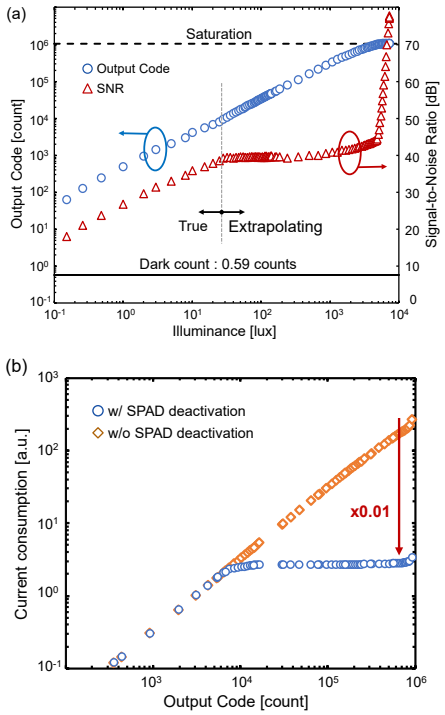

Fig. 10. Measurement results of DR, SNR, and current consumption in subframe photon count extrapolation.

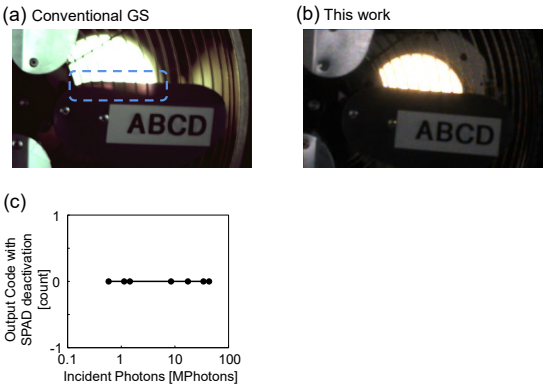

Fig. 11. PLS measurement results and comparison with conventional charge domain GS.

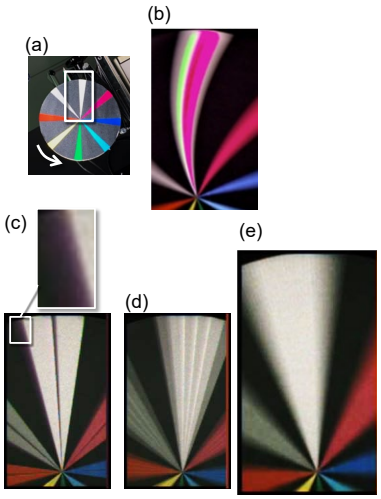

Fig. 12. Measurement results of motion artifact suppression.

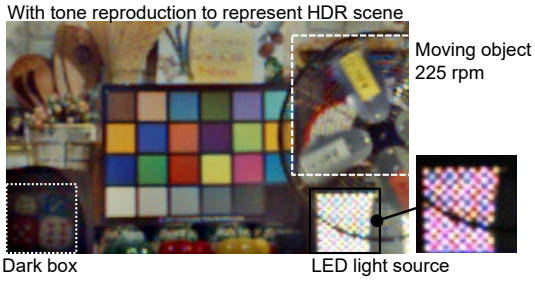

Fig. 13. 250-fps HDR captured image

TABLE I. Performance comparison.

	ISSCC 2016 [3]	ISSW 2020 [4]	Optica 2020 [5]	Sensors 2018 [6]	ISSCC 2019 [2]	This Work
Pixel pitch [μm] ( ) : HDR mode	3.8	80	9.4	8.25	9.2 (36.8 x 9.2)	12.24
Pixel array ( ) : HDR mode	1280 x 720	8 x 8	1024 x 1024	96 x 40	256 x 256 (64 x 256)	160 x 264
CMOS technology	110 nm	180 nm	180 nm	40 nm	Stacked 90 nm/40 nm	Stacked 90 nm/40 nm
Num. count in pixel ( ) : HDR mode	1 bit	14 bit	1 bit	12 bit	14 bit (28 bit)	9 bit shared with 14-bit TC latch
Frame rate [fps] in HDR	15	20	0.45	60	30	60 ~ 250
Dynamic range [dB]	100	129	108.1	109	120	124
SNR dip in HDR	Dipped	Dipped	Dipped	Dipped	No Dip	No Dip
Motion artifact suppression	No	No	Yes	Yes	Yes	Yes
Power* [a.u.] w/ high light	Switched to analog	Switched to analog	0.06	0.008	1	0.01

* Relative power estimated by the number of SPAD activation under high light condition with 10^6 photons.