A 1-Transistor SPAD Quanta Image Sensor for High-Speed and Small-Pitch Arrays

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***Abstract*—A SPAD-based pixel with a single transistor has been designed and implemented in a 150nm standard CMOS technology for the realization of a Quanta Image Sensor (QIS). The inherently digital nature of the SPAD device minimizes circuitry and simplifies the achievement of single-photoelectron sensitivity. The pixel revamps the concept of CMOS passive-pixel sensors to achieve a pixel with a pitch of 7μm and a geometrical fill-factor of 31% in an unoptimized process. The speed of the presented QIS architecture is limited only by the output interface, while requiring extremely simple column circuitry such as a sense amplifier, thus minimizing power requirements.**

***Index Terms*—SPAD, quanta image sensor, binary image, high-speed, single-photon.**

I. Introduction

QUANTA Image Sensors (QIS) are arrays of small pixels (ideally, sub-diffraction limited) with enough sensitivity to recognize whether a photon hit the pixel or not, thus outputting just either '1' or '0', respectively [1]. In practice, a QIS can be realized thanks to the tremendous progress in image sensor pixels and their readout, achieving megapixel arrays with 1.1μm pitch and $0.2e^-$ readout noise, effectively enabling single-photoelectron sensitivity without the need of internal photodiode gain [2]. Nevertheless, on the other hand single-photon avalanche diode (SPAD) devices came to age, recently achieving performance levels that can compete with conventional photodiodes where sensitivity is of importance, such as shot-noise limited high-dynamic range (HDR) up to 124dB at 12.24μm pitch [3].

SPAD-based pixels [4] in principle could exploit the early digitization to avoid the expensive challenge of achieving deep sub-electron readout noise that reasonably needs to be kept below 0.3e-rms over the whole array. Usually the price to pay for the use of SPADs is a reduced quantum efficiency (or photon detection efficiency, PDE), a larger area and a more complex circuitry. State-of-the-art for SPAD-based pixel is a 4T scheme using an active-pixel like circuitry [5]. Instead, in this paper a prototype imager with single-transistor (1T) SPAD-based pixels is presented with the objective to draw a roadmap towards SPAD-based QIS with maximum speed and minimal complexity.

II. 1T Pixel and Readout Concept

Passive pixel sensors (PPS) were rapidly surpassed by active pixel sensors (APS) because of the challenge, for large arrays and small pixels, to preserve the noise performance while handling a column capacitance orders of magnitude higher than the photodiode capacitance. When the signal comes from a SPAD, it is however many orders of magnitude higher than the signal generated by a single photoelectron in a high-conversion-gain pixel: several volts with respect to hundreds of microvolts. Moreover, there is no need to preserve its analog amplitude and strongly minimize the noise, but rather to verify its value against a digital threshold. This brings back and makes attractive again the concept of a passive pixel, implemented by a single SPAD and a single transistor, as shown in Fig. 1. Through the access transistor, the SPAD can be either reset or readout, both by the same column circuitry: a precharge transistor enables bringing the SPAD beyond the breakdown voltage upon activation of the RES signal, while a sense amplifier has the purpose of detecting if there has been an avalanche in the pixel. The obtained single-bit information can then be sampled and streamed-out immediately, without any complex analog operation. The readout of a SPAD-based QIS then becomes like reading-out a simple dynamic RAM, with minimal power consumption and very high speed.

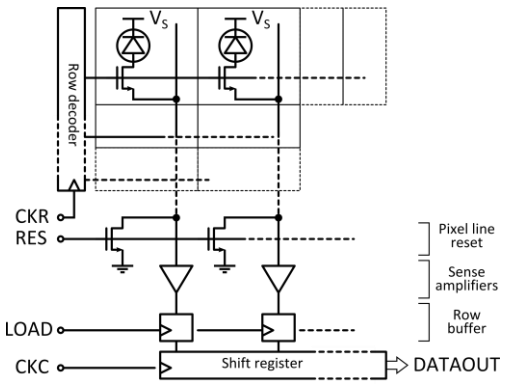

Fig. 1. Schematic of the 1T SPAD pixel and QIS architecture, with per-column pixel line reset, sense amplifier and digital readout.

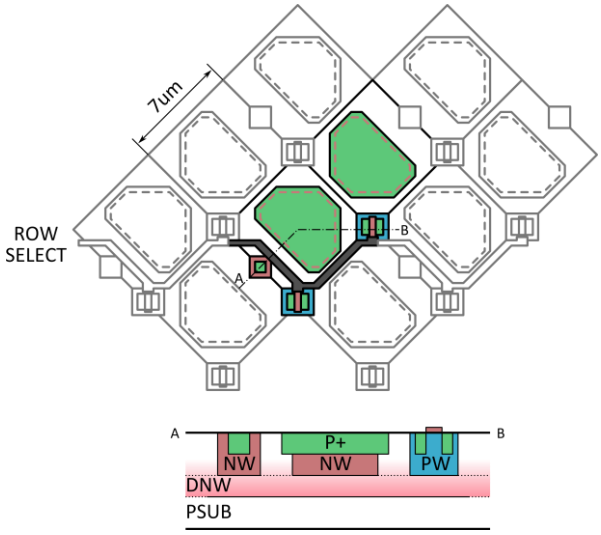

Fig. 2. Layout arrangement and cross-section of one pixel, showing from left to right: the cathode (deep-nwell contact), the p+/nwell SPAD with virtual guardring, and the pwell for the nmos transistor.

The light integration can occur in a rolling-shutter fashion, by resetting a row and reading out the next one, setting the integration time equal to the frame time. However, given the sensitivity of the SPAD device, it is possible to use shorter integration time by integrating during readout of the previous row, thanks to the value latched in the output shift-register. This row-by-row integration avoids early saturation and minimizes row-wise crosstalk between SPADs.

Fig. 2 shows the implemented pixel layout that, in order to minimize the pitch, has been designed with an alternated regular pattern in the diagonal direction to maximise fill factor: however, this does not prevent more conventional arrangements. The SPAD is a p+/nwell junction with low-doped virtual guard-ring, isolated together with the pixel nmos within a deep nwell.

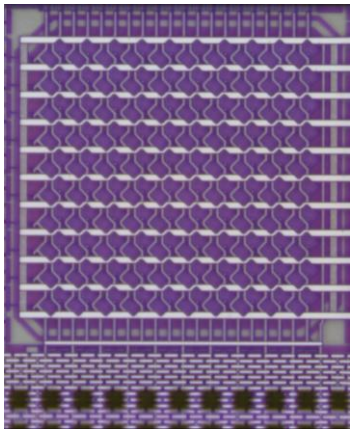

Fig. 3. Micrograph of the 20x10-pixel test imager realized in a standard 150nm CMOS technology.

III. Measurements

A prototype QIS of 20×10 pixels has been designed and fabricated in a standard 150nm CMOS technology (chip micrograph of Fig. 3) in order to validate the concept. The designed pixel has a pitch of 7μm with a drawn fill-factor of 31%.

A. Photon rate estimator

The output of the QIS is a stream of '0' and '1', for each pixel: while a '0' univocally represents zero hits, a '1' can be *one or more* events (either photons or dark counts); for example, with a mean of 1 photon, the probability of '0' is ~0.37, and *P(N>1)* is not negligible. Therefore, while the average of the binary output stream does not properly represent the photon rate, the data can be reconstructed with a Poissonian estimator based on the acquisition of N_f frames (or bitplanes), where for each pixel the number of zeroes over N_f is the measured probability *P(0)*. This method, used for all the following measurements, yields the expected average rate:

$$\lambda = ln\left(\frac{1}{P(0)}\right) \approx ln\left(\frac{N_f}{N(0)}\right) \quad (1)$$

Using eq.(1) removes the pile-up compression until *P(0)* is measurable, i.e. there is at least a '0' over N_f bitplanes. Otherwise, with all '1', the only information is that $\lambda > ln(N_f)$, that gives a higher bound on the estimated rate at a certain N_f.

B. Pixel characterization

SPAD devices have been characterized in terms of breakdown voltage (V_{bd}) and DCR. Exploiting the capability of the sense amplifier to switch even with a very small excess bias (i.e. <0.5V) with a weak illumination, V_{bd} is calculated extrapolating the estimated counts to zero. The resulting measurement is shown in Fig. 4, exhibiting a typical distribution with a dispersion of few tens of mV.

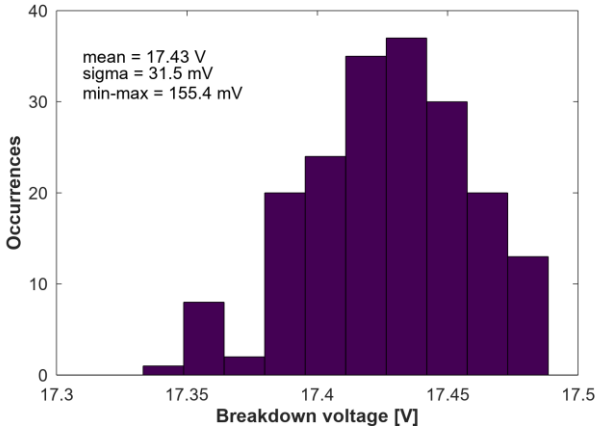

Fig. 4. Breakdown voltage distribution of the p+/nwell SPADs, showing a limited non-uniformity (σ_{Vbd}=31.5mV) expected for small area arrays.

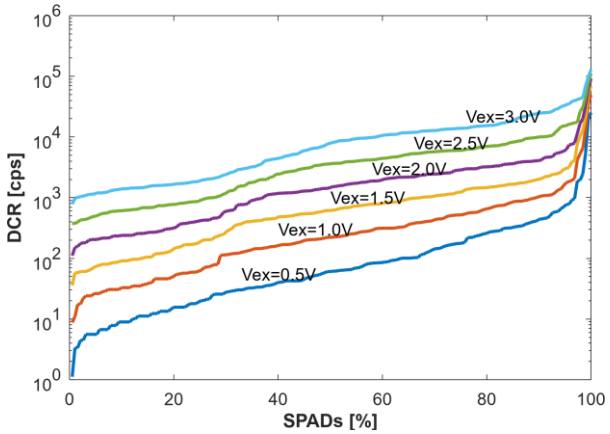

Fig. 5. DCR distribution of the pixel array at different excess bias values.

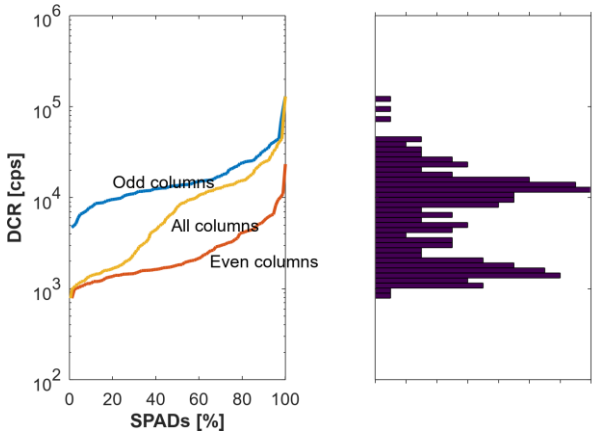

Fig. 6. DCR distribution at Vex=3V for odd and even columns, highlighting a clear pattern in dark noise favoring even columns.

The DCR of all pixels is plotted in Fig. 5: it shows a peculiar distribution, more visible at larger excess biases that can be attributed to the asymmetric pixels' layout. Indeed, by plotting even/odd columns separately, as in Fig. 6 for the 3V excess bias, a bimodal distribution becomes clear and it can be observed that odd columns are ~10× noisier, despite having the same boundary. To the authors' knowledge, such behavior has not been observed before as asymmetric SPAD design is not commonly found in literature: more investigation is needed to understand whether silicon crystal orientation, mask generation artifacts, or tilted implants could be the cause. Overall, the DCR of these pixels is relatively high, with a median of ~60cps/μm^2 at 2V excess bias, that is most probably due to the aggressive layout and no nwell ring (just a single tap) around and between SPADs.

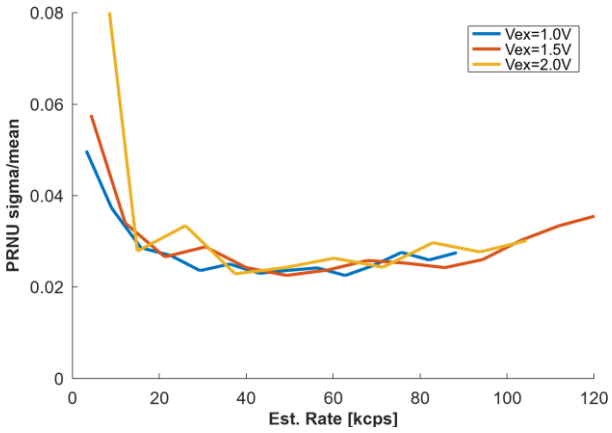

Fig. 7. Photoresponse non-uniformity at different bias and illumination, with a mean value ~3% when the illumination overtakes the DCR.

C. *Imaging measurements*

The uniformity of the array has been evaluated in order to assess whether small SPADs can significantly show pixel-to-pixel differences in detection efficiency. Evenly illuminated pixels show a photoresponse non-uniformity PRNU<3% (Fig. 7), that includes also the illumination uniformity achievable in the measurement.

QISs have an intrinsically excellent linearity, rooted in their concept: moreover, the use of the Poisson estimator of eq.(1) linearizes the otherwise compressed characteristic. As measured and shown in Fig. 8, the developed QIS exhibits a good linearity: the dynamic range is limited on the lower end by the DCR, and on the higher end by the number of acquired bitplanes N_f. This latter aspect enforces the requirement of having a simple and fast readout, i.e. more bitplanes/s, that directly reflects in a high dynamic range. The characterization and subtraction of the pixels' DCR enables recovering the dynamic range of noisy pixels (right side of Fig. 8) at the expense of a higher temporal noise.

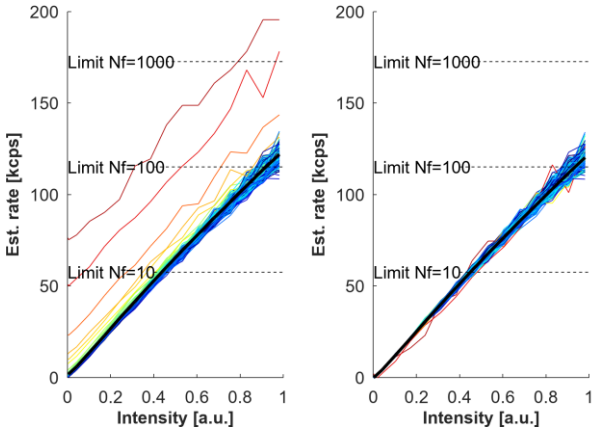

Fig. 8. Power response of all pixels at Vex=1.5V and N_f=5000, without (left) and with DCR subtraction (right), highlighting the absence of pile-up compression and large dynamic range.

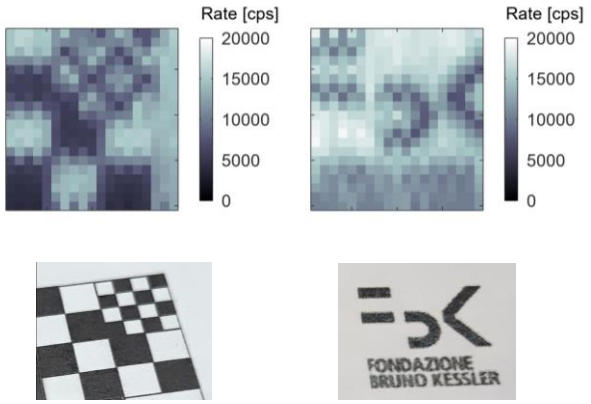

Fig. 9. Sample images obtained at Vex=1.5V, 20μs integration and N_f=5000, interpolated to recover the square form factor from the 20×10 array.

Fig. 9 shows two sample images, resampled to the correct aspect ratio, from 20×10 to 20×20 pixels, by inserting the missing pixels by interpolation of neighbors. The used integration time is 20μs and 5000 bitplanes, corresponding to a total exposure of 100ms, despite it is not required for a good quality image.

A sample image has been acquired with N_f from 1 to 10k bitplanes in order to assess how the quality is affected by the number of bitplanes. Fig. 10 shows on the top part how the image qualitatively reaches the maximum signal-to-noise ratio at N_f = 500, that is also confirmed numerically by the graph on the bottom part. The theoretical SNR considers the shot noise, the PRNU, and the average DCR (including the dark frame subtraction), calculated in the bright and dark areas of the image with N_{ph} being the average number of counted photons:

$$SNR_{max} = \frac{N_{ph}}{\sqrt{N_{ph}+(PRNU \cdot N_{ph})^2+2 \cdot DCR}} \quad (2)$$

The theoretical SNR saturates for strong illumination at about 20log(1/*PRNU*) = 31dB, limited by the sensor non-uniformity. The measured SNR of the acquired images reaches about 27dB: it flattens slightly before the theoretical estimation because of the non-uniform illumination and imaged target.

IV. Discussion and Conclusion

The proposed realization of a prototype QIS by means of 1-T SPAD-based pixels leverages on the photon-to-digital conversion that is intrinsically performed by the device. The main advantage of the single-transistor SPAD pixel is given by the fact that there is no need for ultra-low noise readout circuit and A/D conversion, highlighting the potential for low-power and high-speed operation.

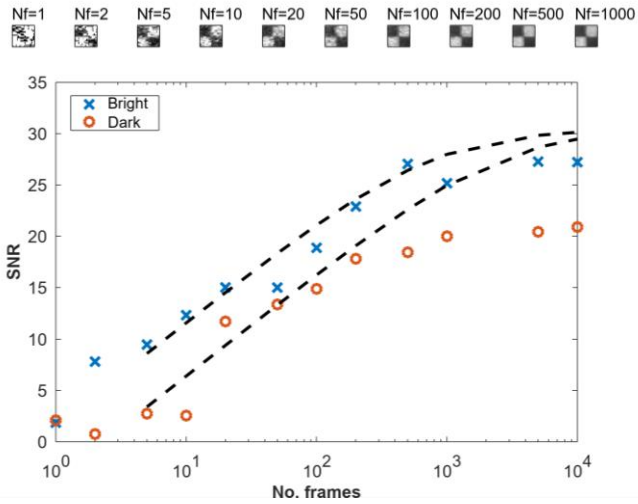

Fig. 10. Image extracted at different number of bitplanes (top) and SNR in dark and bright areas of a checkerboard pattern, highlighting the need for fast readout in QIS.

While the prototype is not optimized (300μA supply current, 50μs readout), the architecture potentially enables sub-μA/column consumption and high speed. Another relevant feature, which is not available in conventional APS-based QIS, is the possibility to adjust the pixel PDE by varying the excess bias, V_{ex}.

Furthermore, there are improvements to be done in order to achieve optimal performance and scalability. In particular, the currently unoptimized SPAD design can be fine-tuned, possibly with process customizations, in order to reduce the DCR of the pixels. In perspective, larger array size will need careful design of the sense amplifier, as the increase of the column line capacitance will pose challenges in the readout, as in a passive-pixel sensor. However, 3D stacking the 1-T SPAD QIS to a bottom tier with pixel-to-pixel connections could enable a whole new generation of imagers, from high-dynamic range imaging to event-based image sensors, but also time-resolved architectures.

References

[1] E. R. Fossum, et al., "The Quanta Image Sensor: Every Photon Counts," Sensors, vol. 16, no. 1260, pp. 1-25, 2016.

[2] J. Ma, et al., "Photon-number-resolving megapixel image sensor at room temperature without avalanche gain," Optica, 4(12), 1474-1481, 2017.

[3] J. Ogi, et al., "A 250fps 124dB Dynamic-Range SPAD Image Sensor Stacked with Pixel-Parallel Photon Counter Employing Sub-Frame Extrapolating Architecture for Motion Artifact Suppression," ISSCC, pp. 113-115, 2021.

[4] M. Perenzoni, "Single-photon avalanche diode-based detection and imaging: Bringing the photodiode out of its comfort zone," IEEE Solid-State Circuits Magazine, 10(3), 26-34, 2018.

[5] M. Mori et al., "A 1280×720 single-photon-detecting image sensor with 100dB dynamic range using a sensitivity-boosting technique," ISSCC, pp. 120-121, 2016.