A 4-tap Lock-in Pixel Time-of-Flight Range Imager with Substrate Biasing and Double-Delta Correlated Multiple Sampling

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1 Introduction

Time-of-flight (TOF) range imaging [1-5] is attracting much attention for various applications. For TOF range imagers, a high-speed lock-in pixel is desired to use a short light/gate pulse or high modulation frequency to improve a depth resolution. In addition, a high-speed carrier collection from a deep substrate is essential because of the utilization of an NIR light source.

The other key point is lower dark noise to improve the range resolution at low signal light conditions. In TOF range imagers, a floating diffusion (FD) is typically used as storage; kTC noise cannot be canceled. Although additional in-pixel storage is often used [2,4], the choice suffers from a limited full well capacity.

For these requirements, this paper presents a lock-in pixel with substrate biasing for high-speed modulation and a readout of double-delta correlated multiple sampling (DDCMS) for lower dark noise.

2 Sensor Architecture

Figure 1 shows the proposed pixel structure. The structure has a small negative bias ($V_{B,SUB}$) applied to the substrate to enhance the collection speed of signal electrons from the deep substrate. The substrate is biased through the substrate contacts placed on the surrounding area other than a pixel array and peripheral circuits. The pixel area has two different bulk voltages: GND (0V) is used for in-pixel transistors, and $V_{S,SUB}$ (typically -1V) is used for the bulk of modulator. For reduced leakage current from the pixel area to the substrate, n-wells are formed surrounding the p-well region. The p-well of peripheral circuits is typically grounded and isolated from the substrate using a deep n-well.

Figure 2 shows a newly-designed 4-tap lateral electric field charge modulator (LEFM) [1,6]. LEFM gate pairs (G1-G4) are formed in point symmetry to a center point. As shown in Fig. 2(b), the generated electron at the upper/lower position is transferred to the upper/lower side of FD4.

We have implemented a prototype chip using 0.11-um CIS technology, as shown in Fig. 3. The pixel array consists of 80(H) X 112(V) for the proposed pixel, and the pixel pitch is 16.8 x 16.8 um^2. Four sets of folding-integration and cyclic ADC [7] are implemented in a column, achieving a simultaneous readout for the 4-tap signal.

3 Measurement results

Figure 4 (a) shows a modulation characteristic with and without the substrate biasing where only one tap (G1) is used. The result shows the improvement of

modulation speed. Fig. 4(b) shows a modulation characteristic after a sensitivity correction between taps.

Figure 5 shows the readout timing of DDCMS. Its concept is similar to correlated quadruple sampling [8], enabling frame CDS while reducing 1/f noise. In DDCMS, the multiple-sampling scheme is introduced to obtain the lower noise even for the large capacitance (>10 fF) at the FDs. In the prototype chip, the dark noise of 80 e- is reduced to 15 e- using DDCMS.

Figure 6 shows measurement results of equivalent depth and depth resolution. The equivalent depth is calculated from the change of delay time of the light source. The light and gate pulse was set to 4 ns. The 4-tap signal enables the depth calculation for three time windows; the measurable range of the single frame is 1.8 m. As shown in Fig. 6, the depth resolution is much improved owing to DDCMS.

Acknowledgments

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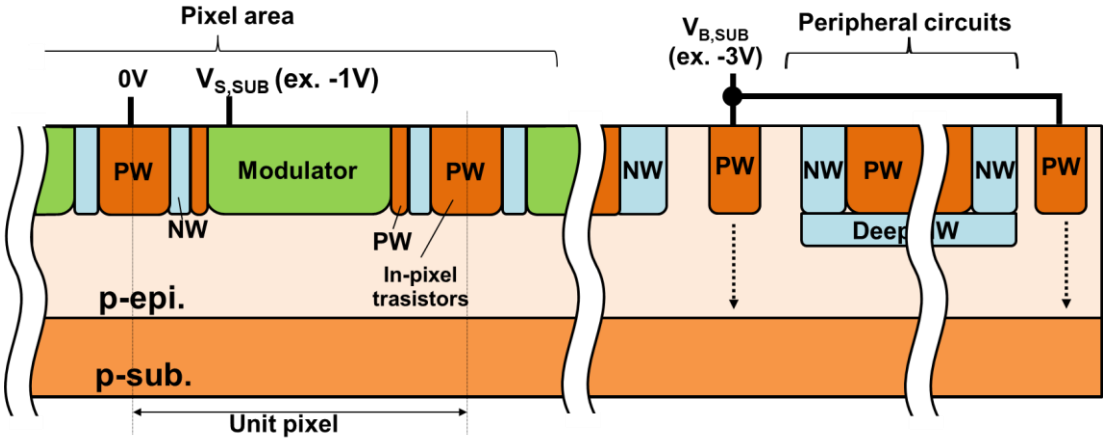

Fig. 1 Substrate biasing structure.

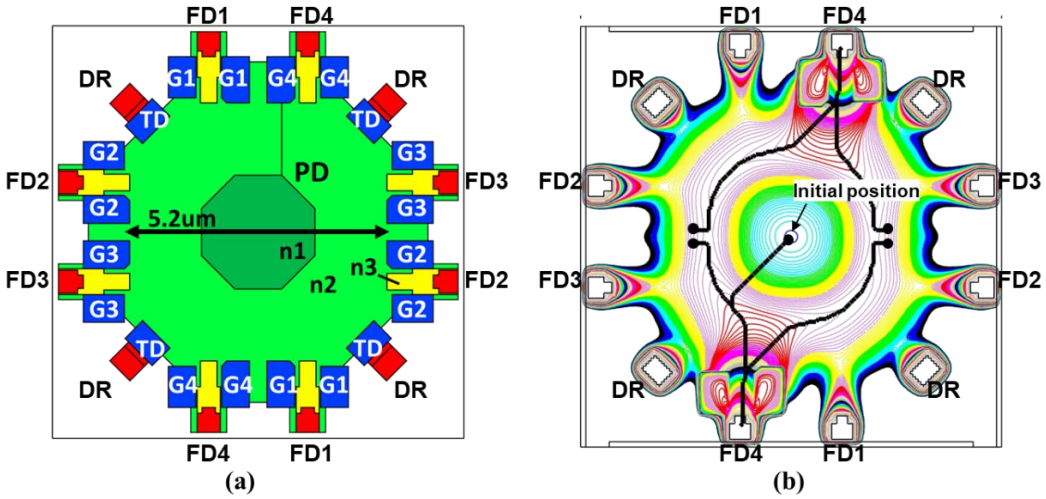

Fig. 2 4-tap LEFM (a) pixel layout. (b) simulation results of potential distribution and electron trajectories at the condition of G4 on. Electron trajectories for five different initial points are also shown.

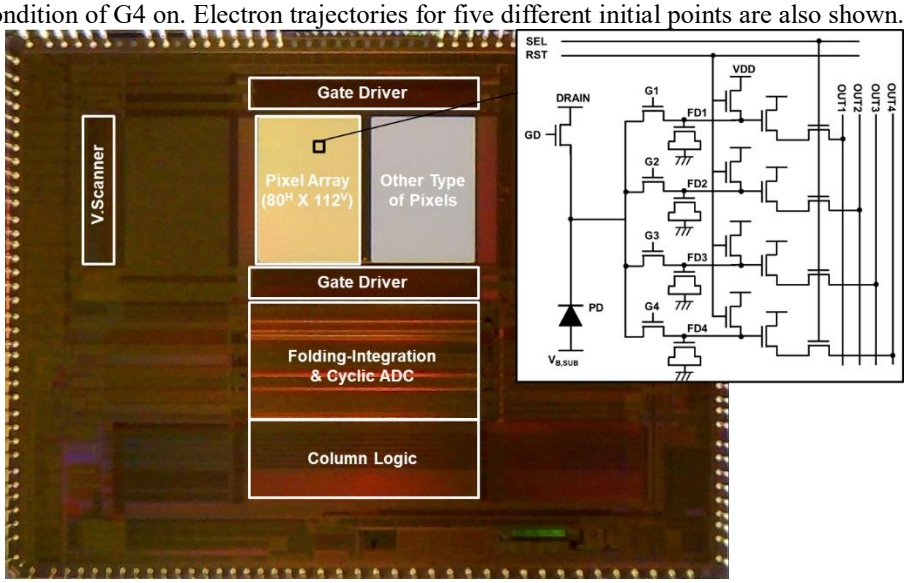

Fig. 3 Prototype chip photograph and pixel schematic

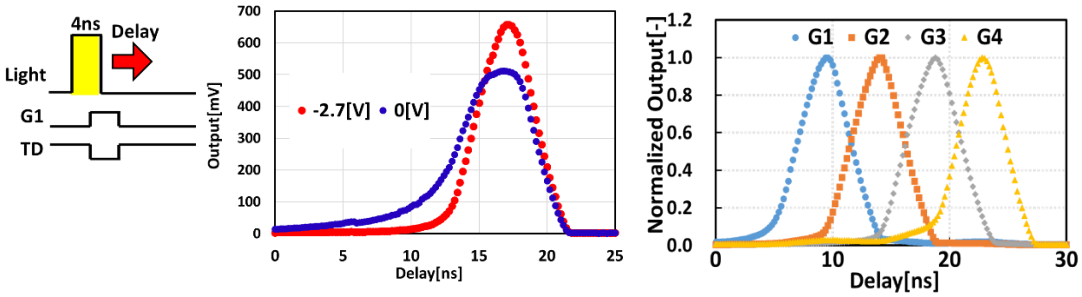

Fig. 4 modulation characteristic. (a) one-tap modulation with/without the substrate biasing. (b) 4-tap modulation with 4-ns light and gate pulse width.

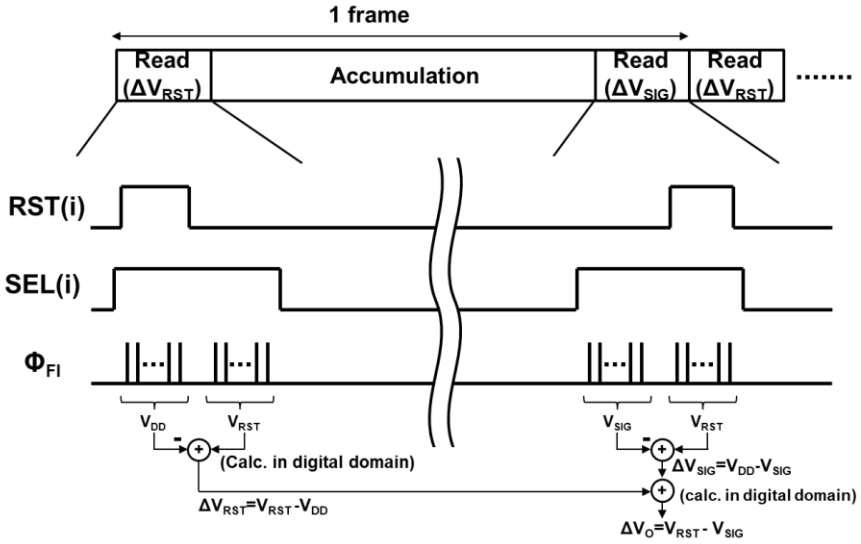

Fig.5 Readout timing of DDCMS. Φ_{FI} represents sampling and integration timing at folding integration and cyclic ADC.

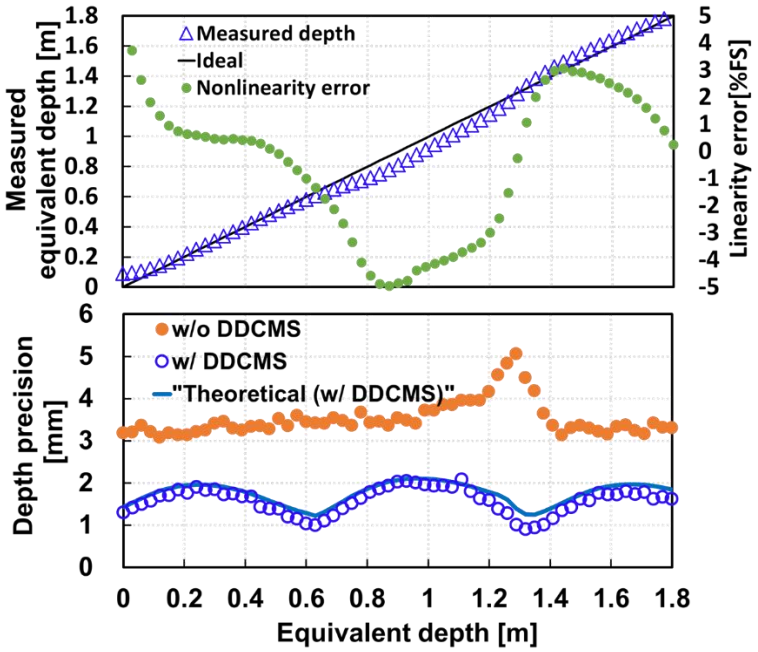

Fig. 6 Equivalent depth measurement results.
The delay of the light trigger virtually varies the target depth.