CMOS 3D-Stacked FSI Multi-Channel Digital SiPM for Time-of-Flight Vision Applications

Francesco Gramuglia*, Andrada Muntean*, Carlo Alberto Fenoglio, Esteban Venialgo, Myung-Jae Lee, Scott Lindner, Makoto Motoyoshi, Andrei Ardelean, Claudio Bruschini**, Edoardo Charbon**

Multi-channel digital silicon photomultipliers (MD-SiPMs) [1] have been introduced to increase spatial granularity of time stamping in multi-photon detection with respect to analog SiPMs. The use of CMOS technologies for their implementation guarantees cost reduction and the integration of new functionality near light detection.

To achieve time stamps with high resolution and low dead time, advanced technology nodes are preferable. However, this choice can potentially compromise the performance of single-photon avalanche diodes (SPADs), the core of the SiPM. 3D integration overcomes this issue by allowing the selection of different technologies for top- and bottom-tier chips. The first 3D-integrated SPAD-based sensor was implemented by employing a backside-illumination (BSI) approach [2]. This chip had very low sensitivity in the 400-500 nm range, making it unsuitable for some applications. Improvements of the technology, led to other implementations of 3D-stacking for SPADs [3,4]. Although higher sensitivity was achieved at lower wavelengths, it is still too low for many time-resolved imaging applications, especially in bioimaging.

We have therefore developed a 3D-stacked frontside-illuminated (FSI) MD-SiPM [5], whereas the approach is similar to the one first proposed in [6]. The sensor consists of top- and bottom-tier chips all fabricated in 0.18µm CMOS technology that are bound in a 3D-stacked configuration. The two tiers are connected by means of through-silicon vias (TSVs) and bump-bonds (Fig. 1), whereas a TSV has been implemented for each SPAD. Fig. 2 shows the back of the top-tier where micropillars are implemented to allow proper electrical connection between the two tiers after 3D-stacking (Fig. 2, *right*). Top and bottom-tier are bonded to create the electrical connection and have a flat and mechanically stable structure, thanks also to the relatively small TSV pitch (Fig. 3). To avoid the need for different TSV structures and to eliminate the risk of breakdown in the oxide surrounding the TSVs, high voltage is provided to SPADs through a set of bonding pads directly on the top tier. In this implementation, the maximum voltage across the TSV oxide never exceeds 5V. To prevent cracks during the wire-bonding process, a support structure is implemented beneath the bonding pad (Fig. 4).

While the top-tier chip is dedicated to light detection, the bottom-tier embeds all the electronics needed for such system, including SPAD address tree, photon counters, time-to-digital converters (TDCs), data distribution, readout scheduler, and a TDC calibration system.

The full chip (Fig. 5) measures 7.5 × 4.2 mm^2 and it comprises two arrays of 64 × 64 SPADs each. The two arrays are segmented in 8 × 8 clusters of 64 pixels each (Fig. 5-6). The MD-SiPM is based on an *event-driven* architecture. Fig. 7 shows a simplified scheme of the cluster architecture. The pixel pitch is 50 µm, the fill factor 67%, and the peak PDP 55% at 500nm (Fig. 8). Each SPAD pixel, based on a P-i-N cross section [7,8], uses a cascode transistor to allow high excess bias voltage, thus improving sensitivity and jitter performance [8,9]. Moreover, active recharge allows the tuning of the pixel dead time, down to about 3 ns [8]; it guarantees a good temporal compression, thus mitigating the limitation given by the dead time of the propagation tree [10,11]. A pixel masking circuit can turn off noisy pixels and thus improve the overall SNR. The pulses generated by the SPADs are propagated through an OR-tree for spatial compression within the cluster, up to the input of the TDC trigger [11]. 128+1 TDCs, based on a multi-path gated ring oscillator [12,13] (Fig. 9), has an LSB of 15ps. The power consumption per TDC is ~1.4mW. A photon-counting system is added in each cluster, along the propagation tree, to estimate the total number of photons detected. The counting is performed by TSPC counters connected to the fifth level of the OR-tree to minimize the effect of dead time. The result of each counter is summed by a 6-bits adder, sampled with a frame signal (STOP) and saved in a memory buffer. Along the propagation OR-tree, a winner-take-all (WTA) tree [2] was inserted to determine the address of the first SPAD that fired, triggering the TDC of its cluster. This strategy allows to reach a spatial granularity at the level of a single SPAD. In addition, correction of the temporal skews given by unbalance of the signal paths is also possible.

A flag bit is asserted every time the TDC is triggered in order to indicate the presence of valid data. All TDC flags are taken as an input by a control unit. The latter acts as a scheduler that implements a priority ceiling protocol, where each cluster has a fixed priority. The use of such a system, especially at low light levels, eliminates the need for reading all of the clusters, thus reducing data throughput, readout time, and power consumption.

Each array of the chip can be read out independently through a random-access architecture composed by a row encoder and column multiplexer (Fig. 6). All the clusters of the same column share the same output bus and access it through a high impedance buffering stage, enabled by the row encoder. The data are output in parallel to increase readout speed. The system was designed to achieve a maximum readout speed up to 1 Mframe/s. Each output word provides the address of the cluster read, the address of the SPAD that triggered the TDC for that frame, the TDC output, and the result of the counting system.

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F. Gramuglia, A. Muntean, C. A. Fenoglio, A. Ardelean, C. Bruschini, and E. Charbon are with EPFL, Switzerland (e-mail: francesco.gramuglia@epfl.ch, andrada.muntean@epfl.ch, , carlo.fenoglio@epfl.ch, a.ardelean@epfl.ch, claudio.bruschini@epfl.ch, edoardo.charbon@epfl.ch). E. Venialgo was with EPFL, Neuchâtel, NE 2002 Switzerland. He is now with TU Delft, Delft, Netherlands. S. Lindner was with EPFL, Neuchâtel, NE 2002 Switzerland. He is now with AMS, Zurich, Switzerland. M.-J. Lee was with EPFL, Neuchâtel, NE 2002 Switzerland. He is now with KIST, Seoul 02792, Republic of Korea (South Korea) (e-mail: mj.lee@kist.re.kr). M. Motoyoshi is with T-Micro, 980-8579 Sendai, Miyagi, Japan (e-mail: motoyoshi@t-microtec.com).
*The first two authors contributed equally. **The last two authors contributed equally.

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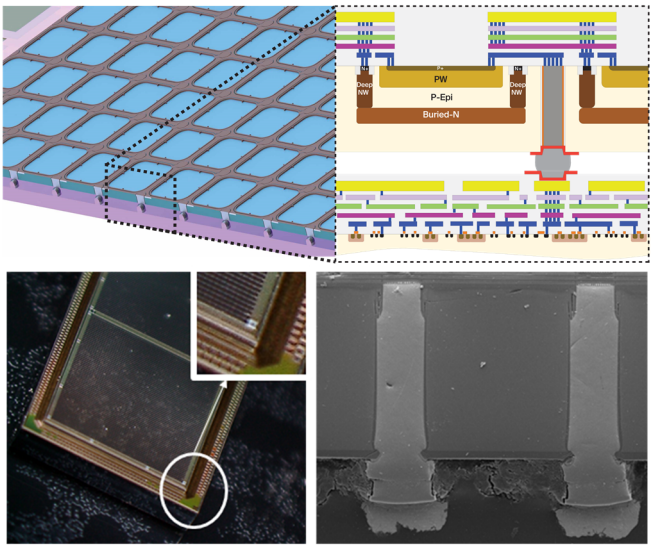

Fig. 1. *Top:* the top tier houses square SPADs with rounded corners and is 3D-stacked to the bottom-tier chip (*left*). The bonding with the bottom-tier chip is ensured through TSVs and micro-bump connections (*right*). *Bottom:* Optical microscope image of the final implementation *(left);* SEM image of the cross section (*right*).

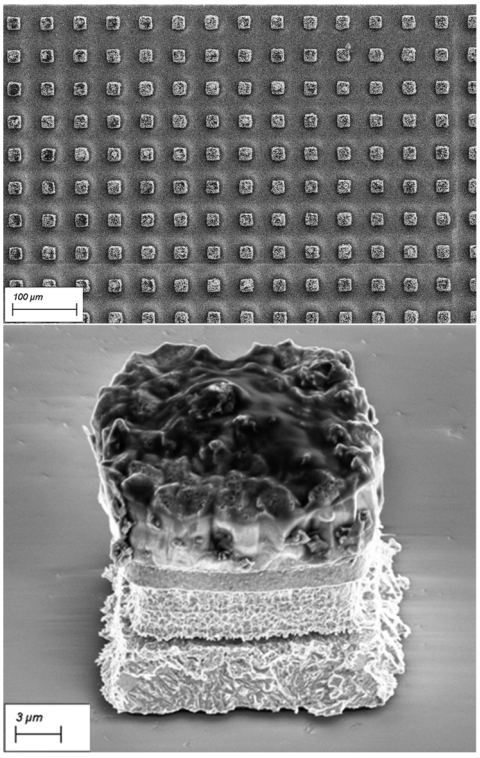

Fig. 2. *Top:* SEM images of the micropillars implemented on the back of the top tier. *Bottom:* detail of the micropillar structure.

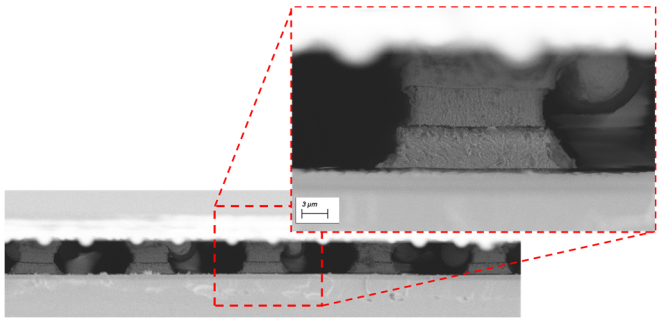

Fig. 3. SEM image of the micropillars used for 3D stacking and implementing the electrical connection between top-tier TSV and bottom-tier pixel frontend.

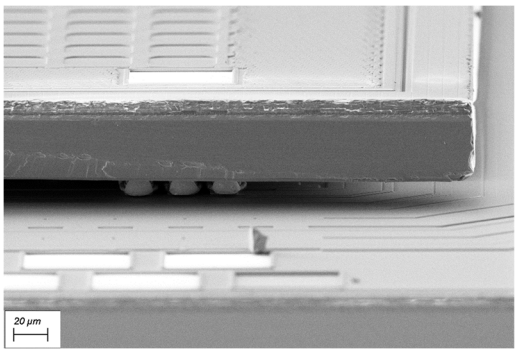

Fig. 4. SEM image showing a detail of the bonding pads on the top tier supported by micropillars beneath to improve reliability and mechanical stability during wire-bonding.

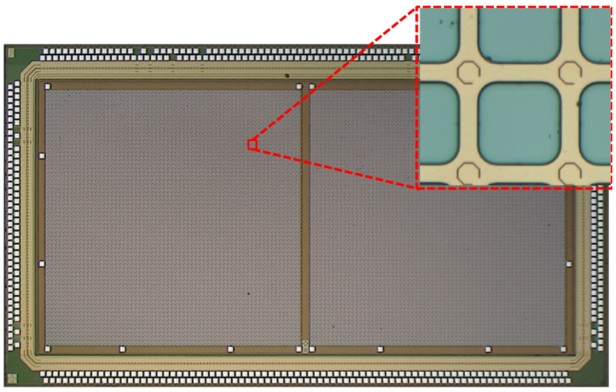

Fig. 5. MD-SiPM micrograph. The chip is partitioned in two independent segments including 4096 pixels each.

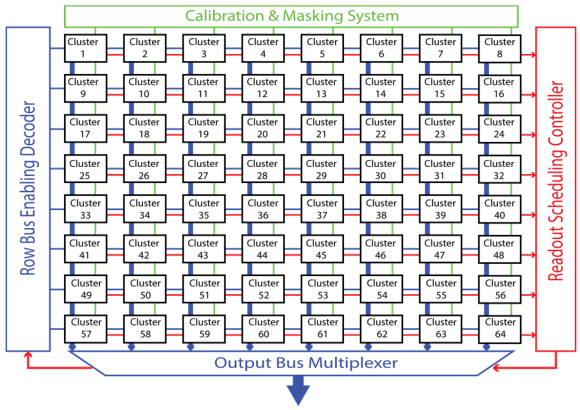

Fig. 6. Top-level architecture.

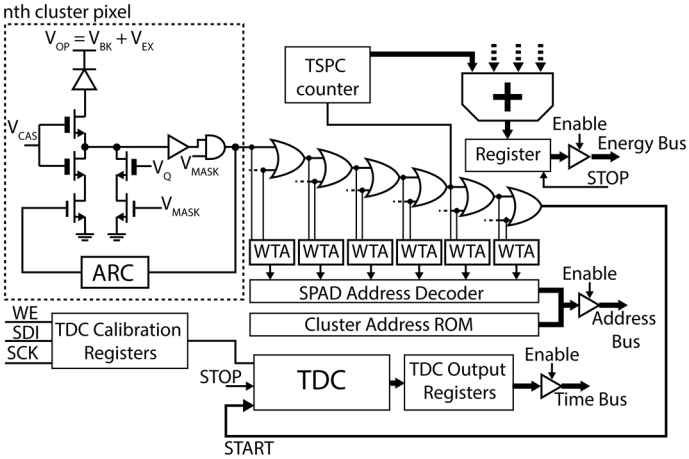

Fig. 7. Cluster architecture.

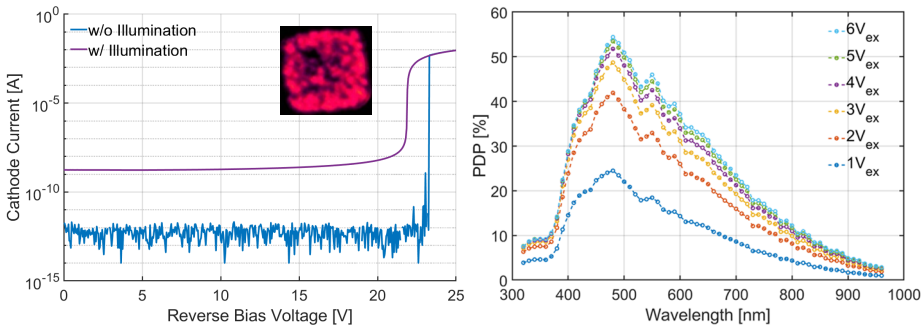

Fig. 8. *Left:* I-V characteristics measured on isolated SPAD samples. The measurements were performed both with and without illumination. The actual breakdown voltage is about 22 V, whereas the measurements without illumination tend to overestimate the voltage of breakdown. *Right:* PDP measurements for several excess bias voltages (from 1 V to 6 V) and wavelength (from 320 nm to 960 nm).

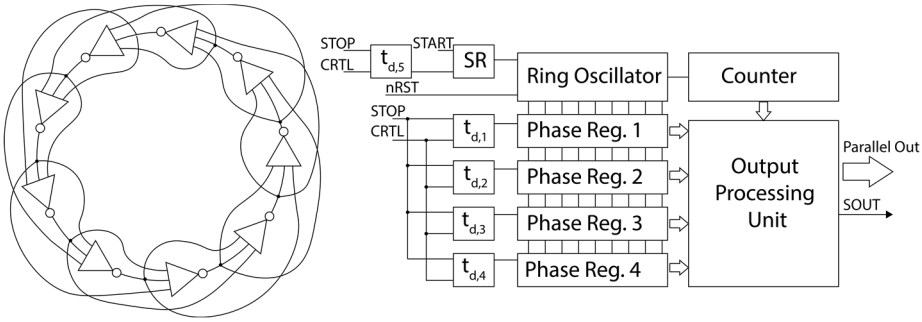

Fig. 9. *Left:* multipath ring oscillator simplified scheme. *Right:* TDC architecture scheme. The ring oscillator output is sampled by 4 sets of phase registers, triggered by a signal, which is delayed by a controllable block $t_{d,i}$. The four values are then input to a processing unit that calculates the final TDC code.