An Ultra-low current operating 5-µm Vertical Field Modulator Pixel for in-direct Time of Flight 3D Sensor

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Abstract

A 640x480 in-direct Time-of-Flight (ToF) 3D sensor is implemented in 90nm backside-illuminated CMOS image sensor technology. We achieved 80% demodulation contrast (Cmod) at 100MHz and 94% DC contrast with an ultra-lower operation current using the neo Pixel. This device shows depth error under 0.5% distance up to 3m with 940nm illumination and 140mW power consumption.

I. Introduction

As a number of applications, such as AI, IoT, robots, autonomous vehicles, drone, and AR/VR, continue to accelerate the fourth industrial revolution, the 3D depth information, which basically enables these applications, is becoming increasingly important. A recent 3D sensor trend shows the growing demand for high resolution to achieve higher accuracy and precision in order to apply the facial recognition technology for personal information security in a number of applications including mobile devices and automatic payments. 2D x-y information, as well as z information in a 3D depth sensor, are also becoming increasingly important in order to achieve a consistently high recognition rate at the wider field of view. In addition, a 3D depth sensor requires a faster modulation speed and a smaller pixel size. To satisfy these requirements, the adoption of in-direct ToF increased as it enables better processing speed and higher resolution. [1-3]. Among the various in-direct ToF methods, the current assisted photonic demodulator (CAPD), as a principle, uses the majority current to guide generated electrons by applying the substrate bias, and it shows a high transfer efficiency in a simple structure [3-4]. Compared to the photo-gate based pixel, in CAPD, the electric field penetrates deeper into the substrate, enabling a good charge separation. [5]. However, as the pixel size decreases, power consumption increases due to leakage current between the electrodes [6]. In this paper, we describe how we addressed this problem with a Vertical Field Modulator (VFM) in a 5um pixel pitch with 640x480 array using a 90nm backside-illuminated CMOS technology.

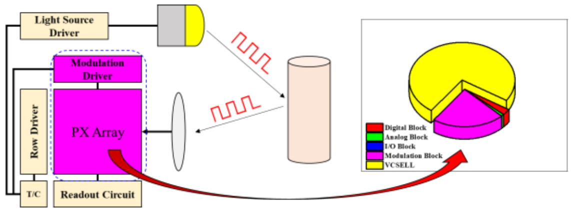
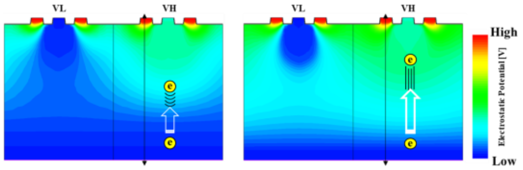


Fig. 1 Comparison portion of current by Sensor block

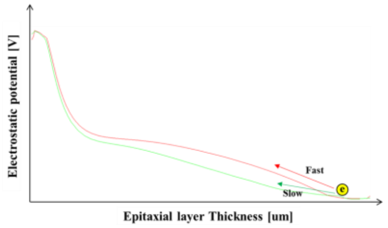
II. Pixel Design and Simulation

In in-direct ToF sensor, the depth is calculated by the ratio of the signal obtained through the high-speed switching operation of two or more taps. During the operation, the dynamic modulation peak current of the modulation driver circuit occupies the largest portion of the sensor power except VSCELL, as described in Fig. 1. The easiest and the most intuitive method to reduce the power consumption in the sensor is using a diffusion type pixel, such as CAPD, to lower the substrate current by increasing the resistance between the electrodes, and lowering the substrate doping concentration. However, as the majority current reduces, the electric field becomes weaker and the charge transfer efficiency deteriorates, making it difficult to accurately calculate depth. In order to overcome this trade-off, in this paper, we propose a new structure called a VFM Pixel. A VFM is a structure that strengthens the vertical electric field by using fully depletion, which occurs inside a substrate, and helps to move electrons located far away closer to the surface, so that those electrons can be detected without a high substrate current. In other words, in this structure, a lower current is sufficient enough to guide the electrons gathered on the modulation region. Fig. 2 shows the results of the 3D device simulation, and it shows that by applying a VFM design, a relatively higher electrostatic potential is formed below the vertical direction of the node to which the high voltage is applied. Therefore, the electrons generated relatively deeper in the photodiode can be easily and quickly collected within a short period as the transfer speed increases.



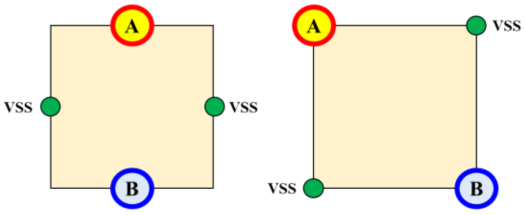
(a) Electrostatic Potential before applying VFM design

(b) Electrostatic Potential after applying VFM profile design



(c) Electrostatic 2D profile of DET to Back-side

Fig. 2 Electrostatic potential by pixel design



(a) The Straight structure VFM (S-VFM)

(b) The Diagonal structure VFM (D-VFM)

Fig. 3 Comparison Pixel Design

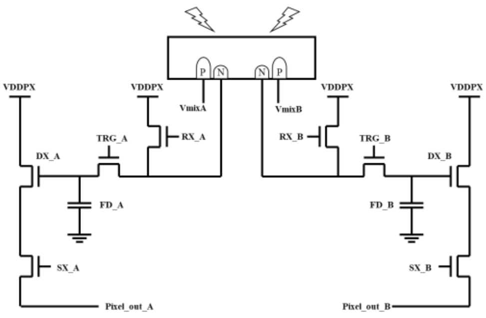


Fig. 4 Pixel schematic

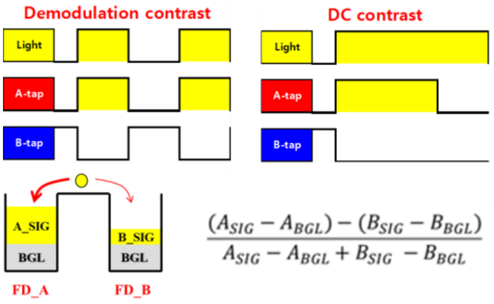


Fig. 5 Measurement method of Cmod and DCC

III. Pixel Architecture and Key Parameters

Fig. 3 shows two pixel structures designed to find a way to maximize the advantages of VFM. In the first structure, two-taps were arranged straight similar to usual devices, and in the second structure, two-taps were arranged diagonal to another. The two taps constituting the pixel are usually arranged vertically or horizontally, but a method was devised to arrange them in a diagonal direction to maximize the current path. The second structure, in which taps are placed at two corners of the unit pixel facing each other to create a maximum distance in the same area, is the final structure that we propose. For convenience, this paper intends to name this structure the Edge Pixel (D-VFM).

As mentioned earlier, the in-direct ToF sensor power consumption depends on the modulation peak current (IDDMD). The pixel ion implant split experiment results confirm that the IDDMD changes by the well doping profile of the detector. Based on results, the IDDMD is divided by the number of pixel arrays, and the level of the majority current flowing during pixel operation can be predicted and compared. The most important role of depth sensor is to obtain the depth information accurately and in a uniform manner. Signal to noise ratio (SNR) and demodulation contrast (Cmod) are key parameters of pixel that determine depth characteristics [3]. In particular, it is important to increase the Cmod value as much as possible, as it indicates how well the tap distinguishes signals in each phase. Albeit difficult in reality, its value can reach up to 100% in theory, and a higher value is regarded to be better. Another parameter that predicts the pixel transfer efficiency is DC contrast (DCC), which enable faster evaluation because the measurement method is simple and correlates well with the device simulation. Fig. 6 shows a photograph of the chip of a VGA VFM Pixel for i-ToF sensor. For the major indicators described above, mass data was obtained at the wafer level test to compare the pixel characteristic between the two structures and the verification was done by

CoB (Chip-on-Board) module evaluation with the better of two pixels.

$$\sigma_{depth} = \frac{1}{\sqrt{2} \cdot SNR} \cdot \frac{1}{2\pi} \cdot \frac{c}{2 \cdot F_{mod}}$$

$$\mathrm{SNR} \equiv \frac{A_{pix} \cdot RE \cdot FF \cdot C_{mod} \cdot \Phi_{active} \cdot t_{int} \cdot \frac{1}{q}}{\sqrt{\left(A_{pix} \cdot RE \cdot FF \cdot (\Phi_{active} \cdot \Phi_{ambient}) \cdot t_{int} \cdot \frac{1}{q}\right) + \left(N_{system}\right)^2}}$$

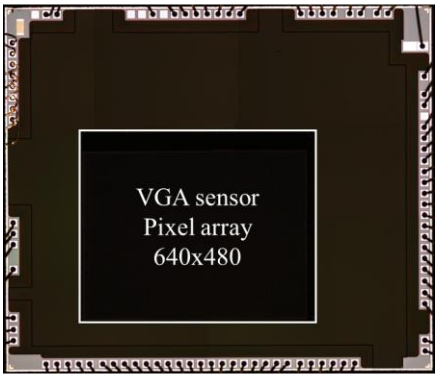


Fig. 6 Chip photograph of VGA Pixel i-ToF Sensor

III. Results and Discussion

Fig. 7 shows the result of the wafer-level test with different pixel structures. This results shows the comparison of modulation peak current by the modulation frequency (Fmod). The Edge Pixel had IDDMD, one tenth lower compared to the other structure in Low Fmod, and 70% lower IDDMD in High Fmod. Even with reduced IDDMD, the Edge pixel achieved better DC contrast and Cmod than S-VFM Pixel. In addition, the Depth error and the Phase Responsibility Non-Uniformity (PRNU) of Edge Pixel improved with the low operating current. Based on the above results, we chose the Edge pixel to fabricate a CoB module and verified it in an actual operating environment. Fig. 8 shows the measurement result of Cmod, which shows 80% at 100MHz. Fig. 9 shows the measurement result of the distance and the calculated depth error. When measured from 30 cm to 3 m, an average depth error of 0.47% was obtained. Finally, we measured power consumption and the dynamic modulation peak current at 100MHz. As described in Fig. 10, we could confirm that the D-VFM structure has a lower modulation peak current than S-VFM, and that the power consumption is also dependent on IDDMD. This Device, in which the Edge Pixel was applied, had a lower power consumption than the previous work.

As a result of this, it can be seen that in the VFM, the substrate current no longer has a major effect on the separating ability of the pixel, and only serves as a guide to collect electrons well during the activation. In particular, when the taps are placed diagonally, at each corner facing each other, the vertical field affects the entire area of the pixel and it is possible to effectively suppress the leakage current between the electrodes, thereby dramatically reducing the substrate current and keeping a good contrast efficiency. This study shows the combination of an optimized layout structure and the pixel implant design that can make the most of the intended VFM operation.

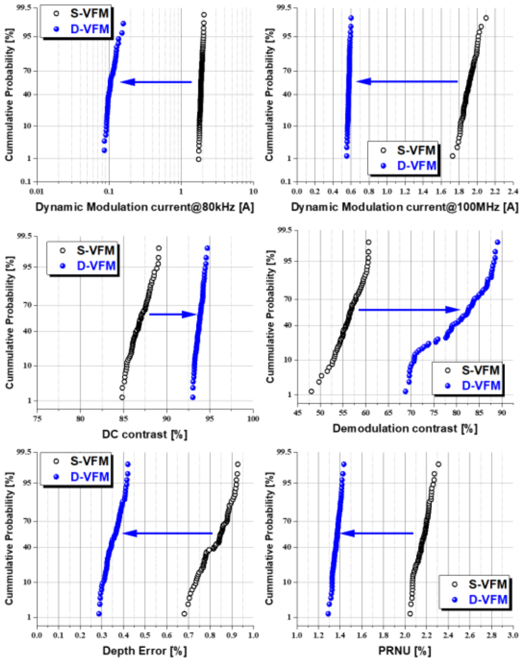


Fig. 7 Comparison Pixel characteristic by Structures

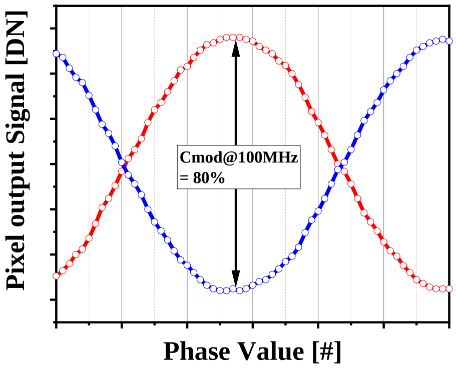


Fig. 8 Demodulation contrast at 100MHz

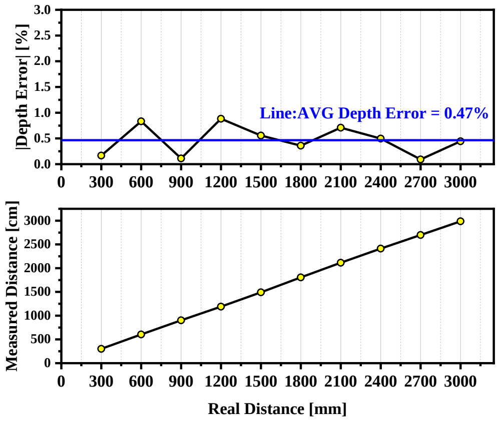


Fig. 9 Depth error result from 30cm to 3m

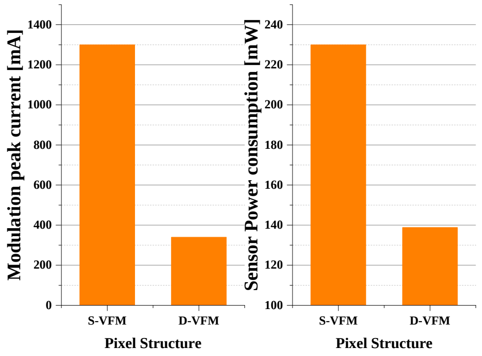


Fig. 10 IDDMD dependency of power consumption

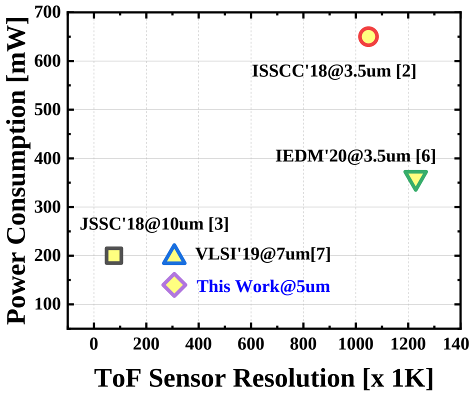


Fig. 11 Comparison Power consumption with the previous work

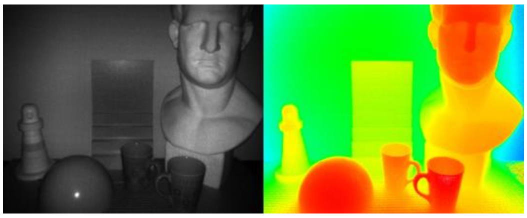


Fig. 12 Depth image sample

IV. Conclusion

In this work, we proposed the development of 5-um Pixel in-direct ToF Sensor optimized for VFM architecture. As the pixel size decreases, we studied in depth to find ways to reduce power consumption as much as possible from the device and layout point of view. As a result, in addition to the anticipated power consumption reduction, we were able to obtain a good depth performance and demodulation contrast even in a low-power operation.

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