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A Partial-Multi-Conversion Single-Slope ADC with Response-Linearized RDAC

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ABSTRACT This paper proposes a Single-Slope column ADC (SSADC) for CMOS Image Sensors (CIS). The response-linearized DAC using digital step pulse injection can realize a fast and accurate ramp wave without increase of power dissipation (P_d). Low P_d of 0.9 µW for a comparator is achieved with a resistive DAC (RDAC). The multi-conversion method is applied only for weak signal of less than 30 mV without significant increase in the conversion time, T_c. As a result, a 12bit SSADC attains a low noise of 32.5 µV and a low P_d of 34 µW while using 8 conversions at the T_c of 4 µs. A high dynamic range of 90 dB and a high Schreier FoM_S (DR) of 183 dB are attained with small size of 3.2 µm x 556 µm in 65 nm CMOS.

KEYWORDS: ADC, DAC, LOW NOISE, LOW POWER, CMOS, SENSOR, IMAGE SENSOR, COLUMN ADC, FOM.

I. Introduction

A SSADC is a major column-ADC architecture used in CIS owing to its extremely short pitch and small area and channel mismatch. It however, continuously receives the demand for low noise operation [1]. On the other hand, it is exceedingly difficult to reduce the noise of the SSADC caused by the comparator. Fig. 1 shows a simplified comparator circuit for the SSADC.

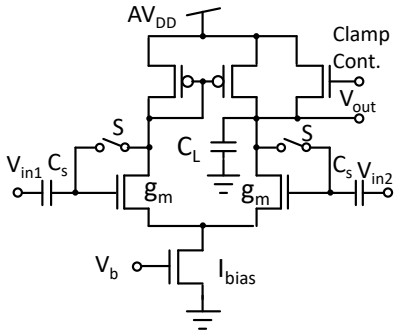

Fig. 1 Comparator circuit for the SSADC.

We have deduced the following noise equation at Correlated Double Sampling (CDS) operation [2].

$$\overline{v_{nc}} = \sqrt{8\sqrt{2}kT\gamma n_e}\left(\frac{V_{FS}}{2g_m V_{CL} C_L T_c}\right)^{0.25} \quad (1)$$

where, k: Boltzmann constant, T: temperature, γ: noise factor, n_e: effective number of transistors, V_{FS}: full scale ramp voltage, g_m: transconductance, V_{CL}: clamp voltage, C_L: load capacitance, T_c: conversion time. Fig. 2 shows our estimated noise by (1) is well matched with the simulation and the comparator noise can't be reduced easily mainly due to the power of 0.25 affecting the parameters in (1). Thus, the lowest noise is about 120 µV at T_c of 1µs. Also increase of analog gain by reducing slope rate of the reference voltage is not efficient to reduce the noise. Noise voltage is about 2/3 if T_c is 16 times longer.

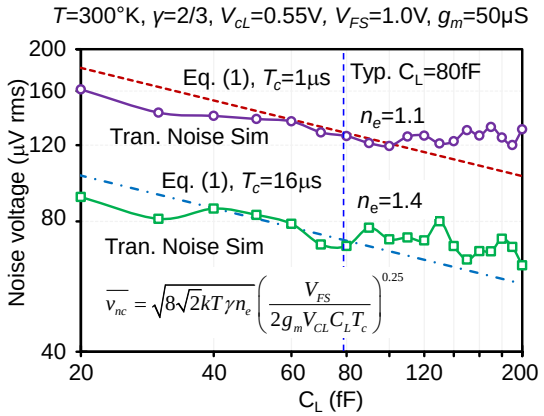

Fig. 2 Noise voltage vs. load capacitance.

The Shreier's FoM is based on physics for energy vs. noise. We estimated power dissipation vs noise voltage by using FoM_S in consideration of CDS effect that the operation time is 1.5 T_c and the noise voltage is 1.4 times larger and those reduce the FoM_S by 4.8 dB. Fig. 3 shows the estimated P_d vs. noise voltage for the world's top FoMs (SNR) of 185 dB and practical FoM_S of 180 dB and 175 dB [3] at T_c of 4 µs. The P_d is rapidly increases with reducing the noise voltage. The P_d of current SSADC [1] is about 8 times larger than the estimation with FoM_S of 175 dB.

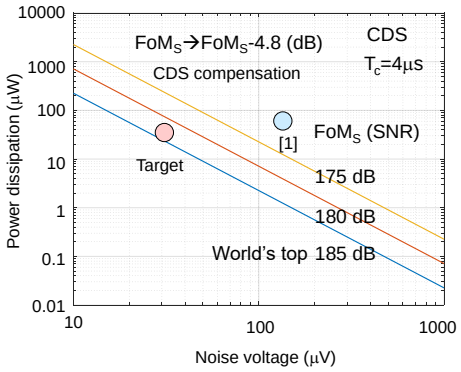

Fig. 3 Estimated power dissipation vs. noise voltage.

Our target (32 μV, 35μW) is almost on the line of the world's top FoM_S and looks difficult to realize it. Another scenario for A/D conversion method is required.

II. Partial-multi-conversion method

A multi-sampling method has been well known to reduce the readout noise in CIS [4]. The random noise voltage can be reduced by increasing the number of samplings, M. As a result, T_c is increased by increasing M. It limits the application to the moving picture. For example, noise voltage of 75 μV was obtained by M of 5, however T_c is 27 μs and the frame rate is only 7.2 frams/s [5].

Fig. 4 shows our proposed Partial-Multi-Conversion (PMC) method. Two DACs, one is a Local DAC (LDAC) for converting limited voltage range and the other is a Global DAC (GDAC) for full voltage range are used.

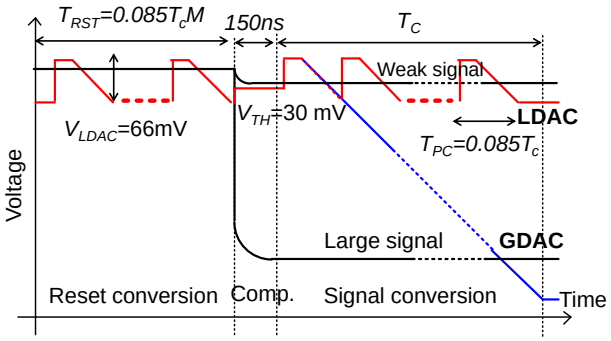

Fig. 4 Partial-Multi-Conversion (PMC) method.

The SSADC converts the reset signal M times with LDAC during reset-conversion within a limited range of about 66 mV. Next, the signal is compared to the threshold voltage, V_{TH} of 30 mV within about 200 ns in order to select the LDAC or the GDAC. The GDAC is selected to convert the full range of 1.0 V for large signal. The LDAC is selected to convert the weak signal M times within a partial range of about 66 mV. The threshold voltage should be determined by considering the shot noise. Fig. 5 shows the signal voltage, the shot noise of the photo-diode at the conversion gain of 30 μV/e^-, and the ADC readout noise.

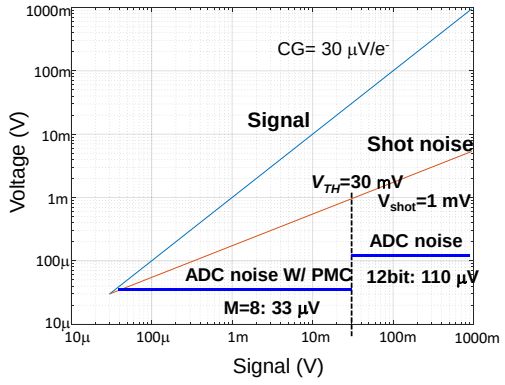

Fig. 5 Signal, shot noise, and ADC noise.

The shot noise at the threshold voltage of 30 mV is about 1 mV. The ADC noise is low enough compared to the shot noise and the SSADC has a sufficient voltage margin to tolerate the error voltage at the DAC switching point.

The proposed PMC method only requires extra conversion time during the reset conversion period and doesn't require it to the signal conversion period. However, the required reset time is only 3.0 μs for T_c= 4.0 μs and M= 8. Furthermore, the proposed PMC method can reduce the pixel noise as well as the ADC noise. The noise power transfer function NTF is

$$NTF(\omega) = \left|1 - e^{-j\omega T_{CDS}}\right|^2 \left|\frac{1 - e^{-j\omega M T_{PC}}}{1 - e^{-j\omega T_{PC}}}\right|^2 \quad (2)$$

where T_{CDS} is the period of CDS and T_{PC} is the period of the partial multi conversion. Therefore, the PMC can additionally suppress the high frequency noise components of the1/f noise, as shown in Fig. 6.

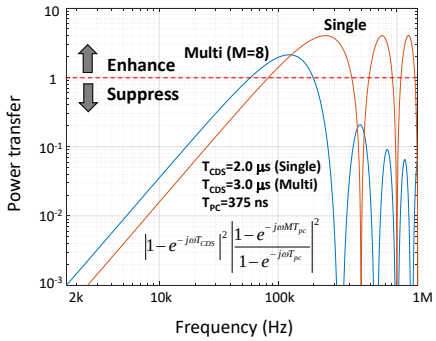

Fig. 6 Noise power transfer of the PMC.

III. Response-linearized RDAC

A fast and accurate ramp signal generation is vitally required for the PMC. However, the nonlinearity of the response caused by RC delay deteriorates the accuracy of the ramp waveform. Conventionally, the reduction of output resistance or voltage buffer are used but this results in an increase of P_d. We have solved this issue by controlling the input data of the DAC. Fig. 7 shows the DAC including an RC circuit at the output terminal.

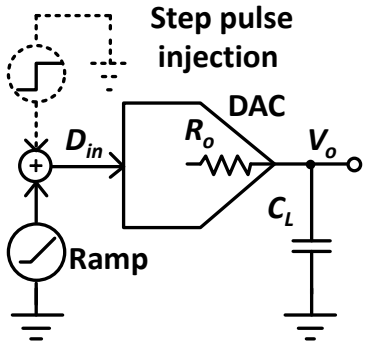

Fig. 7 DAC including an RC circuit at the output.

The output voltage V_o to the input ramp data is

$$V_o(t) = S_R \cdot t - S_R \cdot \tau\left(1 - e^{-\frac{t}{\tau}}\right) \quad (3)$$

where S_R is the slew-rate of the ramp signal and τ is the time constant of R_oC_L. Fig. 8 shows the input and output waveforms of the conventional and the proposed DAC. The output voltage of the conventional DAC is delayed and distorted. The second term in (3) expresses the error and it can be cancelled by injecting the digital step-pulse to the input of the DAC.

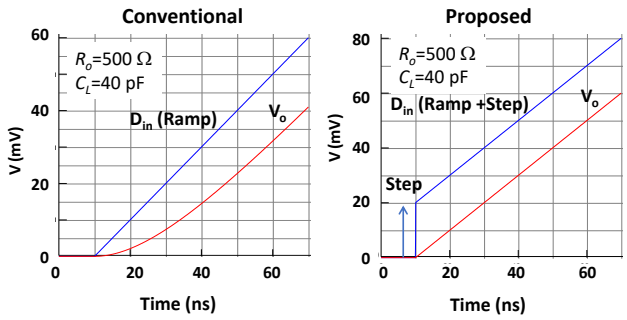

Fig. 8 Input and output waveforms of the conventional and the proposed DAC.

The delay and distortion of the proposed DAC are clearly canceled without any increase in P_d, if the digital step pulse is injected to the DAC. Fig. 9 shows the P_d is 8 times lower while achieving the same INL for the LDAC.

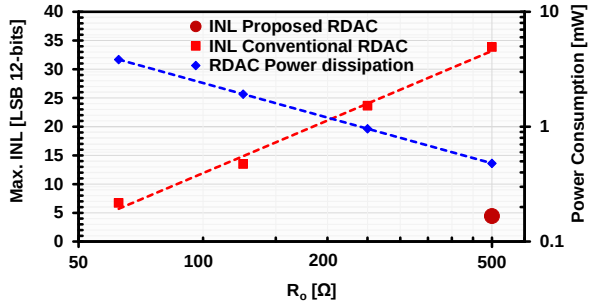

Fig. 9 Linearity and power dissipation vs. R_o in DAC.

The digital calibration can find the optimal value for the injection step within a short time of 4 μs to linearize the DAC response.

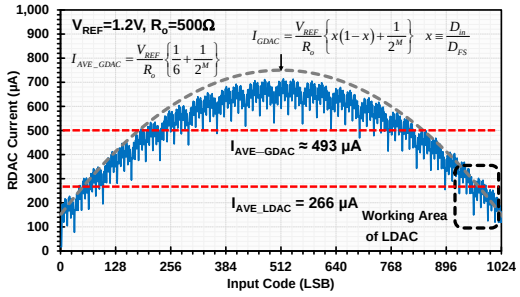

Fig.10 Currents of the GDAC and the LDAC.

Furthermore, we used an RDAC instead of a conventional current DAC (IDAC) to reduce the P_d. Fig. 10 shows the power supply current of the 10bit RDAC vs. input code. The average currents of GDAC and LDAC at R_o of 500 Ω are only 493 μA and 266 μA. Those are 1/4 and 1/8 of the conventional IDAC. Two RDACs consume only 0.9 mW in total and 0.9 μW for each comparator.

IV. SSADC and test chip design

Fig.11 shows the SSADC and Fig. 12 shows the clocks for the Time to Digital Converter (TDC). The comparator uses a conventional cascode amplifier with DAC selection switch. A 4bit TDC uses four dual-edge Gray-code clocks to reduce the P_d. The average P_d of the ADC is 34 μW.

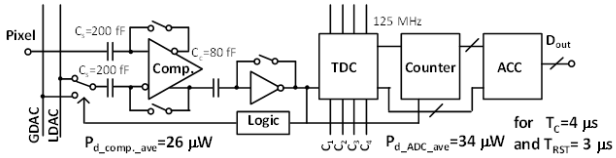

Fig. 11 Block diagram of the SSADC.

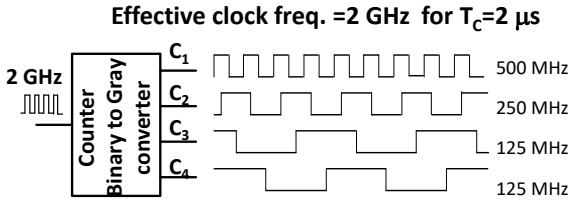

Fig. 12 Dual edge Gray-coded clocks for the TDC.

The size of the ADC is 3.2 μm x 556 μm, and the test chip integrates 960 ADCs in 65nm CMOS, as shown in Fig. 13.

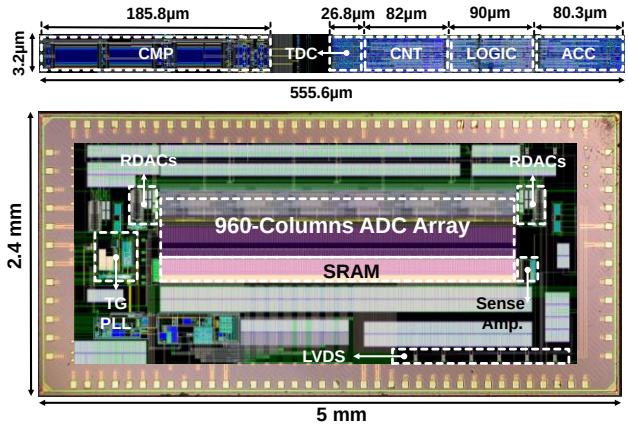

Fig.13 Layout of the SSADC and photo of the test chip.

V. Experimental results

Fig. 14 shows the measured noise voltages after CDS for T_c=2, 3, 4 μs and M=1, 2, 4, 8. At T_c=4 μs, the noise voltage with M=1 is about 120 μV and almost same as the

simulated value. The noise can be reduced to 32 μV when M=8. At T_c=2 μs, the noise voltage with M=1 is about 300 μV, which is three times larger than the simulated value. However, the multi-conversion still works and a noise voltage of 70 μV is obtained when M=8.

Fig. 15 shows the output codes of the ADC around the V_{TH} crossing point for the nearest and the farthest ADC from the DAC. The worst-case gap voltage is 230 μV and well below the shot noise of 1 mV. Measured DNL and channel mismatch are only 0.08 LSB both. Power dissipation of ADC and DAC with CDS at T_c= 4 μs and M=8 is 34 μW and 0.9 μW for one column. The dynamic range is 90 dB and the Schreier FoM_S is 183 dB (DR) and 174 dB (SNR). This performance is competitive compared to CT ΔΣ ADCs for sensors [6] while the area the SSADC is 150 times smaller. Table 1 summarizes the performance.

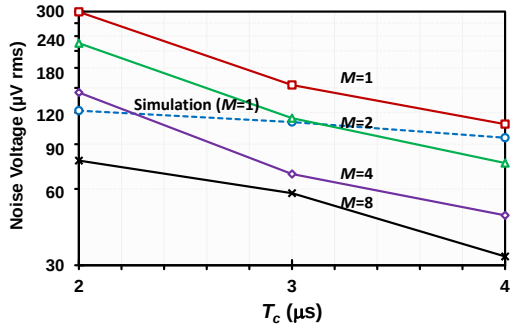

Fig. 14 The measured noise voltages vs. T_c after CDS for T_c=2, 3, 4 μs and M=1, 2, 4, 8.

VI. Conclusion

The response-linearized RDAC using digital step pulse injection can realize the fast and accurate ramp wave. Small P_d of 0.9 μW in the DAC for a comparator is achieved.

Table 1. Performance summary and comparison.

	This work			[1]	[5]	[6]
ADC architecture	SS			SS in CIS	SS in CIS	CT ΔΣ
Resolution (bit)	12			12	11	
Full scale voltage and LSB voltage:	1.0 V(Full), 244 μV (LSB)			923 mV, 225 μV		
INL: p-p (LSB) and DNL: σ (LSB)	-2.4/2.2 (INL), 0.08 (DNL)					
Channel mismatch voltage: σ (LSB)	0.08					
Worst-case voltage gap at V_{TH} for T_c=4 μs: p-p (μV)	230					
P_d of GDAC+LDAC and P_d for one comparator	0.9 mW , 0.9 μW/comp.			32 μW/comp.		
Period of reset conversion for T_c=4 μs and M=8 (μs)	3.0					
P_d (μW) and E_d (pJ/conv.) of ADC w/ CDS for T_c=4 μs and M=8	34 (P_d), 237 (E_d)			48.8, 341 estim.		55, 1375
Area of ADC (μm^2)	3.2 x 556 =1,778					270,000
Conversion time T_c: (μs)	2.0	3.0	4.0	1.53	27.6	25
V_n (μV) rms at M=1	299.0	154.0	108.0	140.0		
V_n (μV) rms at M=2	225.0	114.0	75.9			
V_n (μV) rms at M=4	143.9	68.7	47.2		73 (M=5)	
V_n (μV) rms at M=8	77.6	57.7	32.5			
Dynamic range and SNR for T_c=4 μs and M=8 (dB)	90 (DR), 81 (SNR)			76.3 (DR)		93 (DR)
FoMs(DR) and FoMs(SNR) w/ CDS for T_c=4 μs and M=8 (dB)	183 (DR), 174 (SNR)			167 (DR) estim.		179 (DR)

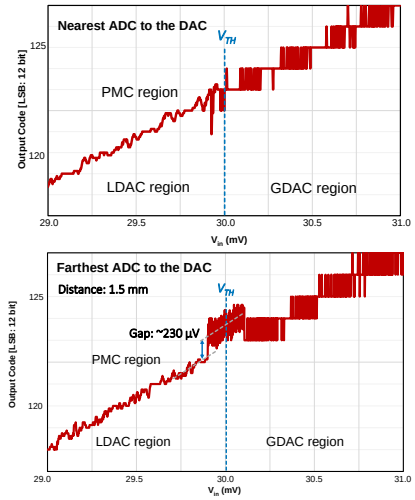

Fig. 15 Measured ADC outputs around V_{TH}. (Nearest and furthest from the DAC.)

The partial multi-conversion method with a 12bit SSADC attained a low noise of 32.5 μV and a low P_d of 34 μW at T_c =4 μs and M=8 with CDS. A high dynamic range of 90 dB and a high Schreier FoM_S (DR) of 183 dB are attained.

Acknowledgement

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