Image sensor with V-shape deflector structures for sensor edge performance improvement

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ABSTRACT

High edge-performance sensor with a three-layer V-shape deflector (VSD) structure is demonstrated in a high resolution CMOS image sensor (CIS) with a 0.8um pixel pitch. The three-layer VSD structure improves the quantum efficiency (QE) of CIS by 15.3% in the chief ray angle (CRA) 30˚ and has a maximum efficiency improvement gain of 1.27 times at CRA 28˚.

I. INTRODUCTION

The camera specifications of smart phones nowadays are getting higher and higher. More CIS pixels and thinner camera modules will be the trend in the future [1-3]. When the number of pixels is increased and the size of the camera module is limited, the pixel size of the CIS must be reduced [4]. When the camera lens has a wide CRA, the sensor edge performance of small pixel CIS is often poor. It is because the wide-angle incident light entering the CIS is absorbed by metal grid and scattered by deep-trench isolation, and hence the photons cannot reach the photo diode [5]. In this paper, we demonstrated a three-layer VSD structure on a CIS to improve the QE of CIS by 15.3% at CRA 30˚.

II. V-SHAPE DEFLECTOR

The three-layer VSD structure, which is on the microlens (ML), is composed of an anti-reflection layer, a high refractive index layer, and a low refractive index layer from top to bottom. The angled facets of the VSD structure deflect the light to smaller angles and enter pixels efficiently at CIS edge.

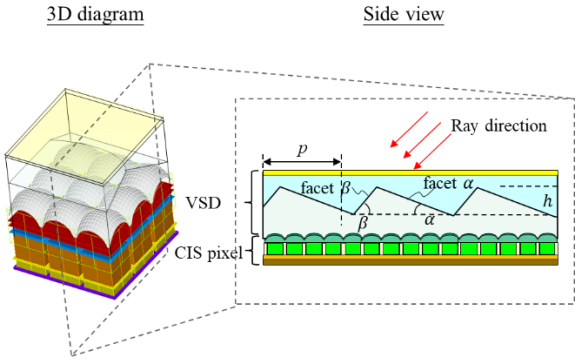


Fig. 1 Schematic diagram of the VSD structure

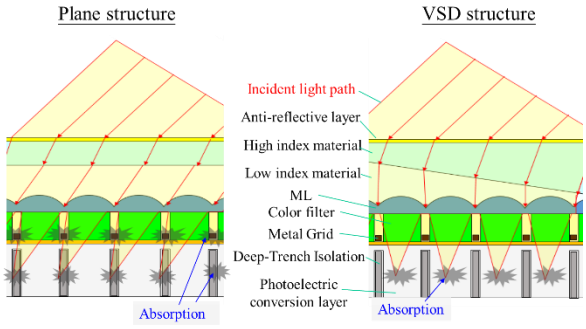


Fig. 2 Optical path schematic diagram of the planar structure and VSD structure.

Fig. 1 shows a schematic diagram of the VSD structure, where α, β, *h*, *p* are the main angle, secondary angle, height and period of VSD, respectively. The angle α and β of VSD have

been designed to control the angle of light entering ML. Fig. 2 shows the optical path diagram of the planar structure and VSD structure. When the wide-angle incident light passes through the metal grid and deep-trench isolation, the most light cannot reach the photoelectric conversion layer. The VSD structure can collimate the light and let more light energy enter the photoelectric conversion layer.

III. SIMULATION & EXPERIMENT

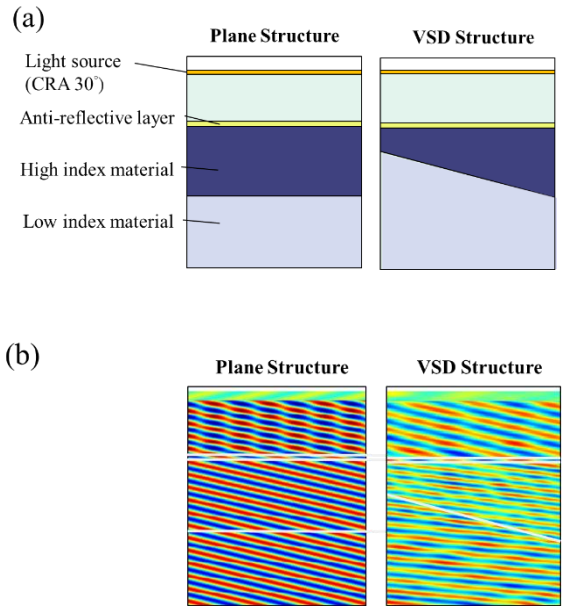


Fig. 3 (a) Schematic diagram of simulation module and (b) Electric field simulation figure with incident light angle 30°

A software of 3D Electromagnetic wave solver is used for VSD and CIS simulation. The model of three-layer VSD structure is constructed on the ML of CIS, where the pixel size of CIS is 0.8um. The high and low refractive index layers on ML allows deflection of light while the function of focusing light is kept. A lower refractive index layer is added on the top for anti-reflection. Fig. 3 shows the electric field simulation with/without VSD for incident light angle 30°, $\alpha\ 30^{\circ}$ and wavelength 550nm. Compared with the planar structure, the electric field propagation angle of the VSD is smaller. Fig. 4 shows the electric field simulation figure with CIS pixels, where Fig. 4(a) is plane structure and Fig. 4(b) is VSD structure. It can be seen from the figure that the VSD structure makes the energy propagate deeper. To understand the effect of the VSD structure, we consider that parameters of VSD structure are $\alpha\ 30^{\circ}$, $\beta\ 76^{\circ}$, h 1.6um, and p 7.2um. The VSD structure is realized with lithograph and etching process. Fig. 5 shows the SEM picture of VSD after lithography patterning, where (a) is the top view, (b) and (c) are the cross section. The VSD has a perfect angle and a smooth facet after lithography patterning. Fig. 6 shows the SEM picture of VSD after etching process with 0.8um pixels. The top corner of the VSD is rounded and the inclined plane is rough after etching process due to the material characteristics.

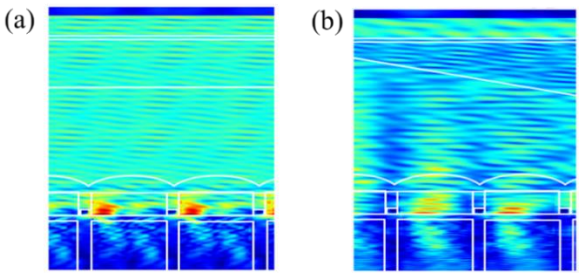


Fig. 4 Electric field simulation figure with CIS pixels, (a) plane structure and (b) VSD structure

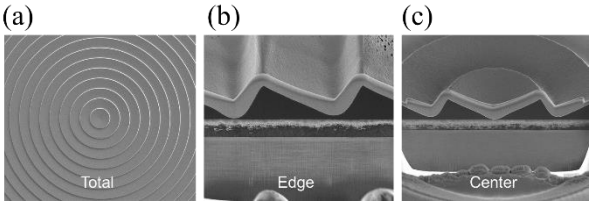


Fig. 5 SEM picture of VSD after lithography patterning, where (a) is the top view, (b) and (c) are the cross section

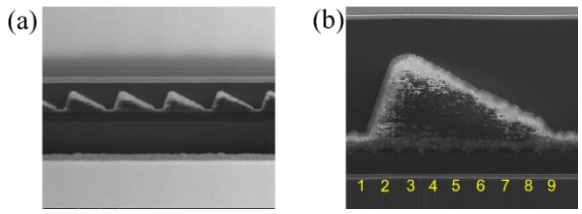
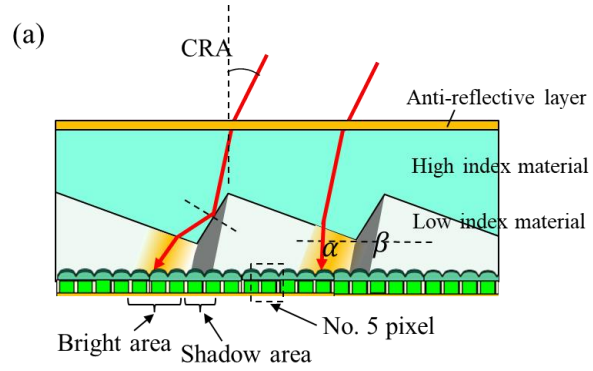


Fig. 6 SEM picture of VSD after etching process, where α 30°, β 76°, h 1.6um and p 7.2um

IV. RESULTS



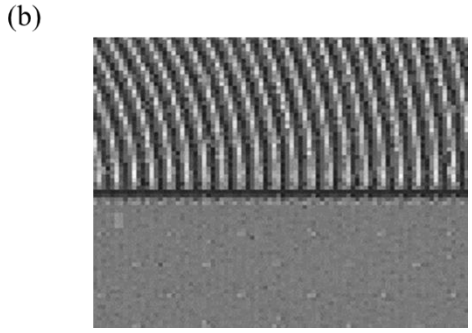


Fig.7 (a) schematic diagram of the TIR light path on facet β, (b) blank photo by the CIS with VSD

The rounding of top corners and total internal reflection (TIR) on facet β are issues of uniformity. The rounded top corners produce focused light. If the light angle does not meet the design, TIR can be generated on the facet β according to the light path analysis. Fig.7 (a) shows a schematic diagram of the TIR light path on facet β. Fig.7 (b) shows a blank photo by the CIS with VSD structure, where the upper part has a VSD structure, and the lower part is the CIS with plane structure. We can find that the VSD structure produces uneven black lines on the photo. In order to avoid the uneven black lines affecting the experimental data, we collect data of the no. 5 pixel for analysis. Fig. 8 (a) shows the measured angular response with normalization. There are not shifting design between ML and photo diode. When comparing the results from VSD and plane structure, the efficiency is improved by 15.3% at CRA 30°, where the efficiency of VSD and plane structure are 75.0% and 59.7%. Fig. 8(b) shows the efficiency improvement between VSD structure and plane structure, where the VSD structure has a maximum gain of 1.27 times at CRA 28°. Therefore, it can be seen from experiments that VSD can greatly increase the optical efficiency on the edge of CIS.

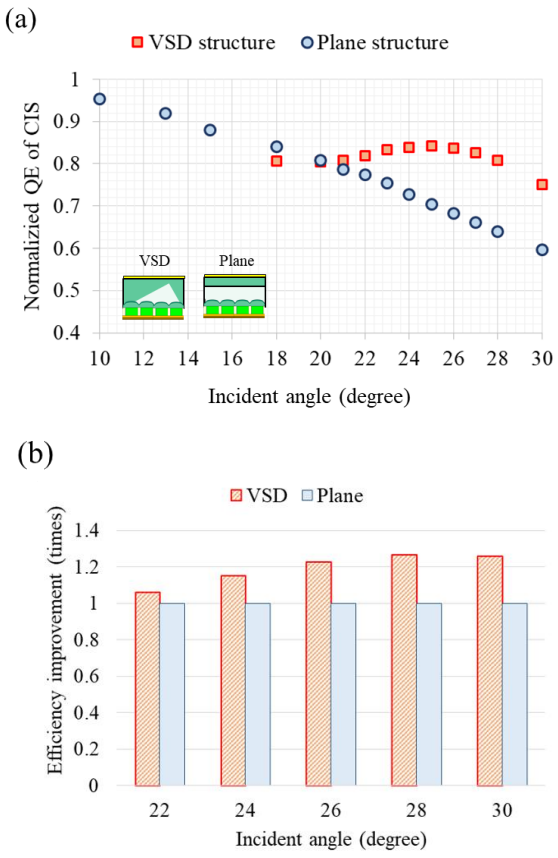


Fig. 8 (a) QE angular response measurement data, (b) efficiency improvement between VSD structure and plane structure

V. CONCLUSION

In this paper, we demonstrated a three-layer VSD structure on a CIS. The VSD structure improves the QE by 15.3% at CRA 30° and has a efficiency improvement gain of 1.27 times at CRA 28°. Obviously, the VSD has the function of improving edge performance, but we need to solve the issue of uneven black lines on CIS also. We believe that one of the ways to eliminate the uneven black lines is to reduce the VSD structure size to the pixel size. However, the manufacturing technical will be a challenge.

VI. ACKNOWLEDGMENT

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