An Extremely High-Speed and Low-Power Digital Pixel Sensor with Advanced Sensor Architecture

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Abstract - This paper presents an extremely high-speed of 1200 fps global-shutter (GS) CMOS image sensor (CIS). A GS CIS is a great alternative to solve image distortion issues caused by a conventional rolling-shutter (RS) CIS operation, since a 2-dimensional image data can be simultaneously sampled by the in-pixel analog memory. In order to achieve a high speed global-shutter operation, we proposed a novel architecture, using a pixel-wise ADC and an in-pixel digital memory, for the digital pixel sensor (DPS) which is a remarkable global-shutter operation CIS. Within 4.95-μm, one ADC and 22-bit memories are integrated by using two small-pitch Cu-to-Cu interconnectors for the wafer-level stacking. The 2-mega pixels (Mp) array, 1668H×1364V, prototype image sensor is successfully fabricated and demonstrated.

I. Introduction

Rolling shutter (RS) CMOS image sensor (CIS) is being widely used as an image capture device for various applications. However, to capture any fast moving objects, it is fairly difficult to avoid the Jello effect, which is an image distortion caused by the difference of the exposure times of each subsequent rows of pixels in RS operation mechanism. This is the critical reason why the RS CIS is mainly used to capture still or slow-moving objects. On the other hand, global shutter (GS) CIS has simultaneous exposure time for the entire array, therefore, it enables to capture an entire image at a single instance without any image distortion. Due to such reason, the demand for GS CIS is being increased in a variety of fields such as broadcasting, industry, mobile and automotive applications. GS CISs are normally implemented by using in-pixel analog memory such as storage diode [1] or capacitor [2]. However, conventional GS CISs still use column-parallel readout circuits same as the one used in RS CIS. It is difficult to achieve high frame rate and low power. Because every pixel at same column is sharing the same single analog-to-digital converter (ADC) and each pixel's analog signal should be converted to the digital data through the column-parallel ADC within a short time, typically less than 5-μsec. As another means of realizing GS CIS, the

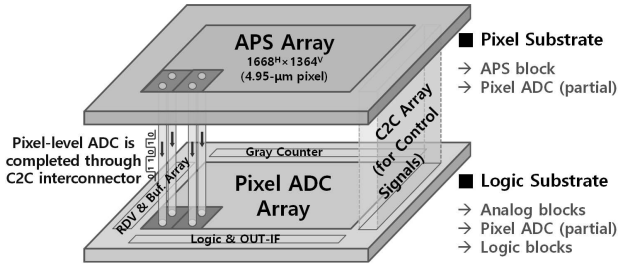


Figure 1. Block diagram of the proposed 2-stack DPS.

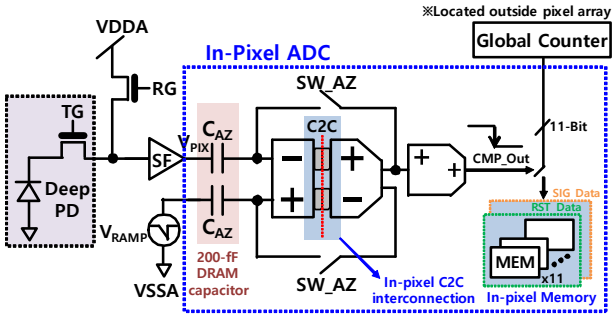


Figure 2. Schematic diagram of in-pixel ADC.

digital pixel sensor (DPS) employing pixel-parallel ADCs have been reported [3, 4]. They successfully show the feasibility of high-speed and low-power GS operation, however, those are not quite yet proper to be used in image sensor which requires large pixel array and sufficiently low random noise operation.

This paper presents the advanced DPS architecture [5], which can overcome problems of conventional GS CIS and DPS, and it has been successfully demonstrated by full chip-level evaluations. The rest of this paper has been organized as the following. Section II describes the architecture of proposed DPS and its operation. Section III shows the simulation and experimental results of the prototype imager. Finally, the conclusion is given in Section IV.

II. Architecture of imager

Three main techniques, 1) a pixel-level Cu-to-Cu (C2C) bonding, 2) single-slope (SS) ADC operating in sub-threshold region, and 3) 22-bit in-pixel digital memories and high-speed data transfer method for a true correlated double sampling (CDS), are used to

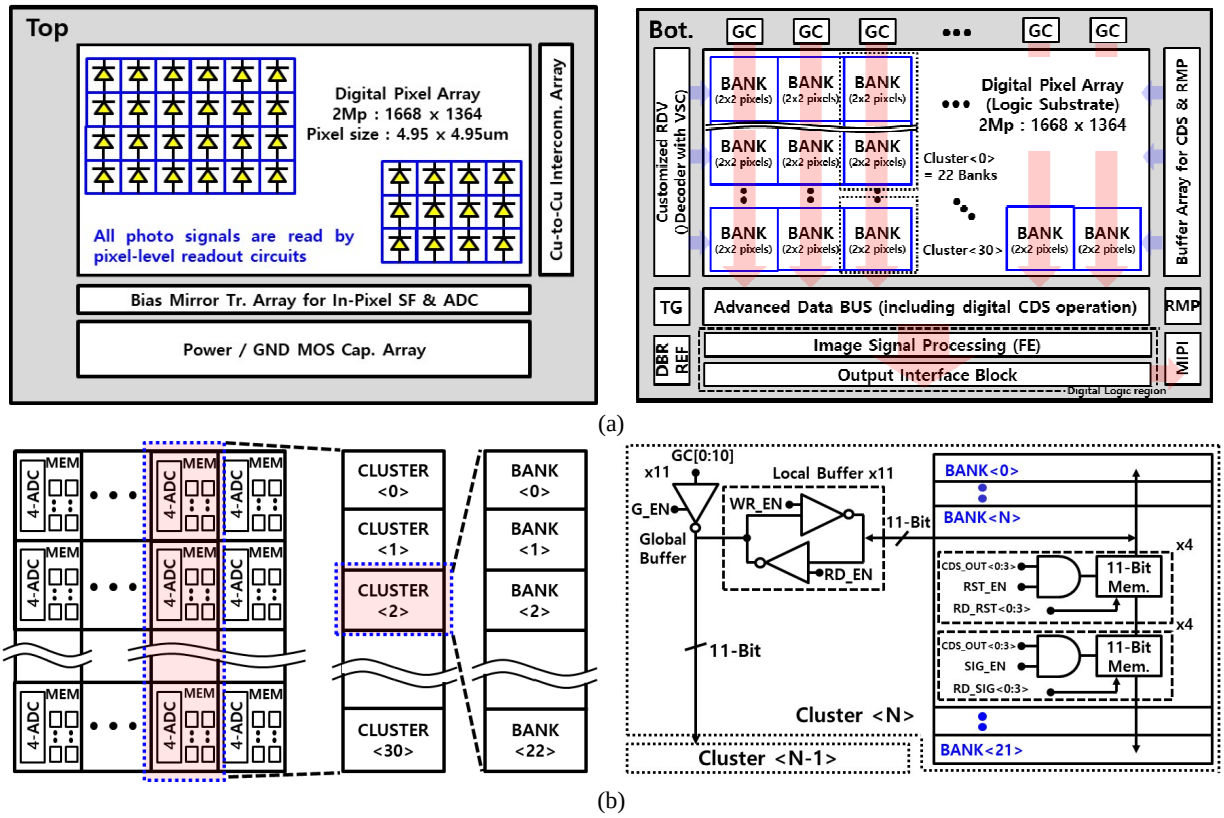


Figure 3. The proposed sensor architecture. (a) Chip diagram. (b) Block diagram of in-pixel memory and data path in-pixel.

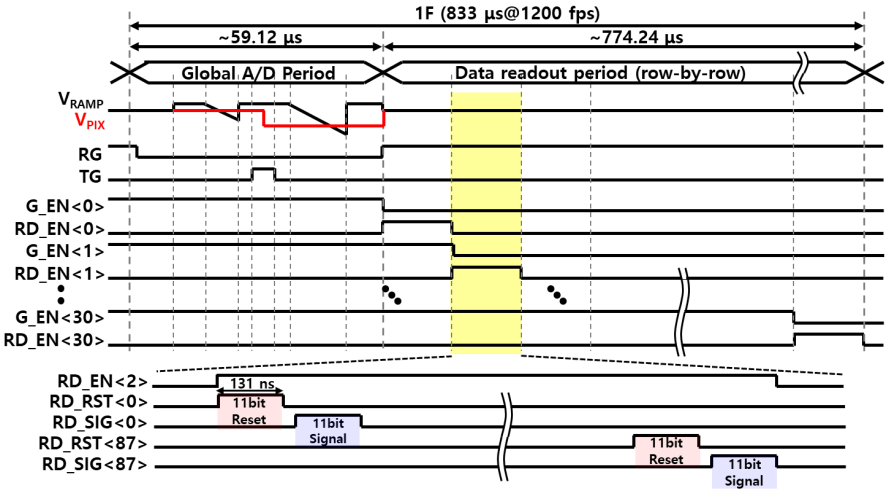


Figure 4. Simplified clock timing for one frame operation.

implement the suggested sensor. Fig. 1 shows the conceptual chip diagram. The prototype is composed of separate pixel and logic substrate for the photo detector and the analog/digital circuitry, respectively. The top chip on the pixel-substrate includes an active pixel sensor (APS) array, a bias circuit block for amplifiers, and a partial pixel-level SS ADC with the 1st-stage operational transconductance amplifier (OTA). The bottom chip on the logic-substrate has the other partial pixel-level ADC including the 2nd-stage OTA, the analog peripheral circuits such as a row driver (RDV), a vertical scanner (VSC) for addressing the pixels, a ramp generator with the horizontal buffers, a gray counter (GC), a doubler (DBR) for supplying the operation powers, timing generator (TG), bandgap reference (BGR), current reference block (REF), and the logic blocks for the image signal process (ISP). Two wafers are connected through a wafer-to-wafer bonding process. The pixel array is 1668H×1364V, and each pixel area is 4.95×4.95 µm^2. Within this area, a unit pixel, one ADC including two 200-fF DRAM capacitors, and 22-bit digital memories are integrated. The schematic diagrams of the in-pixel ADC is shown in Fig. 2. Notice that the 1st-stage OTA of ADC is implemented by combining the pixel substrate with the logic substrate through the extremely narrow pitch C2C bonding of less than 2.5-µm. Fig. 3 (a) and (b) show the simple diagram of sensor architecture and in-pixel memory with its data transfer

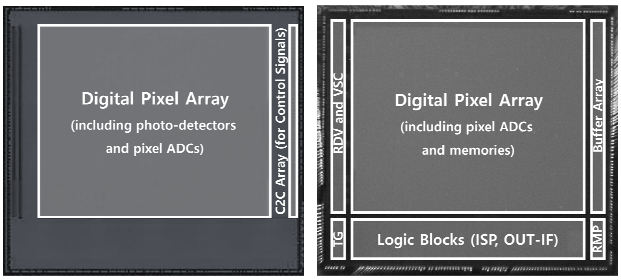


Fig. 5 Chip micrographs (left: top chip, right: bottom chip).

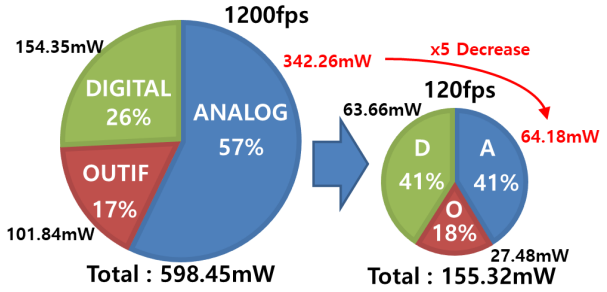
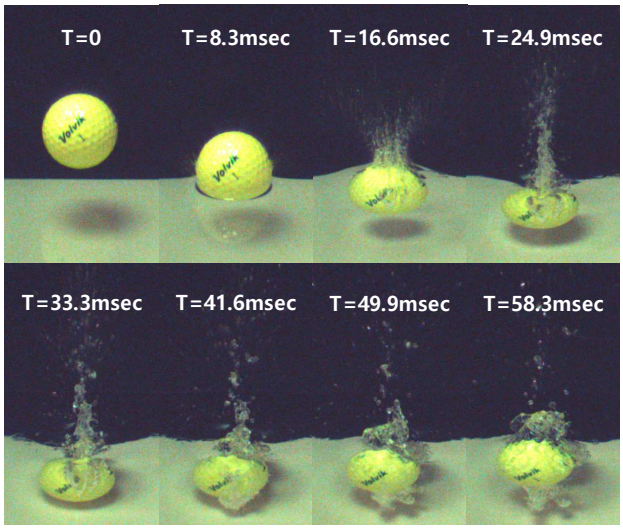
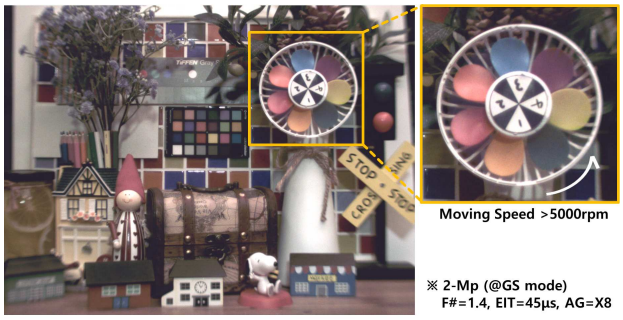


Figure 6. Pie chart of the power consumption distribution.

path, respectively. To effectively organize the sensor operation for the in-pixel digital data writing and reading, two columns comprise 31 CLUSTERs and one CLUSTER contains 22 BANKs. A BANK consists of 2×2 pixel elements, thus, four in-pixel ADCs, and 88-bit memories are laid out under four pixels area. In case of the DPS, for high speed operation, the most difficult design issue is the digital data transfer within very limited time. For addressing this issue, the global buffers (GBs) and the local buffers (LBs) are employed for delivering the data. For example, the count signals are delivered from gray counter (GC) to each BANK through the GBs and LBs, and the ADC results are also transferred from unit pixel to advanced data bus (ADBUS) through the GBs and LBs. A set of GBs and LBs is composed of 11 buffers for 2 columns to drive 11-bit digital codes for the pixel-level ADC resolution. This hierarchical configuration enables high-speed and low-power data transfer compared to conventional sensor architecture. Unlike the global A/D conversion period, the row-by-row readout approach is applied in the data readout period. To read the digital data, the GBs are sequentially deactivated from GB<0> to GB<30> by handling the control signal, G_EN<n> as shown in Fig. 4. The control signal, RD_EN<n>, for LBs is given for enabling the data reading path to the column data transmission line from in-pixel memories. The 11-bit reset and 11-bit signal data of the unit pixels in the CLUSTER are all read out by the control signals, RD_RST<0> to <87> and RD_SIG<0> to <87>, respectively. The transferred data is temporally latched in the ADBUS, then, after performing the digital CDS operation in the ADBUS, the final digital data is moved to the next logic blocks for the image processing. The



(a)



(b)

Figure 7. Sample images of (a) 2-Mp 1200-fps sequential captured image and (b) still-cut with fast-moving fan (Only white balance is applied).

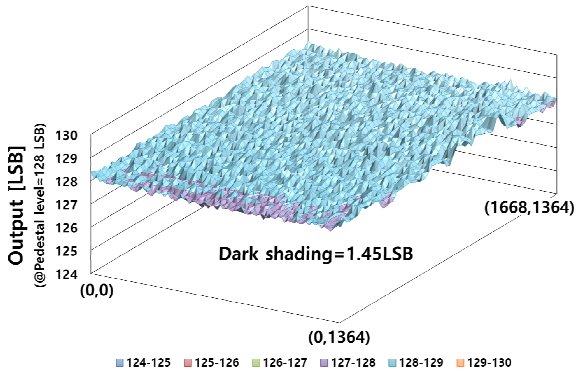


Figure 8. 2-D shading map under dark condition (Analog gain = ×16).

analog circuits only operates during the global A/D period, 59.12 μsec, and they turns into sleep mode to save the power consumption at data readout period. As can be seen in Fig. 4, the global A/D time occupies a small portion of the whole frame time. Thus, even if all in-pixel ADCs operate simultaneously, the power consumption of analog circuits is not critical for achieving the low power performance.

III. Measurement results

A 2-Mp CMOS image sensor with the pixel-parallel

Parameter	This work	[3, ISSCC]	[4, IEDM]	[6, ISSCC]
Process	**65 nm / 28 nm**	90 nm / 65 nm	45nm / 65 nm	65nm / 45 nm
Supply voltage	**2.8 V / 1.05 V**	2.9 V / 1.1 V	2.5 V / 1.2 V	N/A
Array Size	**1668^{H} X 1364^{V}**	1632^{H} X 896^{V}	512^{H} X 512^{V}	4224^{H} X 4224^{V}
Pixel size	**4.95 μm**	6.9 μm	4.6 μm	2.7 μm
Full well capacity	**14 ke-**	16.6 ke-	3.8 ke-	7.4 ke-
Max. frame rate	**1200 fps**	660 fps	480 fps	1000 fps
Readout scheme	**Pixel-parallel ADC**	Pixel-parallel ADC	Pixel-parallel ADC	Array-parallel ADC
Interconnection	**In-pixel C2C**	In-pixel C2C	In-pixel C2C	Pixel-level Inter.
Random noise	**2.6 e-rms (@peak, 24 dB)**	5.15 e-rms (@LN mode)	4.2 e-rms (@0 dB)	2.9 e-rms
In-pixel memory	**22 bits**	14 bits	10 bits	N/A
ADC type	**Single slope**	Single slope	Single slope	Single slope
ADC resolution	**10 bits**	14 bits	10 bits	12
Bias current	**20nA (OTA)**	111nA (OTA, LN)	N/A	N/A
Power	**598.45 mW**	746 mW	5.3 mW(@30fps)	N/A

Table 1. Performance summary and comparison with state-of-the-art CISs for pixel-parallel ADCs.

ADCs is implemented by using 65 nm (pixel substrate) and 28 nm (logic substrate) CIS process. The die micrographs are shown in Fig. 5. Fig. 6 shows the averaged power consumption. The sensor consumes only 598.45mW at 1200 fps and its power significantly decreases as it slowly operates. For example, at 120 fps operating mode, it consumes only 155.32 mW and the power consumption of digital domain becomes a dominant portion of the total power consumption. The images captured by the developed sensor are shown in Fig. 7 (a) and (b). In Fig. 7(a), it shows a ball falling into the water. 7 (b) shows the still–cut image with fast-moving fan rotating at 5000 rpm. Those have been recorded at a frame rate of 1200 fps, due to the high-speed global shutter operation, the shapes in the images are very sharp and it shows no image distortion. The measured dark noise level of 2.6 e-rms with an analog gain (AG) of 16 times. This result shows that the competitive low-noise pixel-parallel ADC can be realized, even if the comparator operates in sub-threshold region for the extremely low-powered operation of the proposed readout architecture. A high pixel conversion gain (CG) of 130 μV/e- for low noise and satisfactorily large full well capacity (FWC) of 14 ke- are achieved. The 2-dimensional dark shading map at AG of 16 times, which is very important evaluation item for global shutter CIS, is shown in Fig. 8. A very small shading value of 70.8 μV is measured at high analog gain condition, even though 2-Mp pixel-parallel ADCs are operating at the same time. This is a sufficiently good performance for most of the imaging applications. The sensor characteristics with the state-of-the-art CISs are summarized in Table 1.

IV. Conclusion

The advanced DPS architecture enabling high-speed and low-power operation is proposed as the next-generation GS CIS. 2-Mp GS-type CMOS image sensor with pixel-parallel ADC and in-pixel memory has been successfully demonstrated. The pitch of each unit pixel is 4.95-μm which is the world's smallest pixel embedding both pixel-level ADC and 22-bit memory. The developed sensor shows the most remarkable performance, such as such as the pixel size, noise, frame rate, and power consumption, among the state-of-the-art published works [3] - [6]. The developed GS image sensor with the pixel- parallel readout architecture will be useful not only as an imaging tool for the mobile, automotive, and machine vision, but also for use in new conceptual imaging applications based on the artificial intelligence (AI) functions.

References

[1] Y. Kumagi et al., Back-Illuminated 2.74 um-Pixel-Pitch Global Shutter CMOS Image Sensor with Charge-Domain Memory Archieving 10k e- Saturation Signal, *IEDM*, Dec. 2018.

[2] J. Lee et al., A 2.1e- Temporal Noise and -105dB Parasitic Light Sensitivity Backside-Illumniated 2.3um-pixel Voltage-Domain GlobalShutter CMOS Image Sensor Using High-Capacity DRAM Capacitor Technology, *ISSCC*, Feb., 2020.

[3] M. Sakakibara et al., A 6.9-um Pixel-Pitch Back-Illuminated Global Shutter CMOS Image Sensor With Pixel-Parallel 14-Bit Subthreshold ADC, *JSSC*, Nov., 2018.

[4] C. Liu et al., A 4.6um, 512x512, Ultra-Low Power Stacked Digital Pixel Sensor with Triple Quantization and 127dB Dynamic Range, IEDM, Dec., 2020.

[5] M. Seo et al., A 2.6 e-rms Low-Random-Noise, 116.2 mW Low-Power 2-Mp Global Shutter CMOS Image Sensor with Pixel-Level ADC and In-Pixel Memory, VLSI, Jun., 2021.

[6] T. Hirata et al., A 1-inch 17Mpixel 1000fps Block-Controlled Coded-Exposure Back-Illuminated Stacked CMOS Image Sensor for Computaional Imaging and Adaptive Dynamic Range Control, ISSCC, Feb., 2021.