A 40000fps global shutter image sensor with 26.7ns 12-bit row readout time

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1 Introduction

In this paper we present a global shutter image sensor with ultra-high-speed readout of 40000fps for scientific applications. Firstly, we include a description of the architecture which allows the high speed performance based on our novel ramp ADC. Secondly, we present techniques to further increase the speed for next generation high-speed sensors.

2 Sensor architecture

The architecture of the sensor is depicted in Fig 1. It has a resolution of 640 x 480 pixels. The pixel architecture is the 8T global shutter with in-pixel storage capacitors and a pitch of 36um. The sensor is implemented in a standard 180nm FSI CIS process. Such mature process node has a good analog performance, therefore we focus on analog techniques to achieve high speed of operation.

In order to reach 40000fps in 180nm node, 2 key techniques were used:

1) Extreme parallelism of 24 ADCs/column, totaling 15360 ADCs per sensor. Such parallelism is made possible by using the simple and area-efficient ramp ADC. Furthermore, each column of pixels is split in 24 column buses (one per ADC) with ground shields in between.
2) 12-bit ramp ADC with 640ns conversion time in digital-correlated-double-sampling mode (DCDS). Such ADCs are known for their simplicity, linearity and low noise, with their main limitation being low speed. To overcome the low speed issue, we developed a new approach that can reduce the required counts by up to 8x, using a manageable 1.4GHz counter clock speed.

The architecture of the ADC is shown in Fig. 2. Each ADC uses 2 parallel comparators with gain 1 and gain 8, and a single counter block. Gain 1 comparator has a ramp steepness that is 8x steeper than gain 8 comparator, and is referred to as fast-ramp comparator. Gain 8 comparator is also referred to as slow-ramp comparator.

The output of only one of the comparators will stop the counter: gain 8 for low-light signals and gain 1 for high-light signals. The high-gain comparator is always connected to the counter while the low gain comparator is only conditionally connected to it. The comparator to use for a specific pixel signal amplitude is chosen as follows: at a moment of time defined by a so-called SEL signal (see Fig. 2), the logic will check if the low-gain comparator has toggled.

a) low-gain comparator has toggled: it means that the pixel signal is a low-light signal and the gain 1 comparator output will not be connected to the counter. The output of the high-gain comparator will remain connected to the counter and will stop it once it has toggled.

b) low-gain comparator did not toggle: output of low-gain comparator will be connected to the counter. As the low-gain comparator uses an 8x faster ramp than the high gain one, it will toggle before the high gain comparator and will be the one to eventually stop the counter.

A bit indicating which gain was selected is saved with the ADC output. The conversion of the reset level of the pixel uses the same gain level chosen during the preceding signal conversion.

As shown in Fig 3, the SNR dip at the switching point between low and high gain is minimal.

Such architecture has several advantages compared to the existing PTC/dual gain-based ramp ADCs such as [2] and [3]:

- Comparators are constantly loaded by the same ramp
- No gain preselection is needed. Gain is chosen during conversion without adding any overhead time
- Signal and reset are converted by the same comparator and same ramp, leading to easier calibration
- Gain variation is defined by the ramp ratio variation and can be calibrated at global level without necessarily requiring a per-column calibration

3 Sensor Performance

With a total AD time of 640ns (including reset and signal conversion), an equivalent readout speed of 78000fps can be achieved, limited to 40000fps due to the 120 IO channels running each at 1.4Gbps. The full capability of the low ADC conversion time can be exploited by halving the number of columns while utilizing all IO channels. In that case, 78000fps can be achieved, while maintaining the full number of rows.

The ADC can also operate in non-DCDS mode. The conversion of the pixel signal is performed in 350ns. Also in this case, the maximum fps is limited by the number of IO channels. Combining this mode with analog CDS stage and column FPN correction could be very useful as it allows to achieve similar noise as in DCDS mode but with almost half the row time.

In high pixel gain mode the sensor achieves 8e- noise and 10ke- full well. The packaged chip and a frame taken at 40000fps are shown in Fig 4. A comparison with great designs of the past [1][2] is shown in Fig. 5.

4 Further speed improvements

The first step to improve the fps of the described sensor is to increase the number of IOs, i.e. increase the data throughput such that the fps can become readout-speed limited.

Next step is to move to BSI technology with reduced tech node (e.g. 65nm and below), ideally combined with 3D stacking. This would increase the readout speed by 4x and above.

First, the lower tech node would allow the doubling of the clock speed of the ADC from 1.4GHz to 2.8GHz, therefore almost halving AD time (ADC overhead remains the limit).

Second, BSI technology would allow an increase in the number of buses per pixel by at least a factor of 2 (the full area of the pixel can be covered by metals without impacting the fill factor). Furthermore, more metal layers could be used, without deteriorating the optical performance (no optical stack increase).

Combining all of the above, the row readout time would reduce to 8.75ns in DCDS mode and 4.68ns in non-DCDS (or analog CDS only) mode, leading to multi-hundred kfps performance.

5 Conclusion

In this paper we have shown that an extremely high readout speed can be achieved by combining the 8T global shutter pixel together with the proposed 12-bit ramp ADC. The ADC could achieve 640ns 12-bit DCDS time thanks to the novel dual gain approach.

To our knowledge, this is among the highest speed ramp ADCs implemented in a product and is among the fastest column ADCs which use DCDS. We also proposed additional improvements which would allow for further conversion time reduction, moving the bottleneck towards the data throughput.

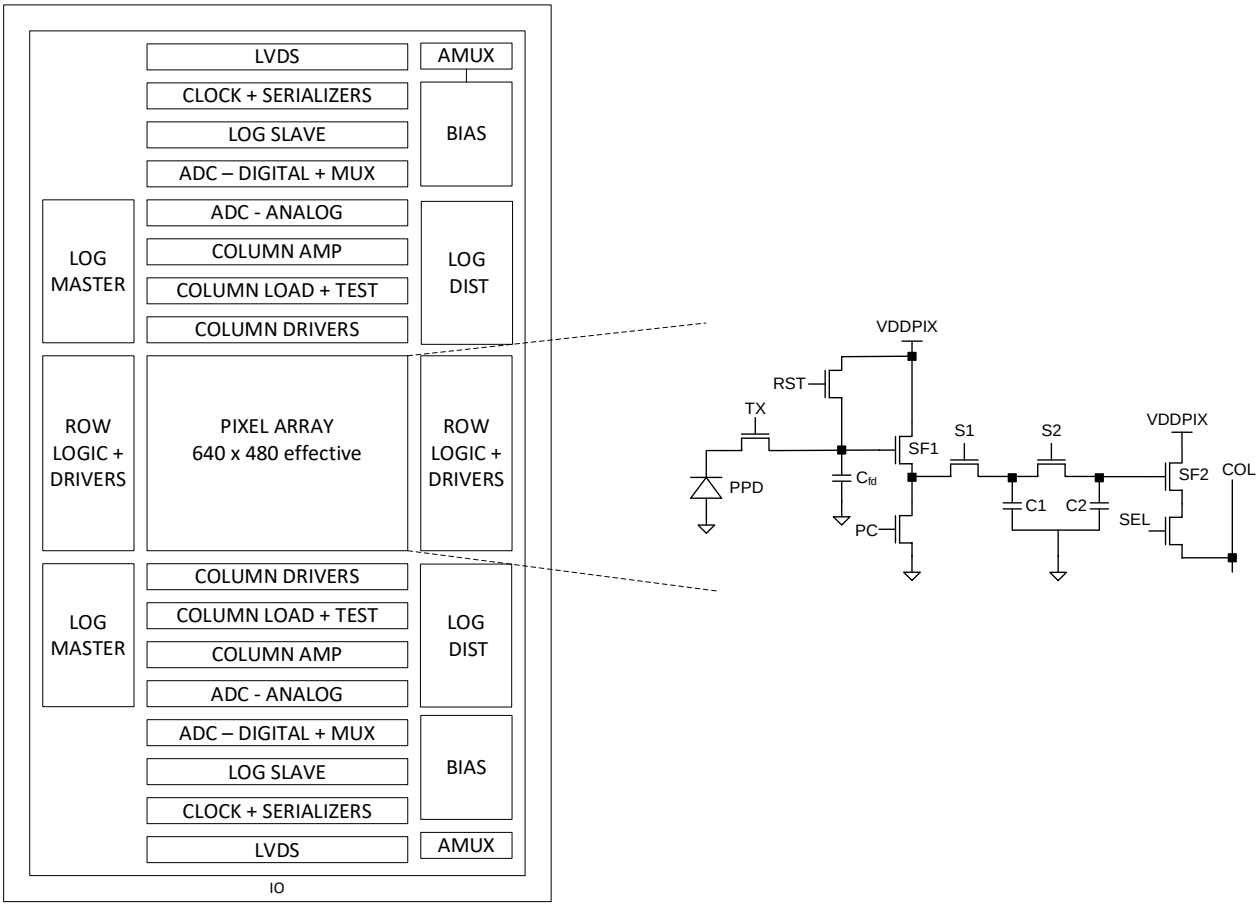

Fig. 1. Architecture of the chip and pixel schematic

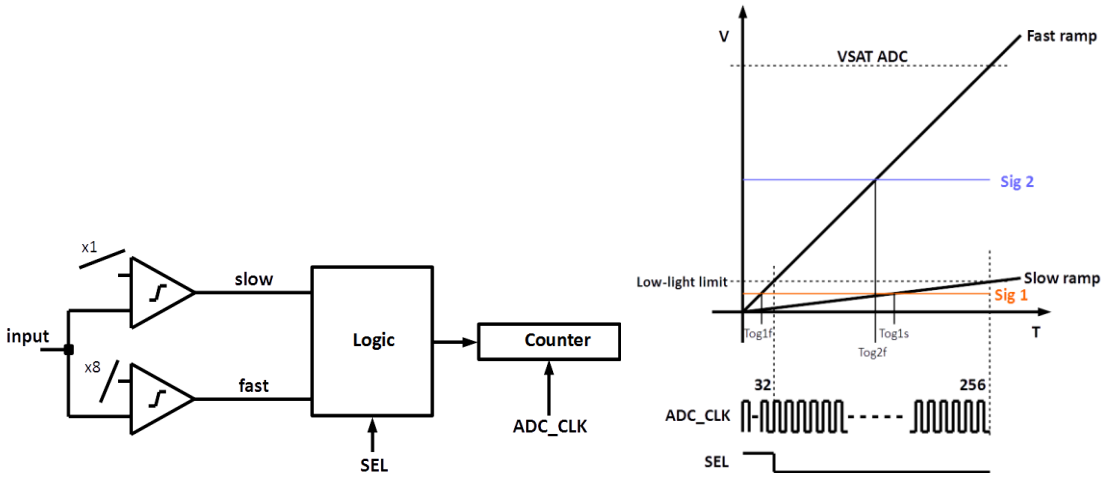

Fig. 2. Dual gain-based ramp ADC. No comparator preselection operation is needed. Instead, the output of the slow ramp comparator or that of the fast ramp comparator is chosen by the logic block to be applied to the counter, optimizing speed, power consumption and ADC area.

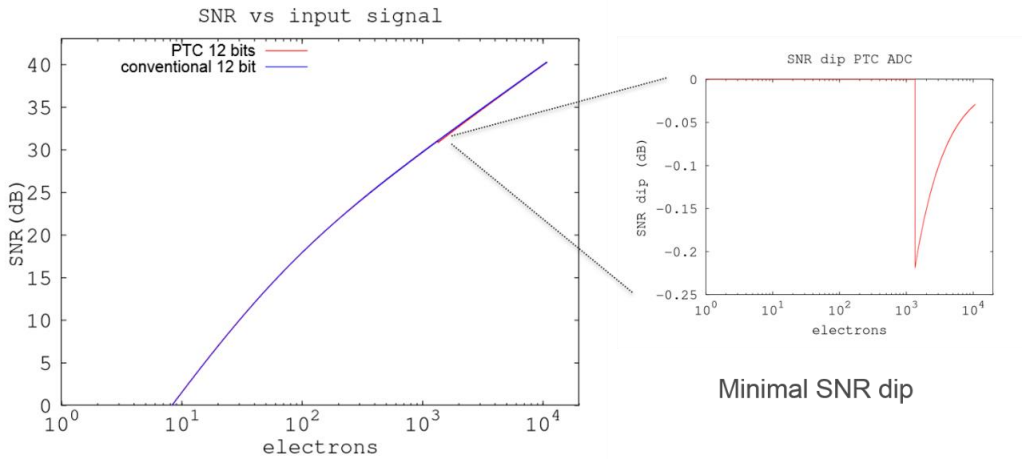

Figure 3 – SNR difference between conventional RAMP ADC and that of the dual-gain (or PTC-based) RAMP ADC with 10ke- full well capacitance

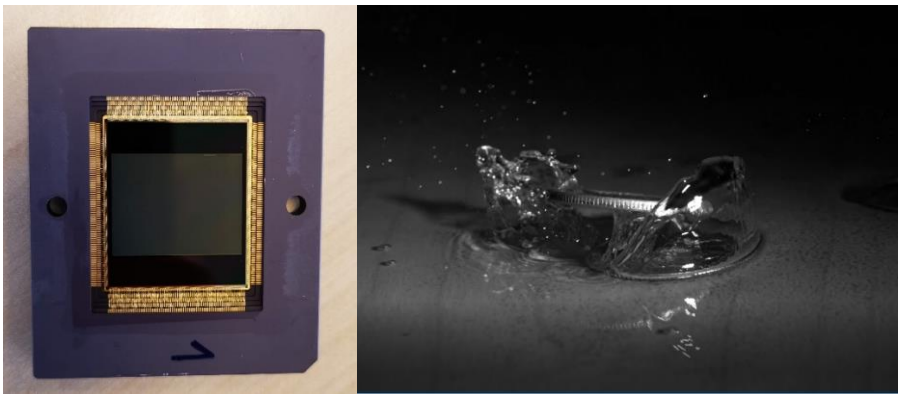

Fig. 4. Packaged chip and sample image taken at 40kfps

Parameter	[1]	[2]	**This work**
technology	180nm FSI	90nm FSI	**180nm FSI**
resolution	2240 x 2240	3840 x 2160	**640 x 480**
shutter	rolling	global	**global**
12 bit ADC time	900ns	6990ns	**640ns (DCDS), 350ns non-CDS**
Row readout time	446ns	964.5ns	**26.7ns**
ADC architecture	Sigma delta	Dual gain ramp	**Dual gain ramp**
noise	5e-	4.6e-	**8e-**
fps	1000	480	**78000 readout, 40000 IO**

Fig. 5. Comparison table

[1] Cremers et al. “A 5 Megapixel, 1000fps CMOS Image Sensor with High Dynamic Range and 14-bit A/D Converters" IISW 2013.

[2] Oike et al, “An 8.3M-pixel 480fps global-shutter CMOS image sensor with gain-adaptive column ADCs and 2-on-1 stacked device structure”, VLSI 2016

[3] Snoeij et al. “Multiple-Ramp Column-Parallel ADC Architectures for CMOS Image Sensors”, JSSC 2007.